**Along the x-axis is the cycle#, and the number of accesses per section is along the y-axis.  
ReadExcel and Write accesses are indicated in two different graphs whenever needed.  
  
applu**The number of clean reads start at 86, but then level off after 100000 cycles and stay at approximately 65 for the remainder of the trace. In other words, data is constantly being moved between the higher caches and memory with the LLC.

**apsi**The number of accesses jumps between 312 and 310, which is relatively constant, across all intervals.

There are no writes for the first 300000 cycles, but this jumps to 310 per interval at around 400000 cycles in. This indicates a heavy overhead in the mid to latter stages of the operation of this workload (as there will be more L1 and L2 cache misses with regard to the beginning). **art\_470**

**Again, we have a relatively constant cycles/interval value. At the very end though, it seems that there is a small amount of read accesses.**

**bwaves\_06**Reads are relatively sporadic through the operation of this workload, but are always at or higher than 538 per interval, which indicates that we are having a significant amount of cache misses for every 50000 cycles. **bzip2\_source**We have a relatively constant amount of read accesses over the 50,000 cycle intervals, ranging from 251 to 241 cycles/interval.

We are writing 250 cycles per interval for all intervals for this workload. **cactusADM\_06**For this benchmark, we have two writes: one at cycle 931168, the other at cycle 1103207.  
Otherwise, we are continuing to read from the L3 cache, but starting around 240 cycles per interval, we end up steadily decreasing until we are below 50 cycles per interval.  
  
  
  
  
  
  
  
**applu~apsi**The reads are relatively sporadic, but they generally center around 375 cycles per interval. This could be that there are fewer cache misses in the higher level caches of the memory hierarchy.

Initially, there are no writes to the cache, but after approximately 300000 cycles, there is a huge increase and there is approximately 310 cycles per interval after this period. Perhaps this is the point where L1 and L2 are full and we are filling more of the contents of L3. **art\_470~bwaves\_06**The number of read accesses to the L3 cache is relatively large after our 1,000,000 cycle forwarding, with over 1200 per 500000 cycles, but then drops suddenly drops to 0 read accesses.

The same goes for the number of write accesses to this cache. **bzip2\_source~cactusADM\_06**The number of read accesses is distributed relatively normally.The number of write accesses for this workload is less evenly distributed.