



VN5772AK-E

Quad smart power solid-state relay for complete H-bridge configurations

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN5772AK-E	100 m Ω ⁽¹⁾	18 A ⁽²⁾	36 V

1. Total resistance of one side in bridge configuration.
2. Typical current limitation value.

■ General features

- Inrush current management by active power limitation on the high-side switches
- Very low standby current
- Very low electromagnetic susceptibility
- Compliant with European directive 2002/95/EC

■ Protections

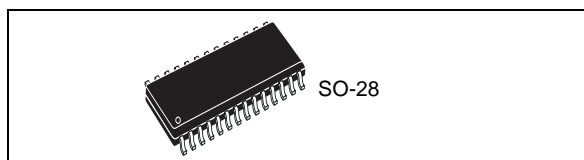
- High-side drivers under voltage shutdown
- Overvoltage clamp
- Output current limitation
- High and low-side overtemperature shutdown
- Short-circuit protection
- ESD protection

■ Diagnostic functions

- Proportional load current sense
- Thermal shutdown indication on both the high and low-side switches

Applications

- DC motor driving in full or half-bridge configuration
- All types of resistive, inductive and capacitive loads



Description

The VN5772AK-E is a device formed by three monolithic chips housed in a standard SO-28 package: a double high-side and two low-side switches. The double high-side is made using STMicroelectronics® VIPower® M0-5 technology, while the low-side switches are fully protected VIPower M0-5 OMNIFET III. This device is suitable to drive a DC motor in a bridge configuration as well as to be used as a quad switch for any low-voltage application. The dual high-side switches integrate built-in non latching thermal shutdown with thermal hysteresis. An output current limiter protects the device in overload conditions. In the case of long overload duration, the device limits the dissipated power to a safe level up to thermal shutdown intervention. An analog current sense pin delivers a current proportional to the load current (according to a known ratio) and indicates overtemperature shutdown of the relevant high-side switch through a voltage flag. The low-side switches have built-in non latching thermal shutdown with thermal hysteresis, linear current limitation and overvoltage clamping. In case of long overload duration, the low-side switches limit the dissipated power to a safe level up to the thermal shutdown intervention. Fault feedback for overtemperature shutdown of the low-side switch is indicated by the relevant status pin.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-28	VN5772AK-E	VN5772AKTR-E

Contents

1	Block diagram and pin description	5
2	Electrical specification	7
2.1	Absolute maximum ratings	7
2.2	Thermal data	8
2.3	Electrical characteristics	9
2.3.1	Electrical characteristics for dual high-side switches	9
2.4	Electrical characteristics curves for dual high-side switches	15
2.5	Electrical characteristics for low-side switch	17
2.6	Electrical characteristics curves for low-side switch	19
3	Application information	21
3.1	Maximum demagnetization energy ($V_{CC} = 13.5 \text{ V}$)	24
4	Package and PC board thermal data	25
4.1	SO-28 thermal data	25
5	Package and packing information	30
5.1	ECOPACK® package	30
5.2	Package mechanical data	30
5.3	Packing information	32
6	Revision history	33

List of tables

Table 1.	Device summary	1
Table 2.	Pin description	6
Table 3.	Dual high-side switch	7
Table 4.	Low side switch.	8
Table 5.	Thermal data.	8
Table 6.	Power section	9
Table 7.	Switching ($V_{CC} = 13\text{ V}$)	9
Table 8.	Logic inputs.	10
Table 9.	Protection and diagnostics	10
Table 10.	Current sense ($8\text{ V} < V_{CC} < 16\text{ V}$)	11
Table 11.	Truth table high-side driver.	13
Table 12.	Electrical transient requirements (part 1/3).	14
Table 13.	Electrical transient requirements (part 2/3).	14
Table 14.	Electrical transient requirements (part 3/3).	14
Table 15.	PowerMOS section - off	17
Table 16.	PowerMOS section - on	17
Table 17.	Switching ($T_j = 25^\circ\text{ C}$, unless otherwise specified)	17
Table 18.	Source drain diode	17
Table 19.	Input section	17
Table 20.	STATUS pin	18
Table 21.	Protection and diagnostics ($-40^\circ\text{ C} < T_j < 150^\circ\text{ C}$, unless otherwise specified)	18
Table 22.	Truth table low-side driver	18
Table 23.	Thermal calculations in clockwise and anti-clockwise operation in steady-state mode . . .	26
Table 24.	Thermal resistances definitions	26
Table 25.	Single pulse thermal impedance definitions	26
Table 26.	Thermal calculations in transient mode	27
Table 27.	Thermal parameters	29
Table 28.	SO-28 mechanical data	31
Table 29.	Document revision history	33

List of figures

Figure 1.	Block diagram	5
Figure 2.	Configuration diagram (top view)	6
Figure 3.	Current sense delay characteristics	12
Figure 4.	Switching time waveforms	12
Figure 5.	Output voltage drop limitation	12
Figure 6.	Off-state output current	15
Figure 7.	High-level input current	15
Figure 8.	Input voltage clamp	15
Figure 9.	Low level input voltage	15
Figure 10.	High-level input voltage	15
Figure 11.	Input voltage hysteresis	15
Figure 12.	On-state resistance vs Tcase	16
Figure 13.	On-state resistance vs VCC	16
Figure 14.	Undervoltage shutdown	16
Figure 15.	Turn-on voltage slope	16
Figure 16.	I_{LIMH} vs Tcase	16
Figure 17.	Turn-off voltage slope	16
Figure 18.	Source diode forward characteristics	19
Figure 19.	Static drain source on-resistance vs drain current (3 pin)	19
Figure 20.	Static drain source on-resistance vs input voltage (3 pin)	19
Figure 21.	Static drain source on-resistance vs drain current	19
Figure 22.	Transfer characteristics	19
Figure 23.	Output characteristics	19
Figure 24.	Normalized on-resistance vs temperature	20
Figure 25.	Normalized input threshold vs temperature	20
Figure 26.	Typical application schematic	21
Figure 27.	Recommended motor operation	22
Figure 28.	Waveforms (high-side switches)	23
Figure 29.	Maximum turn-off current vs load inductance ⁽¹⁾	24
Figure 30.	SO-28 PC board ⁽¹⁾	25
Figure 31.	Chipset configuration	25
Figure 32.	Auto and mutual Rthj-amb vs PCB copper area in open box free air condition ⁽¹⁾	26
Figure 33.	SO-28 HSD thermal impedance junction-ambient single pulse	27
Figure 34.	SO-28 LSD thermal impedance junction-ambient single pulse	28
Figure 35.	Thermal fitting model of an H-bridge in SO-28	29
Figure 36.	SO-28 package dimensions	30
Figure 37.	SO-28 tube shipment (no suffix)	32
Figure 38.	Tape and reel shipment (suffix "TR")	32

1 Block diagram and pin description

Figure 1. Block diagram

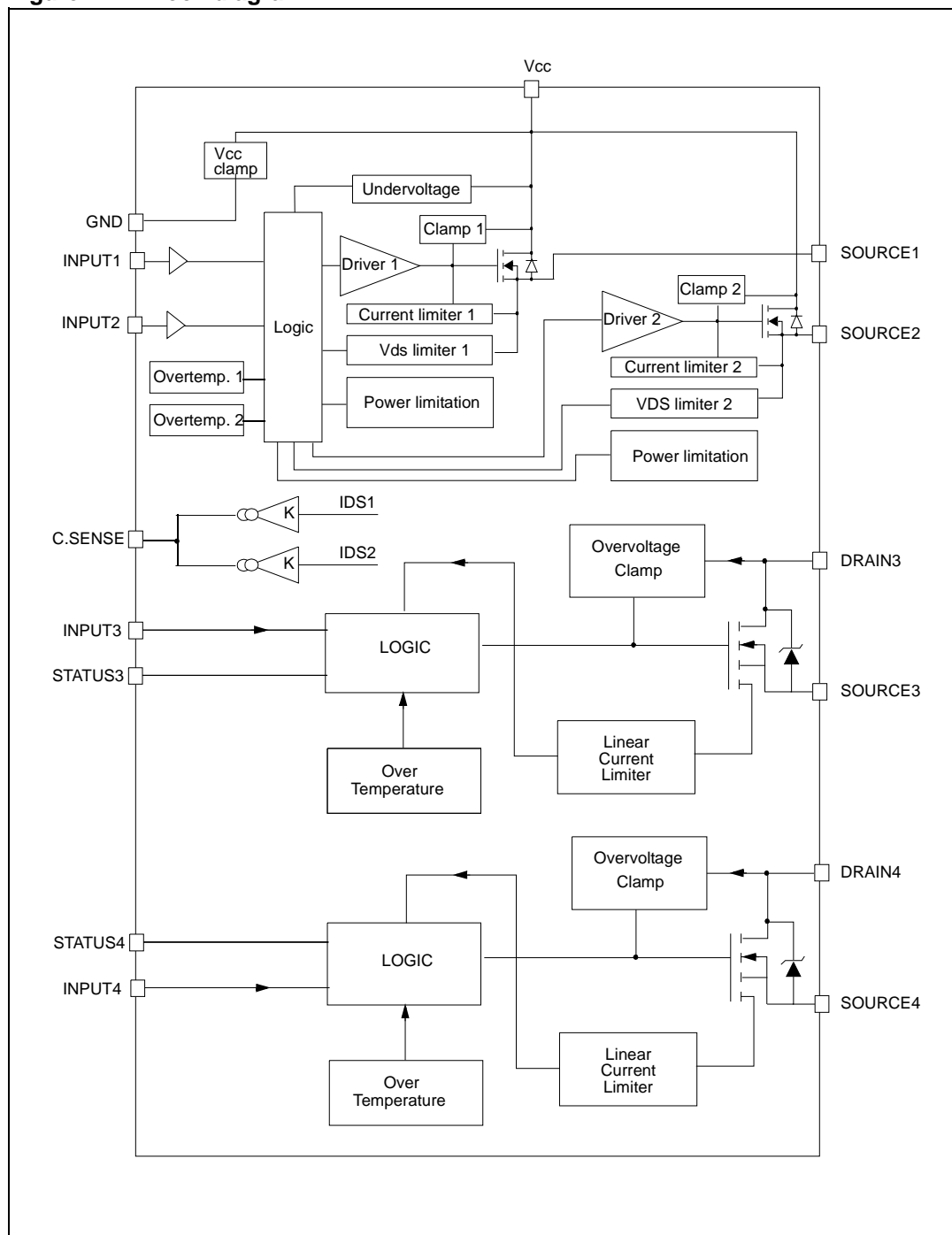
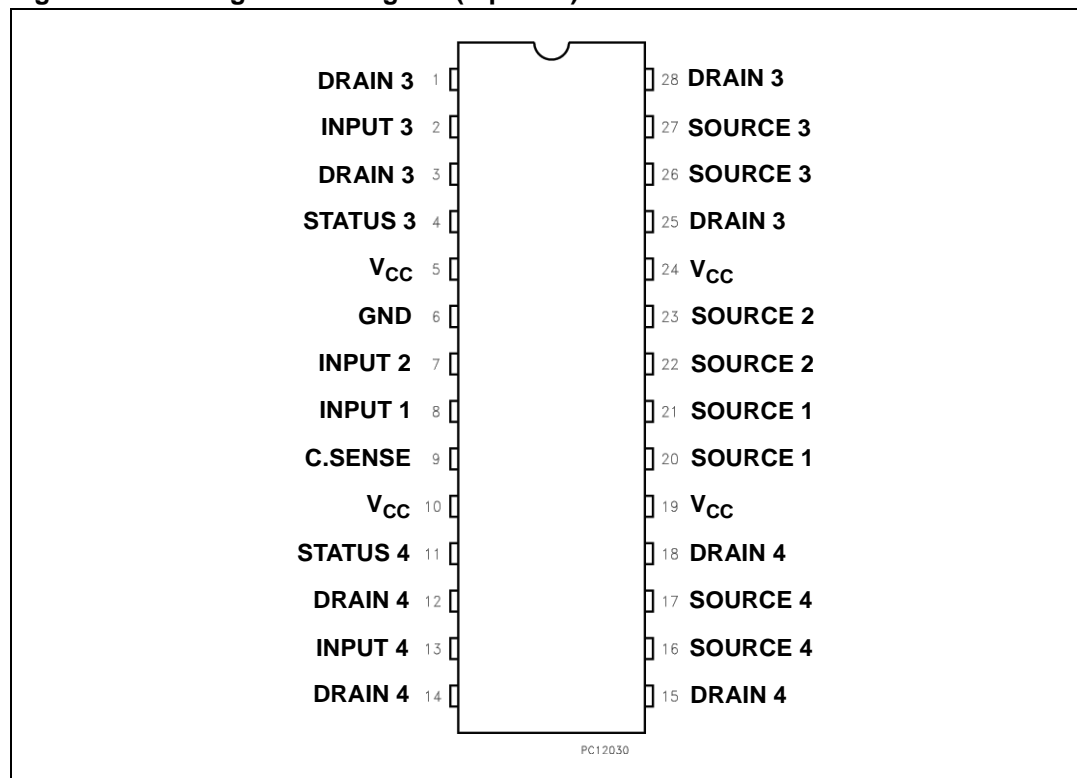


Table 2. Pin description

N° pin	Name	Function
1, 3, 25, 28	DRAIN 3	Drain of switch 3 (low-side switches)
2	INPUT 3	Input of switch 3 (low-side switch)
4	STATUS 3	Status of switch 3 (low-side switch)
11	STATUS 4	Status of switch 4 (low-side switch)
5, 10, 19, 24	V _{CC}	Drain of switches 1 and 2 (high-side switches) and power supply voltage
6	GND	Ground of switches 1 and 2 (high-side switches)
8	INPUT 1	Input of switch 1 (high-side switch)
7	INPUT 2	Input of switch 2 (high-side switch)
9	C.SENSE	Analog current sense pin, delivers a current proportional to the load current
12, 14, 15, 18	DRAIN 4	Drain of switch 4 (low-side switches)
13	INPUT 4	Input of switch 4 (low-side switch)
16, 17	SOURCE 4	Source of switch 4 (low-side switches)
22, 23	SOURCE 2	Source of switch 2 (high-side switches)
20, 21	SOURCE 1	Source of switch 1 (high-side switches)
26, 27	SOURCE 3	Source of switch 3 (low-side switches)

Figure 2. Configuration diagram (top view)

2 Electrical specification

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the tables below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 3. Dual high-side switch

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-12	A
I_{IN}	DC input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse C.SENSE pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	$V_{CC} - 41$ $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) ($L = 3\text{ mH}$; $R_L = 0\ \Omega$; $V_{bat} = 13.5\text{ V}$; $T_{jstart} = 150\text{ }^{\circ}\text{C}$; $I_{OUT} = I_{limL}(Typ.)$)	104	mJ
V_{ESD}	Electrostatic discharge (human body model: $R = 1.5\text{ K}\Omega$; $C = 100\text{ pF}$) – Input – Current sense – $SOURCE_n/DRAIN_n$ – V_{CC}	4000 2000 5000 5000	V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$

Table 4. Low side switch

Symbol	Parameter	Value	Unit
V_{DSn}	Drain-source voltage ($V_{INn} = 0$ V)	Internally clamped	V
I_{INn}	Input current	-1 to 10	mA
I_{Dn}	Drain current	Internally limited	A
$-I_{Dn}$	Reverse DC output current	-4	A
I_{STAT}	DC status current	-1 to 10	mA
V_{ESD1}	Electrostatic discharge ($R = 1.5$ K Ω , $C = 100$ pF): – Drain – Supply, status, input	5000 4000	V
V_{ESD2}	Electrostatic discharge on output pins only ($R = 330$ Ω , $C = 150$ pF)	2000	V
T_j	Operating junction-temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj-leadHS}$	Thermal resistance junction-case (high-side switch)	22	°C/W
$R_{thj-leadLS}$	Thermal resistance junction-case (low-side switch)	21	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (high-side switch)	47	°C/W
	Thermal resistance junction-ambient (low-side switch)	57	°C/W

2.3 Electrical characteristics

2.3.1 Electrical characteristics for dual high-side switches

Values specified in this section are for $8\text{ V} < V_{CC} < 36\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise specified (for each channel).

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance	$I_{OUT} = 3\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$			50	$\text{m}\Omega$
		$I_{OUT} = 3\text{ A}$; $T_j = 150\text{ }^{\circ}\text{C}$			100	
		$I_{OUT} = 3\text{ A}$; $V_{CC} = 5\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$			65	
V_{clamp}	Voltage clamp	$I_S = 20\text{ mA}$	41	46	52	V
I_S	Supply current	Off-state: $V_{CC} = 13\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$, $V_{IN} = V_{OUT} = V_{SENSE} = 0\text{ V}$		2 ⁽¹⁾	5 ⁽¹⁾	μA
		On-state: $V_{CC} = 13\text{ V}$; $V_{IN} = 5\text{ V}$, $I_{OUT} = 0\text{ A}$		3	6	mA
$I_{L(off)}$	Off-state output current ⁽²⁾	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$, $T_j = 25\text{ }^{\circ}\text{C}$	0	0.01	3	μA
		$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$, $T_j = 125\text{ }^{\circ}\text{C}$	0		5	
V_F	Output - V_{CC} diode voltage ⁽²⁾	$I_{OUT} = 3\text{ A}$, $T_j = 150\text{ }^{\circ}\text{C}$			0.7	V

1. PowerMOS leakage included.

2. For each channel.

Table 7. Switching ($V_{CC} = 13\text{ V}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 6.5\text{ }\Omega$ (see Figure 4)	—	25	—	μs
$t_{d(off)}$	Turn-off delay time	$R_L = 6.5\text{ }\Omega$ (see Figure 4)	—	20	—	μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 6.5\text{ }\Omega$	—	See Figure 15	—	$\text{V}/\mu\text{s}$
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L = 6.5\text{ }\Omega$	—	See Figure 17	—	$\text{V}/\mu\text{s}$

Table 7. Switching ($V_{CC} = 13\text{ V}$) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
W_{ON}	Switching energy losses during t_{won}	$R_L = 6.5\ \Omega$ (see Figure 4)	—	0.24	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_L = 6.5\ \Omega$ (see Figure 4)	—	0.2	—	mJ

Table 8. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage				0.9	V
I_{IL}	Low-level input current	$V_{IN} = 0.9\text{ V}$	1			μA
V_{IH}	High-level input voltage		2.1			V
I_{IH}	High-level input current	$V_{IN} = 2.1\text{ V}$			10	μA
$V_{I(hyst)}$	Input voltage hysteresis		0.25			V
V_{ICL}	Input voltage clamp	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		

Table 9. Protection and diagnostics⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short-circuit current	$V_{CC} = 13\text{ V}$	12	18	24	A
		$5\text{ V} < V_{CC} < 36\text{ V}$			24	A
I_{limL}	Short-circuit current during thermal cycling	$V_{CC} = 13\text{ V}; T_R < T_j < T_{TSD}$		7		A
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
T_R	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}\text{C}$
T_{RS}	Thermal reset of STATUS		135			$^{\circ}\text{C}$
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)			7		$^{\circ}\text{C}$
V_{DEMAG}	Turn-off output voltage clamp	$I_{OUT} = 2\text{ A}; V_{IN} = 0; L = 6\text{ mH}$	$V_{CC} - 41$	$V_{CC} - 46$	$V_{CC} - 52$	V
V_{ON}	Output voltage drop limitation	$I_{OUT} = 0.1\text{ A}, T_j = -40\text{ }^{\circ}\text{C} \text{ to } 150\text{ }^{\circ}\text{C}$ (see Figure 5)		25		mV

1. To ensure long-term reliability under heavy overload or short-circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Current sense ($8\text{ V} < V_{CC} < 16\text{ V}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT} / I_{SENSE}	$I_{OUT} = 0.35\text{ A}$; $V_{SENSE} = 0.5\text{ V}$; $T_j = -40\text{ }^{\circ}\text{C}$ to $50\text{ }^{\circ}\text{C}$	1430	2140	2890	
K_1	I_{OUT} / I_{SENSE}	$I_{OUT} = 1\text{ A}$; $V_{SENSE} = 0.5\text{ V}$; $T_j = -40\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$ $T_j = 25\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$	1470 1570	2020 2020	2610 2470	
K_2	I_{OUT} / I_{SENSE}	$I_{OUT} = 2\text{ A}$; $V_{SENSE} = 4\text{ V}$; $T_j = -40\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$ $T_j = 25\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$	1740 1790	2020 2020	2320 2250	
K_3	I_{OUT} / I_{SENSE}	$I_{OUT} = 6\text{ A}$; $V_{SENSE} = 4\text{ V}$; $T_j = -40\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$ $T_j = 25\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$	1890 1890	2010 2010	2140 2140	
V_{SENSE}	Max analog sense output voltage	$I_{OUT} = 4\text{ A}$;	5			V
I_{SENSE0}	Analog sense leakage current	$I_{OUT} = 0\text{ A}$, $V_{SENSE} = 0\text{ V}$, $V_{IN} = 0\text{ V}$, $T_j = -40\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$	0		1	μA
		$I_{OUT} = 0\text{ A}$, $V_{SENSE} = 0\text{ V}$, $V_{IN} = 5\text{ V}$, $T_j = -40\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$	0		2	
V_{SENSEH}	Analog sense output voltage in overtemperature condition	$V_{CC} = 13\text{ V}$, $R_{SENSE} = 10\text{ K}\Omega$		9		V
I_{SENSEH}	Analog sense output current in overtemperature condition	$V_{CC} = 13\text{ V}$, $V_{SENSE} = 5\text{ V}$		8		mA
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	$V_{SENSE} < 4\text{ V}$, $0.5\text{ A} < I_{OUT} < 4\text{ A}$, $I_{SENSE} = 90\%$ of $I_{SENSE\text{ max}}$ (see Figure 3)		80	250	μs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	$V_{SENSE} < 4\text{ V}$, $0.5\text{ A} < I_{OUT} < 4\text{ A}$, $I_{SENSE} = 10\%$ of $I_{SENSE\text{ max}}$ (see Figure 3)		100	250	μs

Figure 3. Current sense delay characteristics

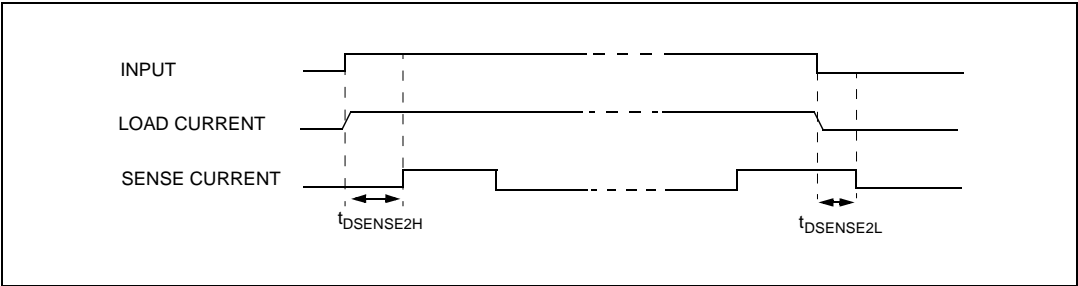


Figure 4. Switching time waveforms

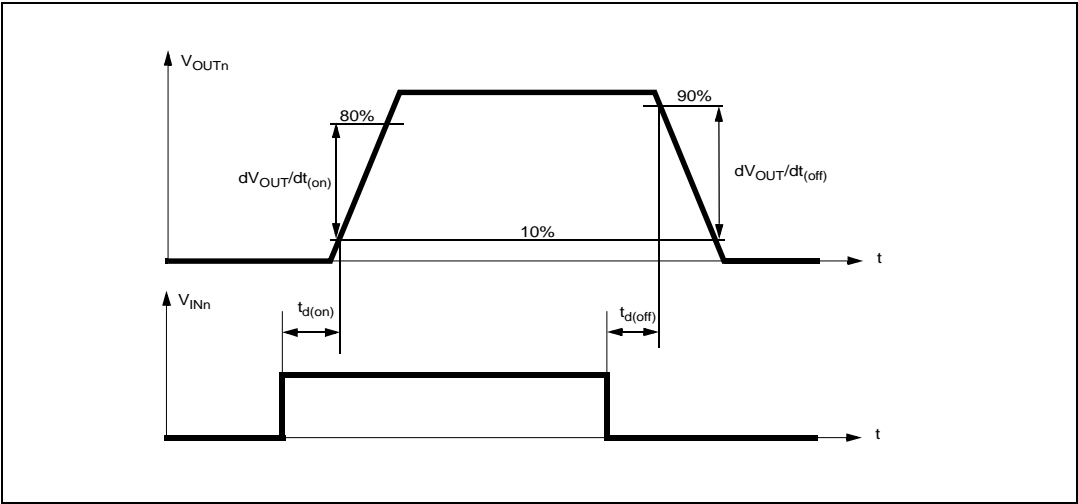


Figure 5. Output voltage drop limitation

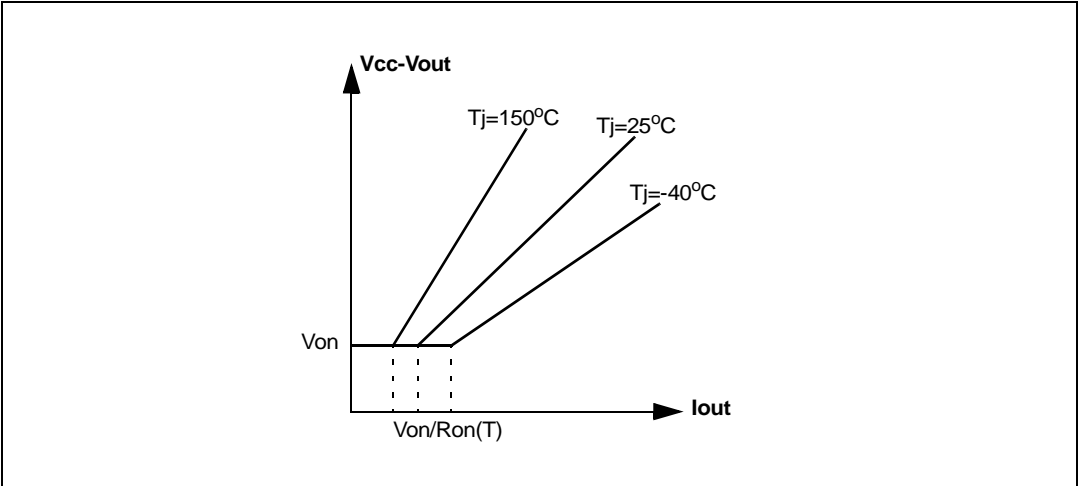


Table 11. Truth table high-side driver

Conditions	Input	Output	Sense
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Short-circuit to GND ($R_{SC} \leq 10 \text{ m}\Omega$)	L	L	0
	H	L	0 if $T_j < T_{TSD}$
	H	L	V_{SENSEH} if $T_j > T_{TSD}$
Short-circuit to V_{CC}	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

Table 12. Electrical transient requirements (part 1/3)⁽¹⁾

ISO 7637-2: 2004(E) test pulse	Test levels ⁽²⁾		Number of pulses or test times	Burst cycle / pulse repetition time		Delays and Impedance
	III	IV				
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50μs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1μs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1μs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b ⁽³⁾	+65V	+87V	1 pulse			400ms, 2Ω

1. Valid for HSD and H-bridge configuration
2. The above test levels must be considered referred to $V_{CC} = 13.5$ V except for pulse 5b.
3. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 13. Electrical transient requirements (part 2/3)

ISO 7637-2: 2004E test pulse	Test level results ⁽¹⁾	
	III	VI
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b ⁽²⁾	C	C

1. The above test levels must be considered referred to $V_{CC} = 13.5$ V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 14. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Electrical characteristics curves for dual high-side switches

Figure 6. Off-state output current

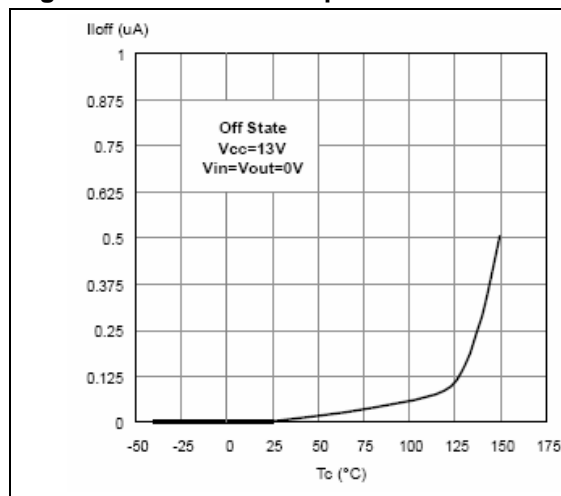


Figure 7. High-level input current

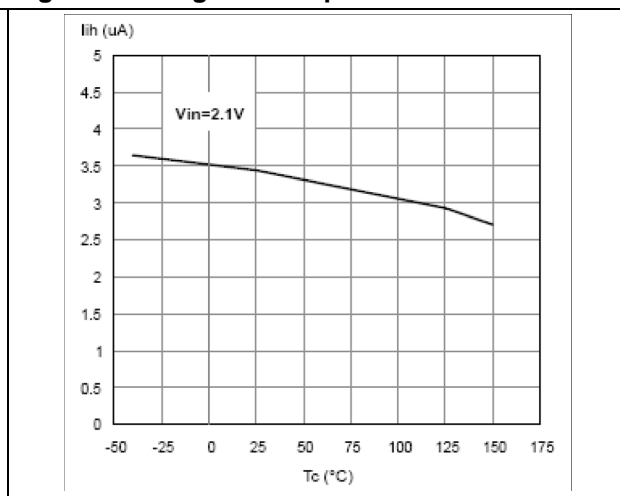


Figure 8. Input voltage clamp

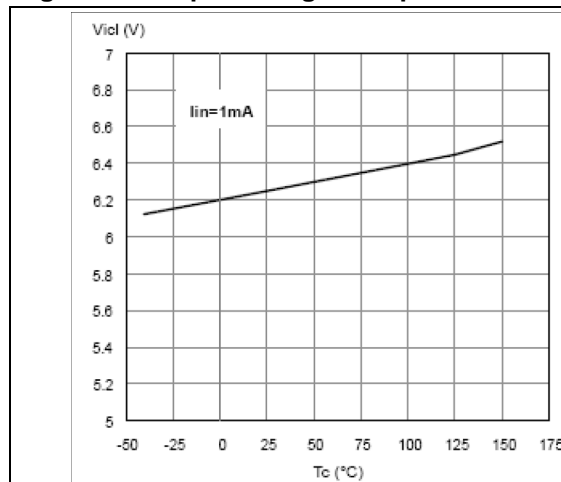


Figure 9. Low level input voltage

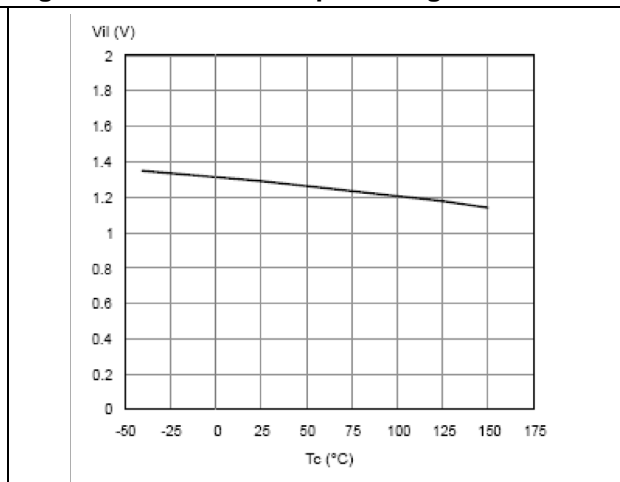


Figure 10. High-level input voltage

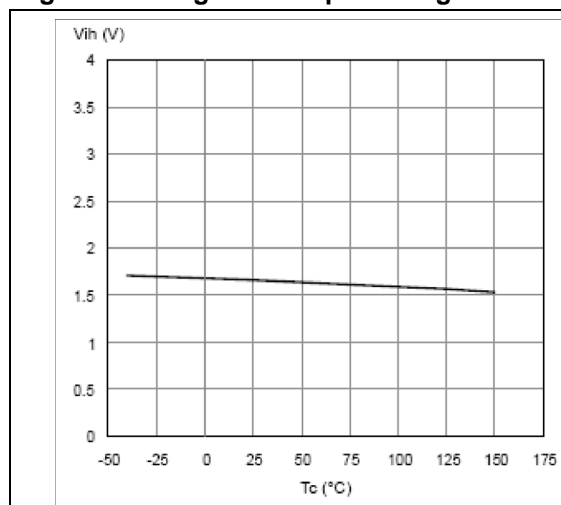


Figure 11. Input voltage hysteresis

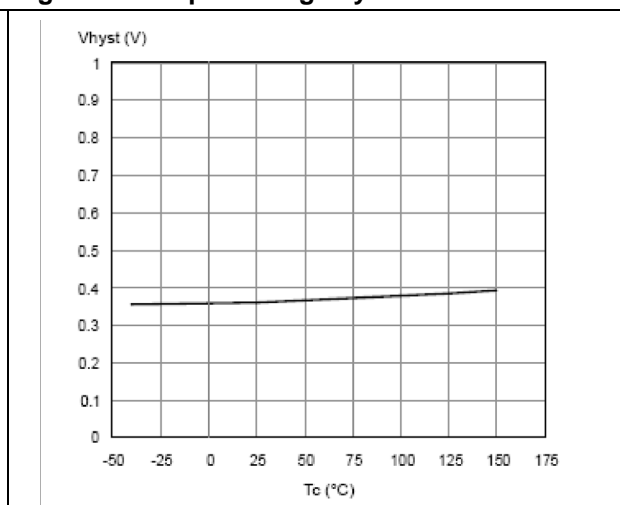


Figure 12. On-state resistance vs T_{case}

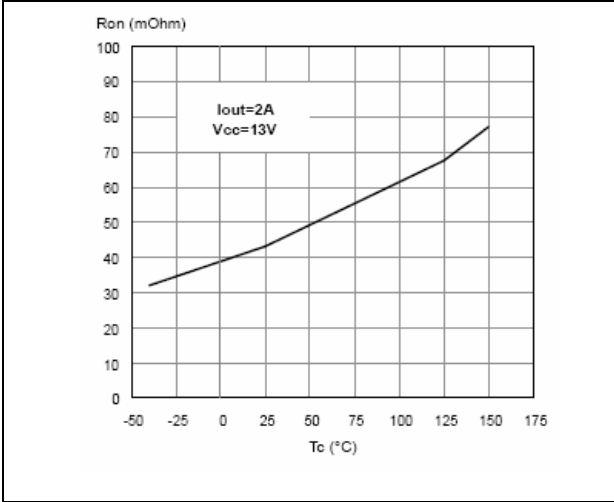


Figure 13. On-state resistance vs V_{CC}

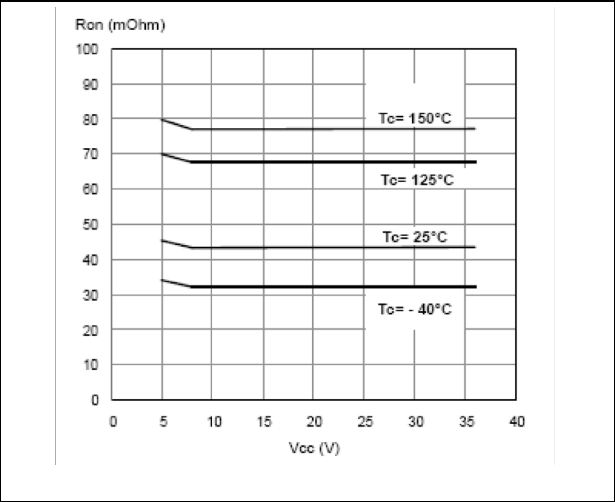


Figure 14. Undervoltage shutdown

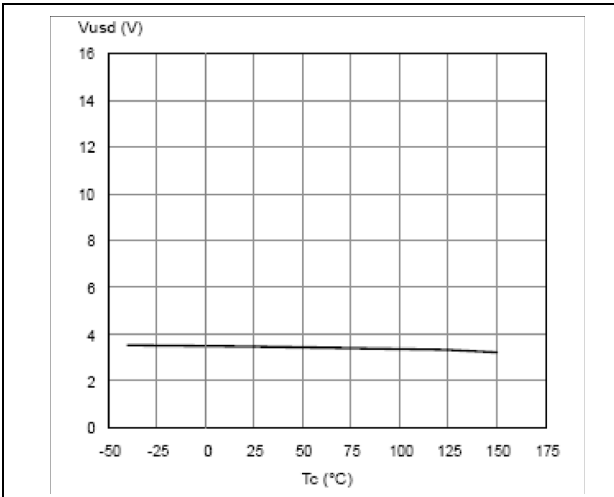


Figure 15. Turn-on voltage slope

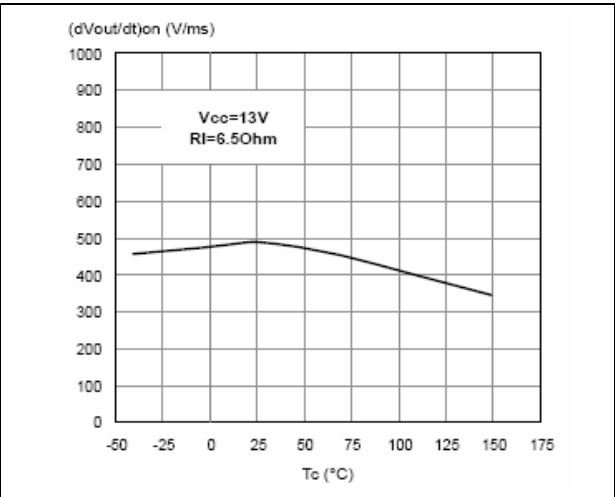


Figure 16. I_{LIMH} vs T_{case}

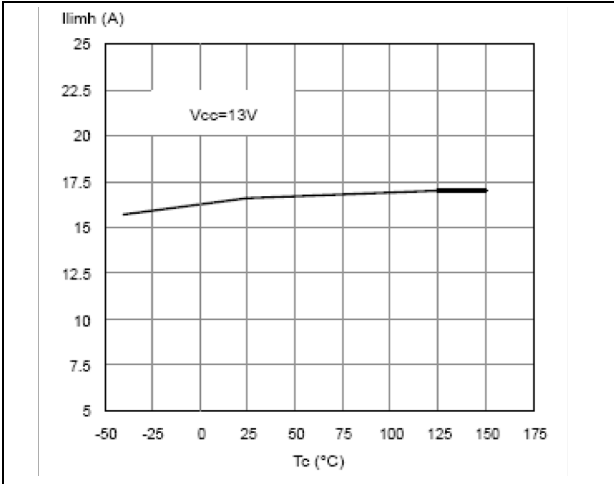
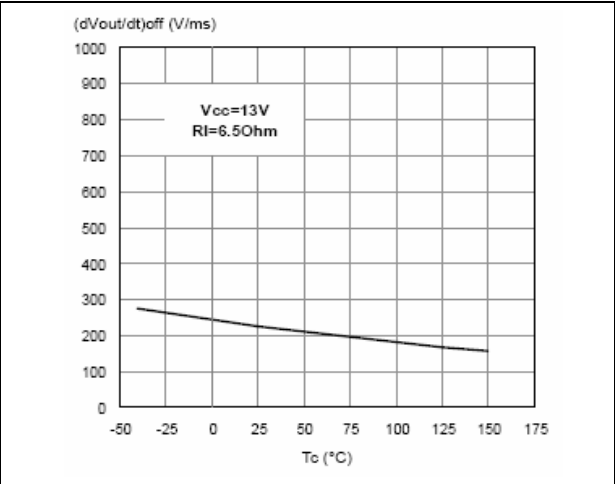


Figure 17. Turn-off voltage slope



2.5 Electrical characteristics for low-side switch

Values specified in this section are for $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise specified

Table 15. PowerMOS section - off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CLAMP}	Drain-source voltage clamp	$V_{\text{IN}} = 0\text{ V}; I_{\text{D}} = 2\text{ A}$	41	46	52	V
V_{CLTH}	Drain-source threshold voltage clamp	$V_{\text{IN}} = 0\text{ V}; I_{\text{D}} = 2\text{ mA}$	36			V
I_{DSS}	Zero input voltage Drain current ($V_{\text{IN}} = 0\text{ V}$)	$V_{\text{DS}} = 13\text{ V}; V_{\text{IN}} = 0\text{ V}; T_j = 25^{\circ}\text{C}$	0		3	μA
		$V_{\text{DS}} = 13\text{ V}; V_{\text{IN}} = 0\text{ V}; T_j = 125^{\circ}\text{C}$	0		5	

Table 16. PowerMOS section - on

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{IN}} = 5\text{ V}; I_{\text{D}} = 2\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$	—	—	50	$\text{m}\Omega$
		$V_{\text{IN}} = 5\text{ V}; I_{\text{D}} = 2\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	—	—	100	$\text{m}\Omega$

Table 17. Switching ($T_j = 25^{\circ}\text{C}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$R_{\text{L}} = 6.5\text{ }\Omega; V_{\text{CC}} = 13\text{ V}$	—	6	—	μs
$t_{\text{d(off)}}$	Turn-off delay time	$R_{\text{L}} = 6.5\text{ }\Omega; V_{\text{CC}} = 13\text{ V}$	—	20	—	μs
t_{r}	Turn-on voltage slope	$R_{\text{L}} = 6.5\text{ }\Omega; V_{\text{CC}} = 13\text{ V}$	—	10	—	μs
t_{f}	Turn-off voltage slope	$R_{\text{L}} = 6.5\text{ }\Omega; V_{\text{CC}} = 13\text{ V}$	—	10	—	μs
W_{ON}	Switching energy losses during t_{won}	$R_{\text{L}} = 6.5\text{ }\Omega; V_{\text{CC}} = 13\text{ V}$	—	0.04	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_{\text{L}} = 6.5\text{ }\Omega; V_{\text{CC}} = 13\text{ V}$	—	0.06	—	mJ

Table 18. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{\text{SD}}^{(1)}$	Forward on voltage	$I_{\text{SD}} = 2\text{ A}; V_{\text{IN}} = 0\text{ V}$	—	0.8	—	V

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 19. Input section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ISS}	Supply current from input pin	On-state: $V_{\text{IN}} = 5\text{ V}; V_{\text{DS}} = 0\text{ V}$		30	110	μA

Table 19. Input section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ICL}	Input voltage clamp	$I_S = 1 \text{ mA}$	5.5		7	V
		$I_S = -1 \text{ mA}$		-0.7		
V_{INTH}	Input voltage threshold	$V_{DS} = V_{IN}; I_D = 1 \text{ mA}$	1		3.5	V

Table 20. STATUS pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	$I_{STAT} = 1 \text{ mA}$			0.5	V
I_{LSTAT}	Status leakage current	Normal operation, $V_{STAT} = 5 \text{ V}$			10	μA
C_{STAT}	STATUS pin input capacitance	Normal operation, $V_{STAT} = 5 \text{ V}$			100	pF
V_{STCL}	Status voltage clamp	$I_{STAT} = 1 \text{ mA}$	5.5		7	V
		$I_{STAT} = -1 \text{ mA}$		-0.7		

Table 21. Protection and diagnostics ($-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short-circuit current	$V_{DS} = 13 \text{ V}, V_{IN} = 5 \text{ V}$	19	27	38	A
I_{limL}	Short-circuit current during thermal cycling	$V_{DS} = 13 \text{ V}, T_R < T_j < T_{TSD}$		11		A
t_{dlim}	Step response current limit	$V_{IN} = 5 \text{ V}, V_{DS} = 13 \text{ V}$		20		μs
T_{TSD}	Overtemperature shutdown		150	175	200	$^\circ\text{C}$
T_R	Overtemperature reset		135			$^\circ\text{C}$

Table 22. Truth table low-side driver

Conditions	Input	Drain	Status
Normal operation	L	H	H
	H	L	H
Overtemperature	L	H	H
	H	H	L

2.6 Electrical characteristics curves for low-side switch

Figure 18. Source diode forward characteristics

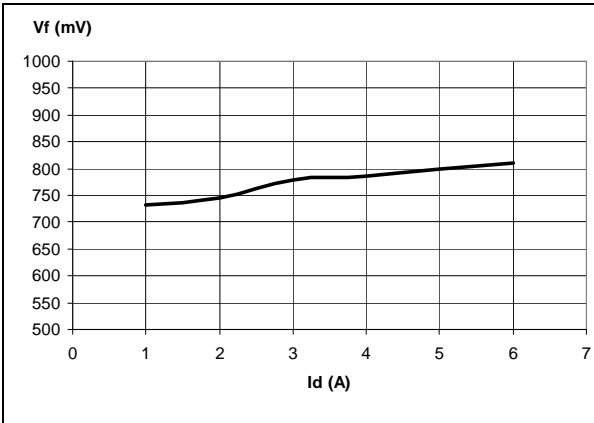


Figure 19. Static drain source on-resistance vs drain current (3 pin)

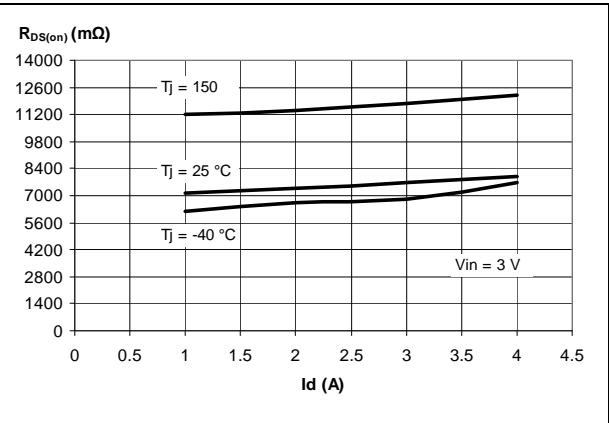


Figure 20. Static drain source on-resistance vs input voltage (3 pin)

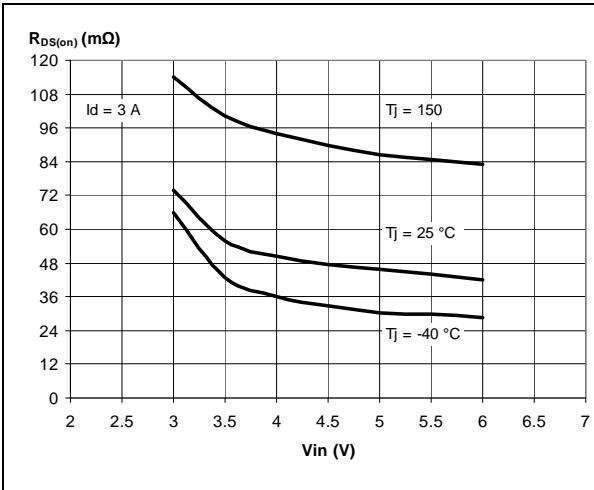


Figure 21. Static drain source on-resistance vs drain current

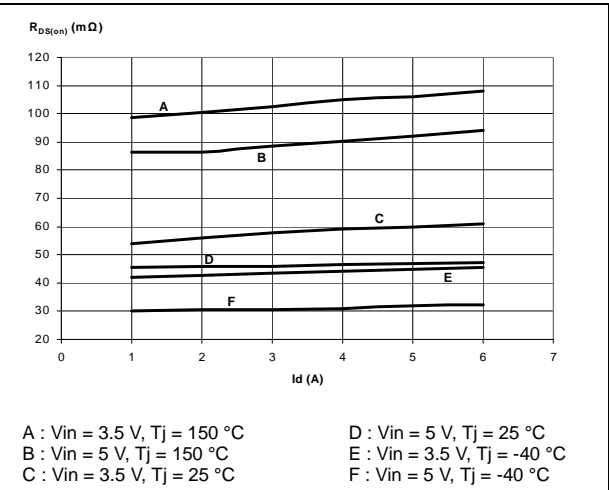


Figure 22. Transfer characteristics

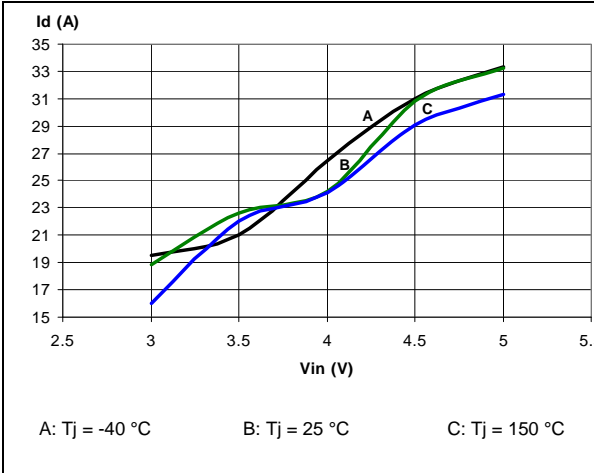


Figure 23. Output characteristics

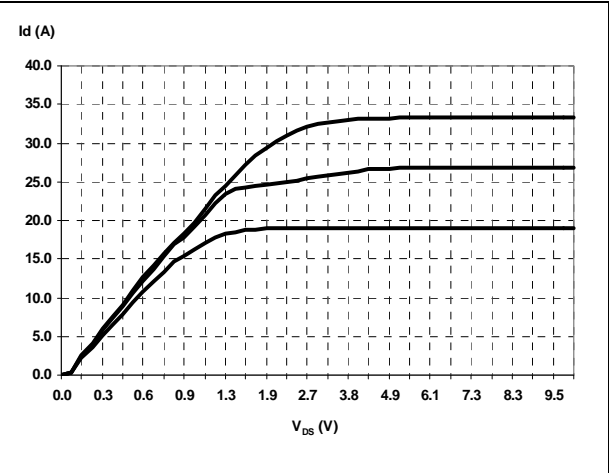


Figure 24. Normalized on-resistance vs temperature

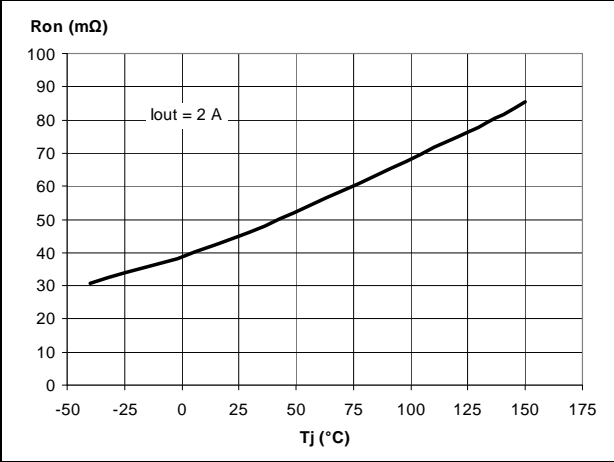
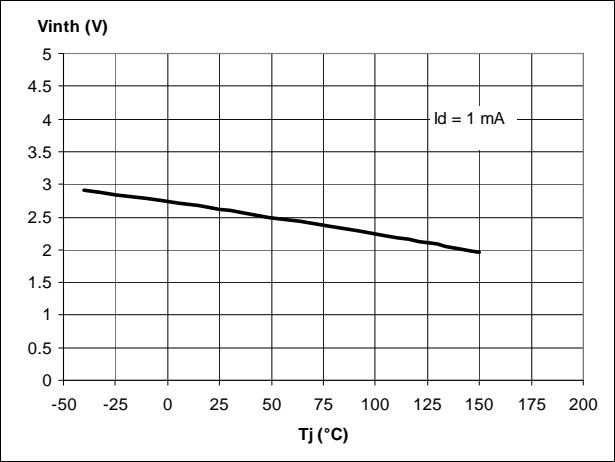
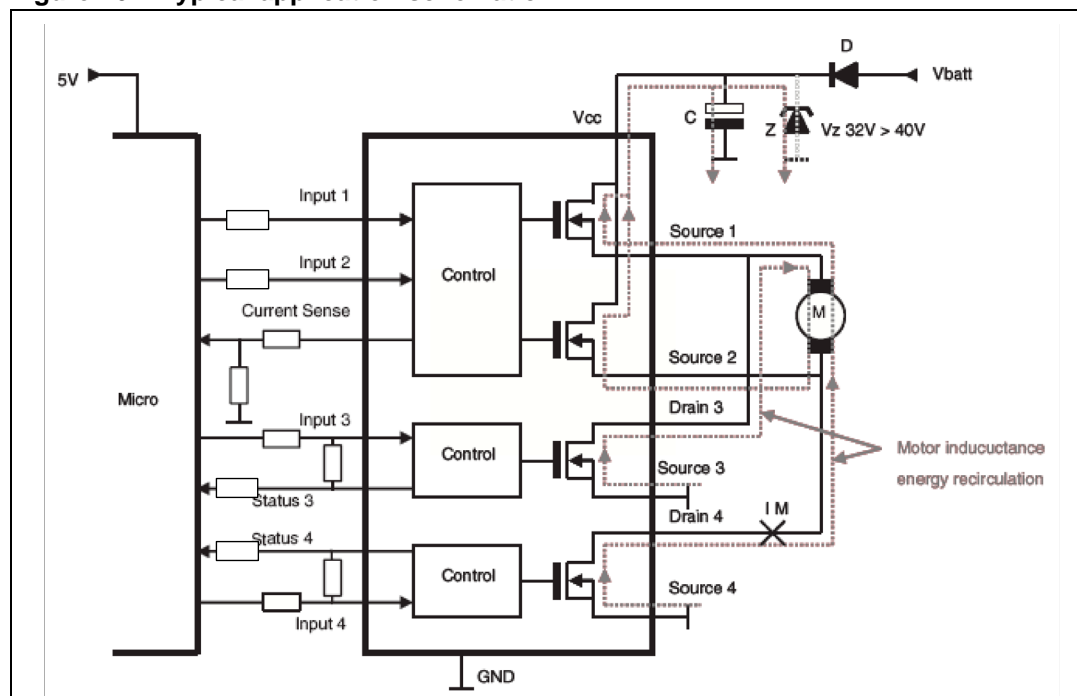


Figure 25. Normalized input threshold vs temperature



3 Application information

Figure 26. Typical application schematic



Mostly motor bridge drivers use a reverse battery protection diode (D) inside supply rail. This diode prevents a reverse current flow back to Vbatt in case the bridge gets disabled via the logic inputs while motor inductance still carries energy. In order to prevent a hazardous overvoltage at circuit supply terminal (V_{CC}), a blocking capacitor (C) is needed to limit the voltage overshoot. As basic orientation, 50 μF per 1 A load current is recommended. In alternative, also a Zener protection (Z) is suitable.

Even if a reverse polarity diode is not present, it is recommended to use a capacitor or zener at V_{CC} because a similar problem appears in case supply terminal of the module has intermittent electrical contact to the battery or gets disconnected while motor is operating.

Figure 27. Recommended motor operation

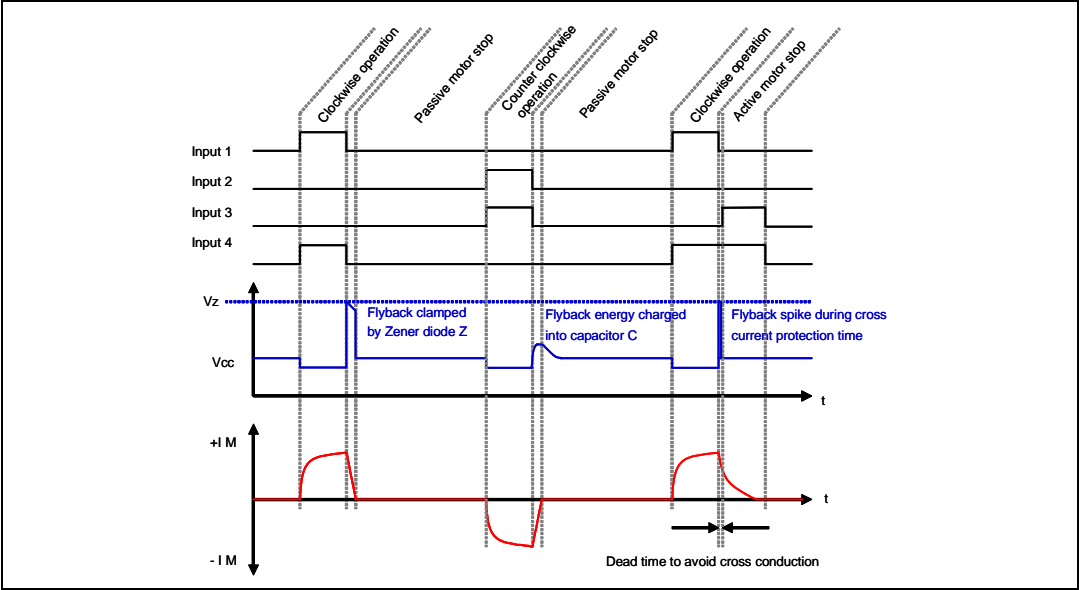
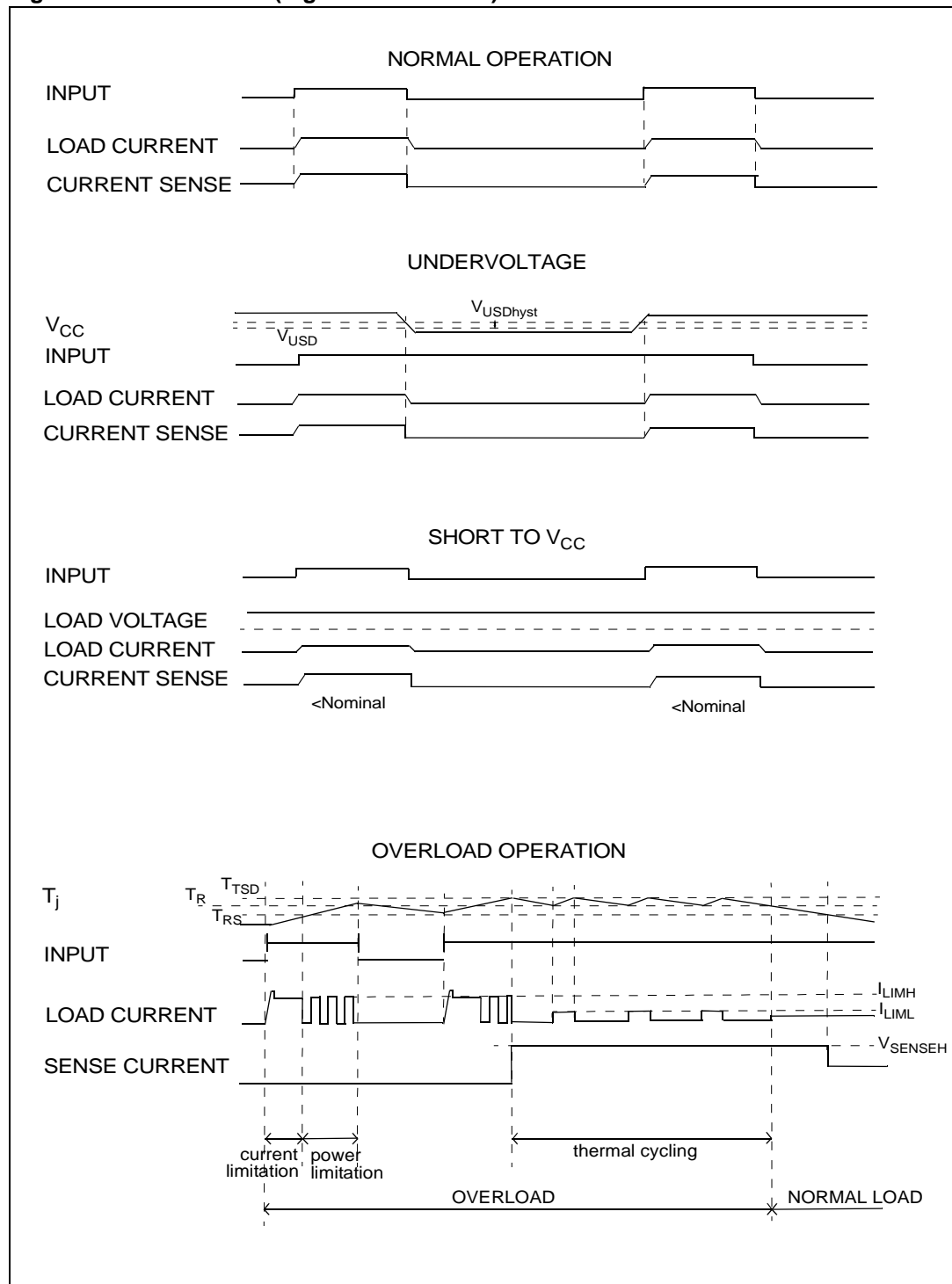
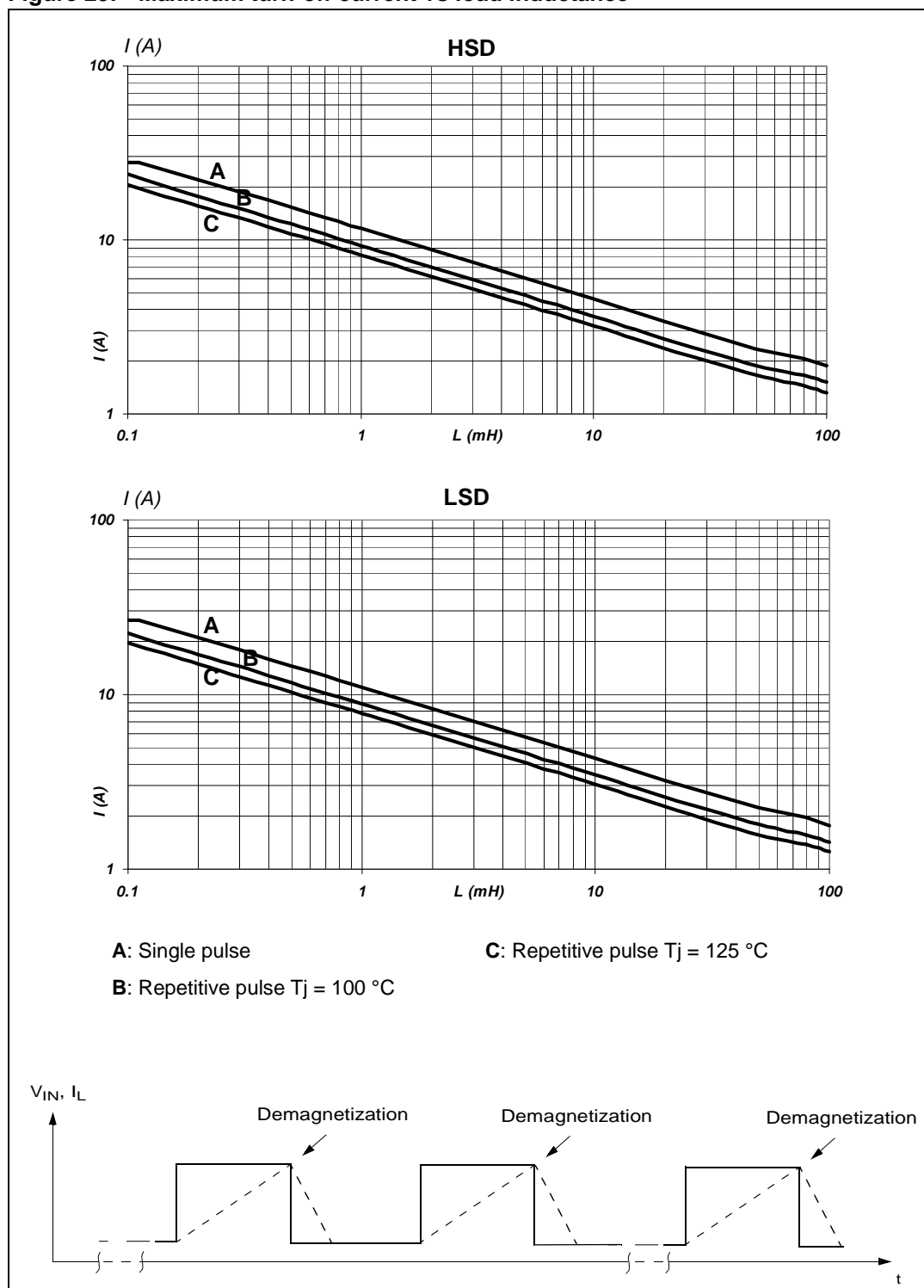


Figure 28. Waveforms (high-side switches)



3.1 Maximum demagnetization energy ($V_{CC} = 13.5\text{ V}$)

Figure 29. Maximum turn-off current vs load inductance⁽¹⁾

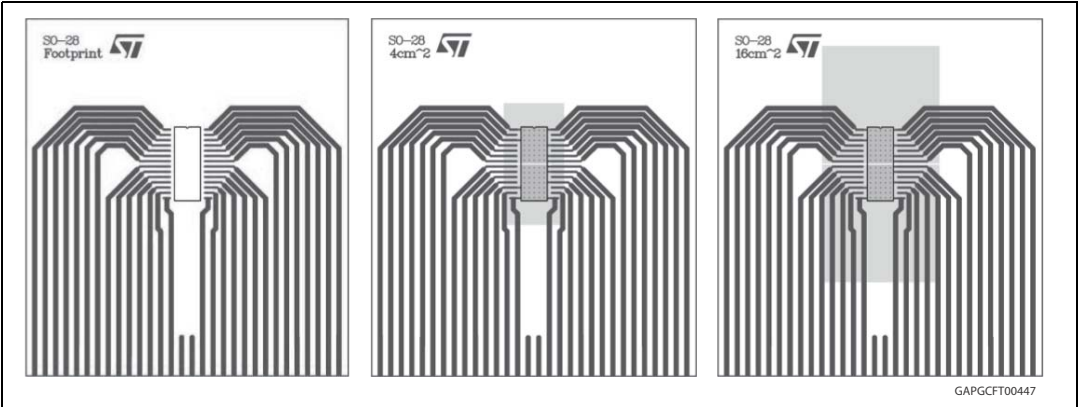


1. Values are generated with $R_L = 0\ \Omega$.
In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

4 Package and PC board thermal data

4.1 SO-28 thermal data

Figure 30. SO-28 PC board⁽¹⁾



1. Layout condition of Rth and Zth measurements (Board finish thickness 1.6 mm +/- 10%; Board double layers; Board dimension 77x86; Board Material FR4; Cu thickness 0.070mm (front and back side); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm).

Figure 31. Chipset configuration

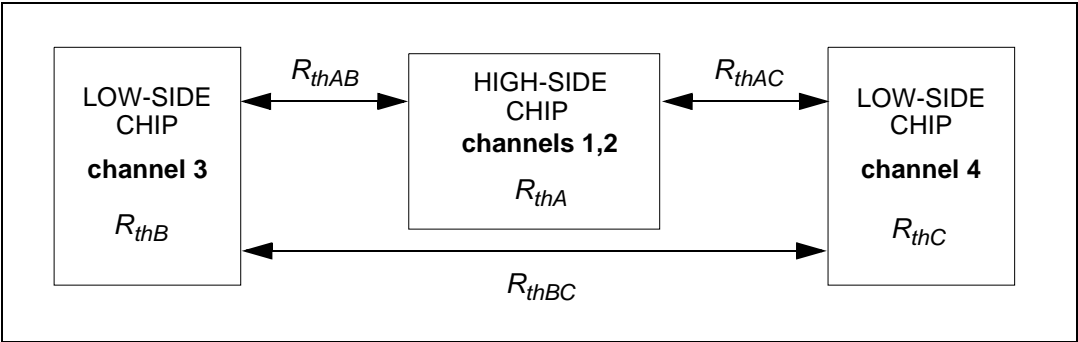
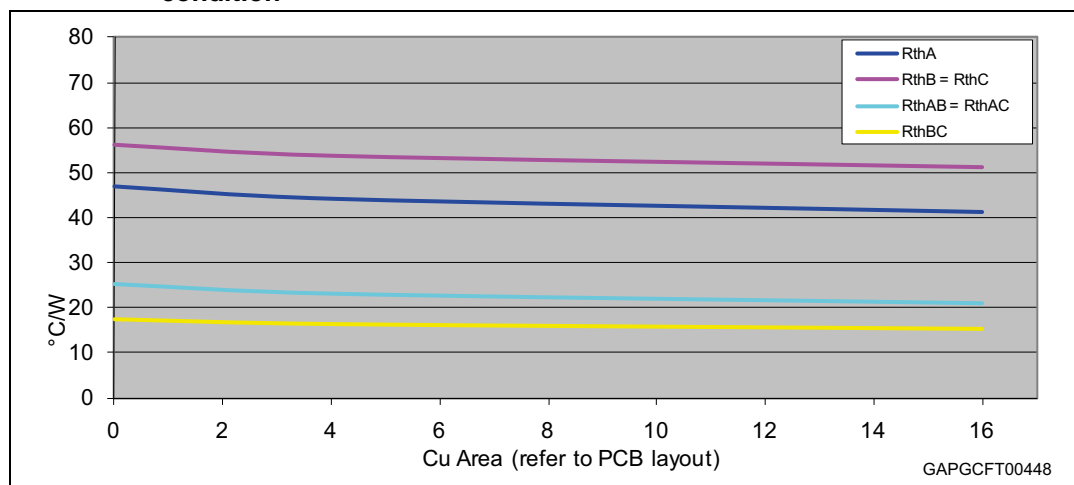


Figure 32. Auto and mutual Rthj-amb vs PCB copper area in open box free air condition⁽¹⁾

1. See [Figure 31](#). For more detailed information see [Table 23](#) and [Table 24](#).

Table 23. Thermal calculations in clockwise and anti-clockwise operation in steady-state mode

HS ₁	HS ₂	LS ₃	LS ₄	T _{jHS12}	T _{jLS3}	T _{jLS4}
On	Off	Off	On	$P_{dHS1} \times R_{thHS} + P_{dLS4} \times R_{thLSLS} + T_{amb}$	$P_{dHS1} \times R_{thHSLS} + P_{dLS4} \times R_{thLSLS} + T_{amb}$	$P_{dHS1} \times R_{thHSLS} + P_{dLS4} \times R_{thLS} + T_{amb}$
Off	On	On	Off	$P_{dHS2} \times R_{thHS} + P_{dLS3} \times R_{thHSLS} + T_{amb}$	$P_{dHS2} \times R_{thHSLS} + P_{dLS3} \times R_{thLS} + T_{amb}$	$P_{dHS2} \times R_{thHSLS} + P_{dLS3} \times R_{thLSLS} + T_{amb}$

Table 24. Thermal resistances definitions⁽¹⁾

$R_{thHS} = R_{thHS1} = R_{thHS2}$	High-side chip thermal resistance junction-to-ambient (HS ₁ or HS ₂ in on-state)
$R_{thLS} = R_{thLS3} = R_{thLS4}$	Low-side chip thermal resistance junction-to-ambient
$R_{thHSLS} = R_{thHS1LS4} = R_{thHS2LS3}$	Mutual thermal resistance junction-to-ambient between high-side and low-side chips
$R_{thLSLS} = R_{thLS3LS4}$	Mutual thermal resistance junction-to-ambient between low-side chips

1. values dependent on PCB heatsink area.

Table 25. Single pulse thermal impedance definitions⁽¹⁾

Z_{thHS}	High-side chip thermal impedance junction-to-ambient
$Z_{thLS} = Z_{thLS3} = Z_{thLS4}$	Low-side chip thermal impedance junction-to-ambient
$Z_{thHSLS} = Z_{thHS12LS3} = Z_{thHS12LS4}$	Mutual thermal impedance junction-to-ambient between high-side and low-side chips
$Z_{thLSLS} = Z_{thLS3LS4}$	Mutual thermal impedance junction-to-ambient between low-side chips

1. values dependent on PCB heatsink area.

Table 26. Thermal calculations in transient mode⁽¹⁾

T_{jHS12}	$Z_{thHS} \times P_{dHS12} + Z_{thHSL} \times (P_{dLS3} + P_{dLS4}) + T_{amb}$
T_{jLS3}	$Z_{thHSL} \times P_{dHS12} + Z_{thLS} \times P_{dLS3} + Z_{thLSL} \times P_{dLS4} + T_{amb}$
T_{jLS4}	$Z_{thHSL} \times P_{dHS12} + Z_{thLSL} \times P_{dLS3} + Z_{thLS} \times P_{dLS4} + T_{amb}$

1. Calculation is valid in any dynamic operating condition. Pd values set by user.

Figure 33. SO-28 HSD thermal impedance junction-ambient single pulse

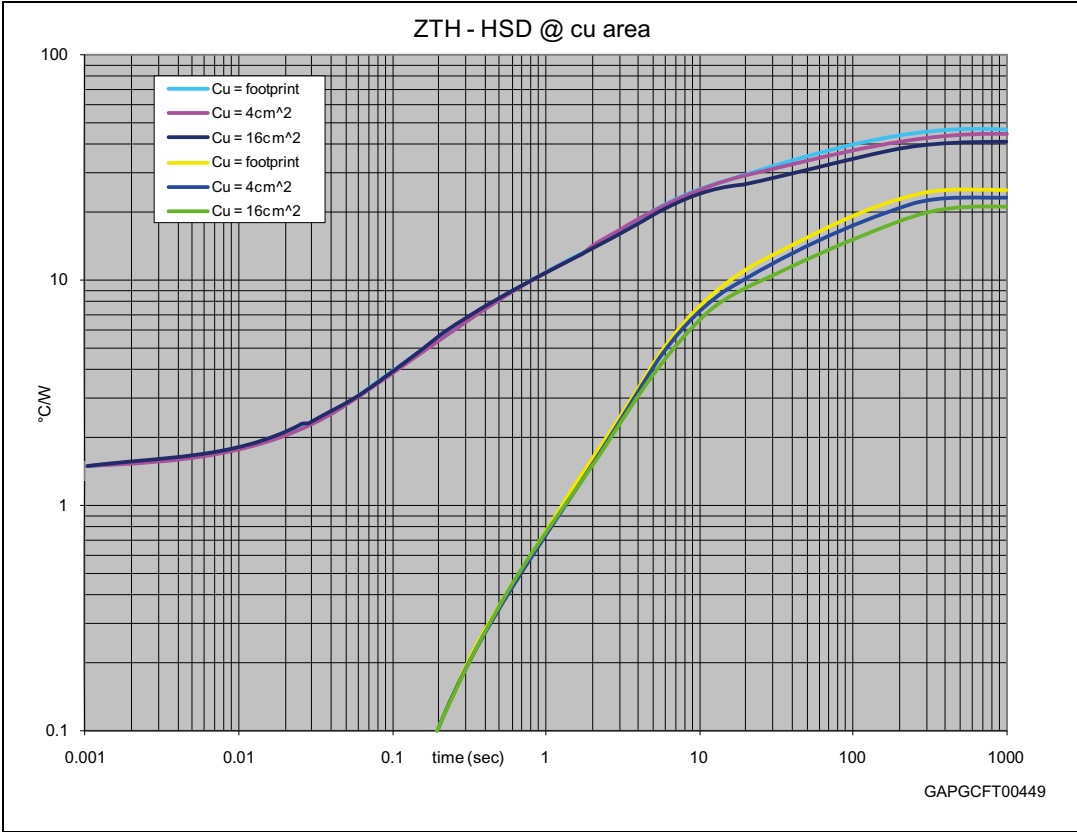
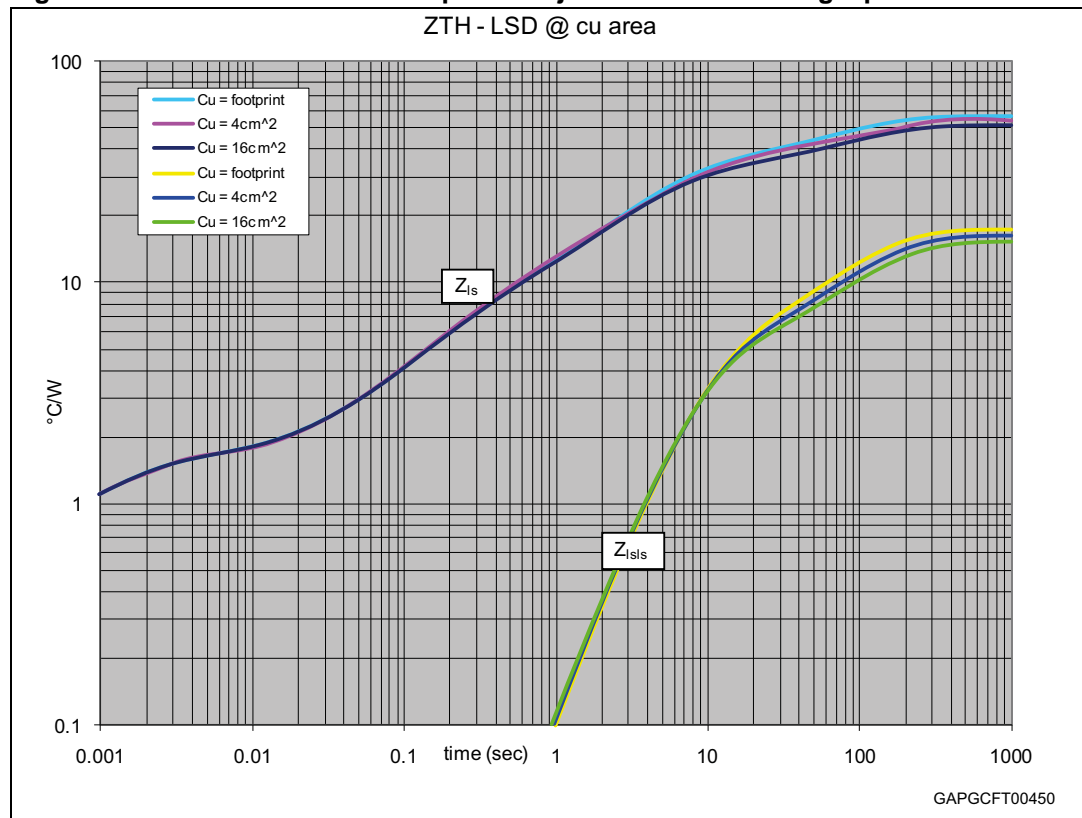
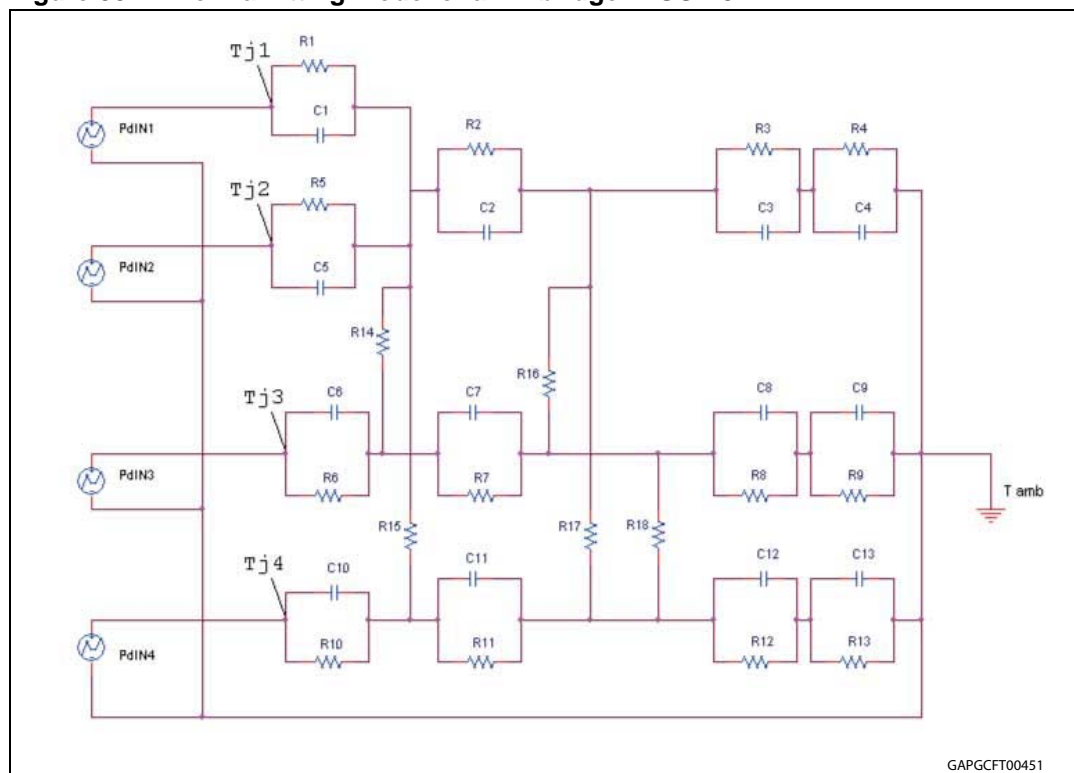


Figure 34. SO-28 LSD thermal impedance junction-ambient single pulse**Equation 1: Pulse Calculation Formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 35. Thermal fitting model of an H-bridge in SO-28

Table 27. Thermal parameters⁽¹⁾

Area/island (cm ²)	FP	4	16
R1 = R5 = R6 = R10 (°C/W)	1.5		
R2 = R7 = R11 (°C/W)	5.5		
R3 (°C/W)	36	34	32
R4 (°C/W)	50	43	36
R8 = R12 (°C/W)	40	38	36
R9 = R13 (°C/W)	54	52	50
R14 = R15 (°C/W)	120		
R16 = R17 (°C/W)	200		
R18 (°C/W)	400	350	300
C1 = C5 (W·s/°C)	0.00025		
C2 = C7 = C11 (W·s/°C)	0.04		
C3 (W·s/°C)	0.2		
C4 (W·s/°C)	2.2	3	4
C6 = C10 (W·s/°C)	0.00075		
C8 = C12 (W·s/°C)	0.15		
C9 = C13 (W·s/°C)	1.6	1.8	2

1. A blank space means that the value is the same as the previous one

5 Package and packing information

5.1 ECOPACK[®] package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

5.2 Package mechanical data

Figure 36. SO-28 package dimensions

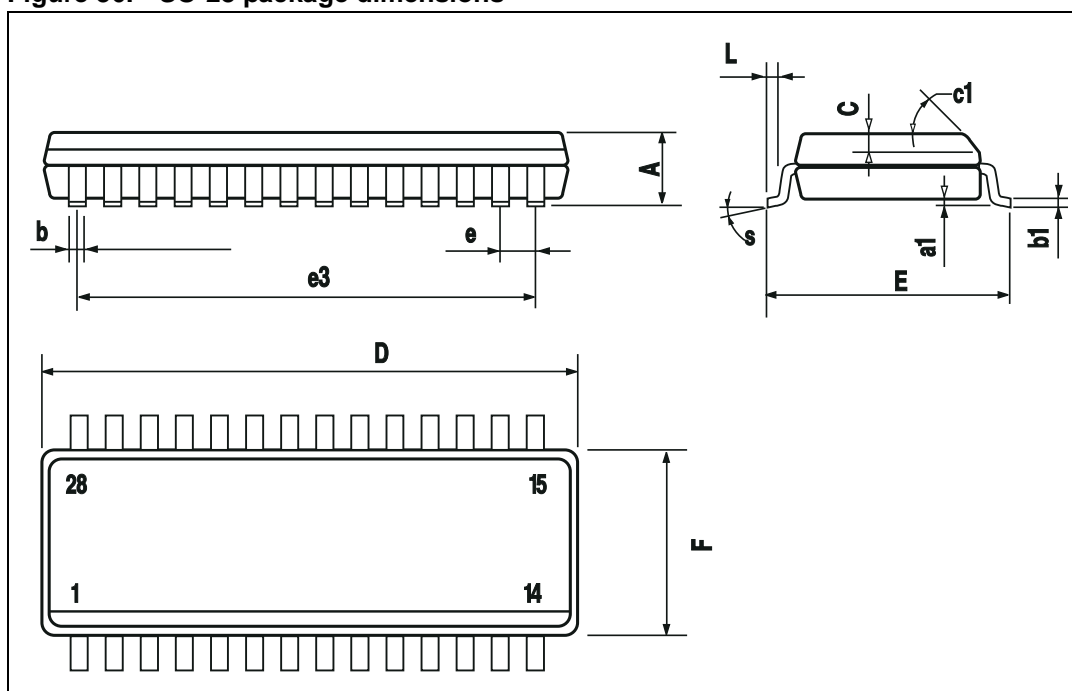


Table 28. SO-28 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.65
a1	0.10		0.30
b	0.35		0.49
b1	0.23		0.32
C		0.50	
c1	45° (typ.)		
D	17.7		18.1
E	10.00		10.65
e		1.27	
e3		16.51	
F	7.40		7.60
L	0.40		1.27
S	8° (max.)		

5.3 Packing information

Figure 37. SO-28 tube shipment (no suffix)

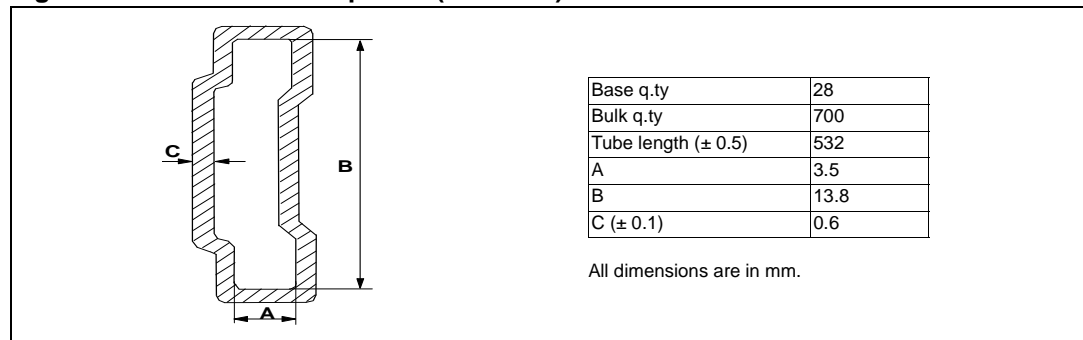
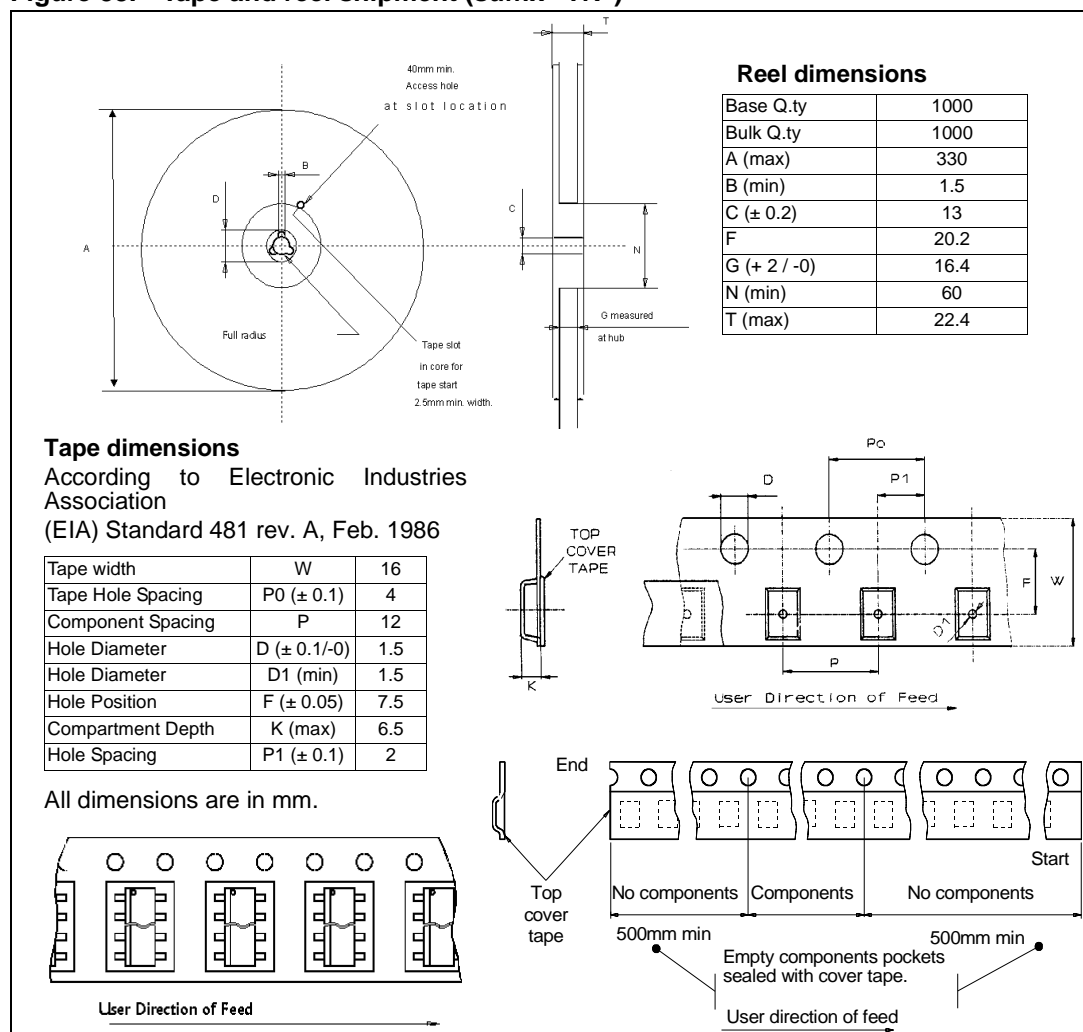


Figure 38. Tape and reel shipment (suffix “TR”)



6 Revision history

Table 29. Document revision history

Date	Revision	Changes
30-Jul-2009	1	Initial release.
10-Sep-2009	2	Updated following figures: – Figure 29: Maximum turn-off current vs load inductance⁽¹⁾ – Figure 32: Auto and mutual Rthj-amb vs PCB copper area in open box free air condition⁽¹⁾ – Figure 33: SO-28 HSD thermal impedance junction-ambient single pulse – Figure 34: SO-28 LSD thermal impedance junction-ambient single pulse Updated Table 27: Thermal parameters .
14-Jan-2010	3	Updated Figure 26: Typical application schematic .
13-Jul-2011	4	Updated Features list Updated Figure 35: Thermal fitting model of an H-bridge in SO-28 Updated Table 27: Thermal parameters
02-Nov-2011	5	Table 17: Switching ($T_j = 25^\circ\text{C}$, unless otherwise specified): – Changed $(dV_{OUT}/dt)_{on}$ to t_r – Changed $(dV_{OUT}/dt)_{off}$ to t_f Added following tables: – Table 12: Electrical transient requirements (part 1/3) – Table 13: Electrical transient requirements (part 2/3) – Table 14: Electrical transient requirements (part 3/3)
19-Sep-2013	6	Updated Disclaimer.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com