CS303 – Logic & Digital System Design CS303 – Term Project

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1. Project Description

Designing a sequential circuitry for a simple telephone conversation and implementing it using Verilog HDL. In Particular, the caller will start the telephone conversation, and will be sending characters to callee (or vise versa). As an output, circuitry will reveal sent characters, and calculated conversation cost sent to each other.

Design:

The state diagram on the following page includes all specific information and states used throughout the circuitry.
Overall, there are 6 states, such as: “Idle”, “Ring”, “Rjct”, “Caller”, “Callee”, “Finn”.
Note: whenever the “rst” button is pressed, circuitry goes to the “Idle” state.

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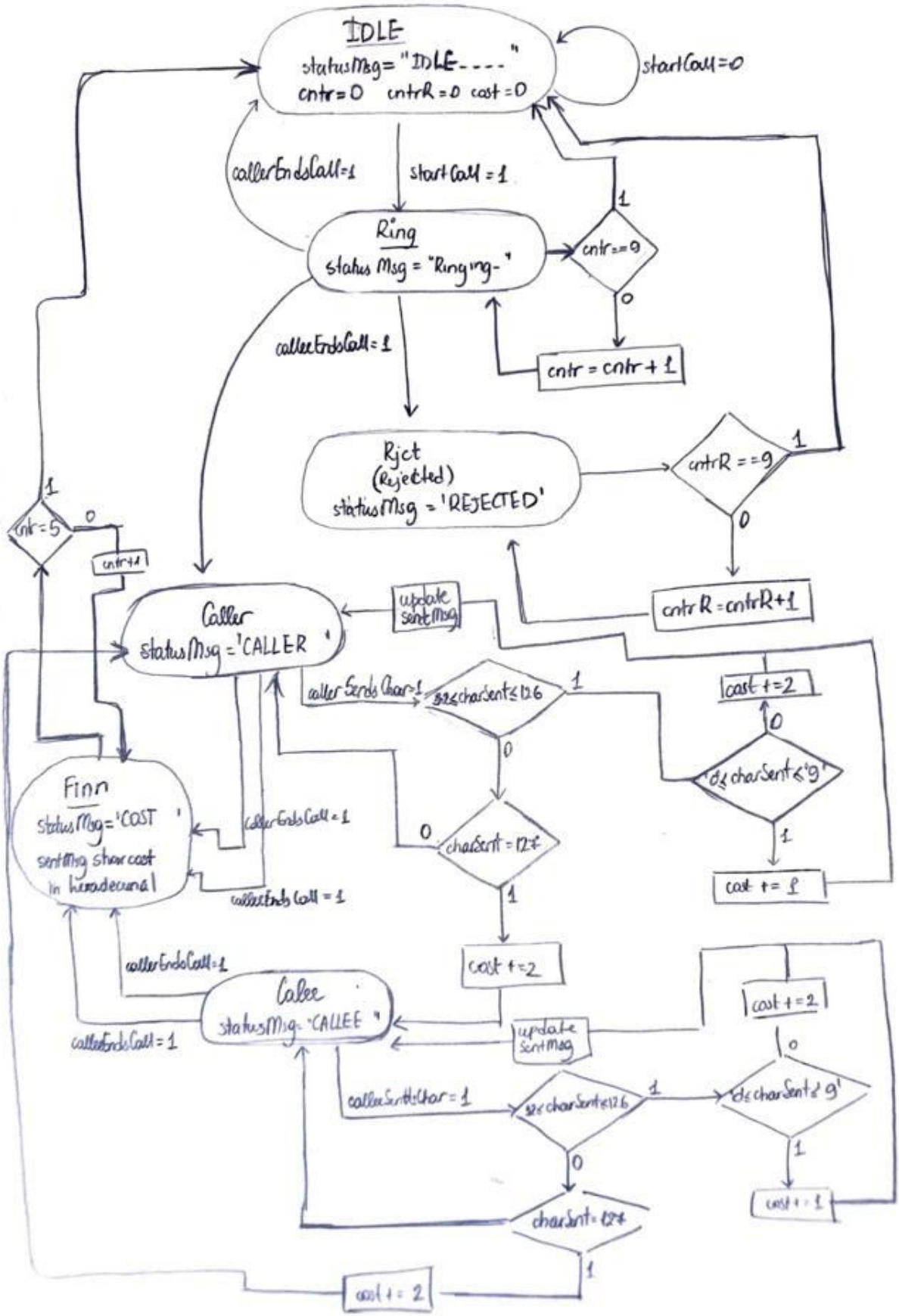
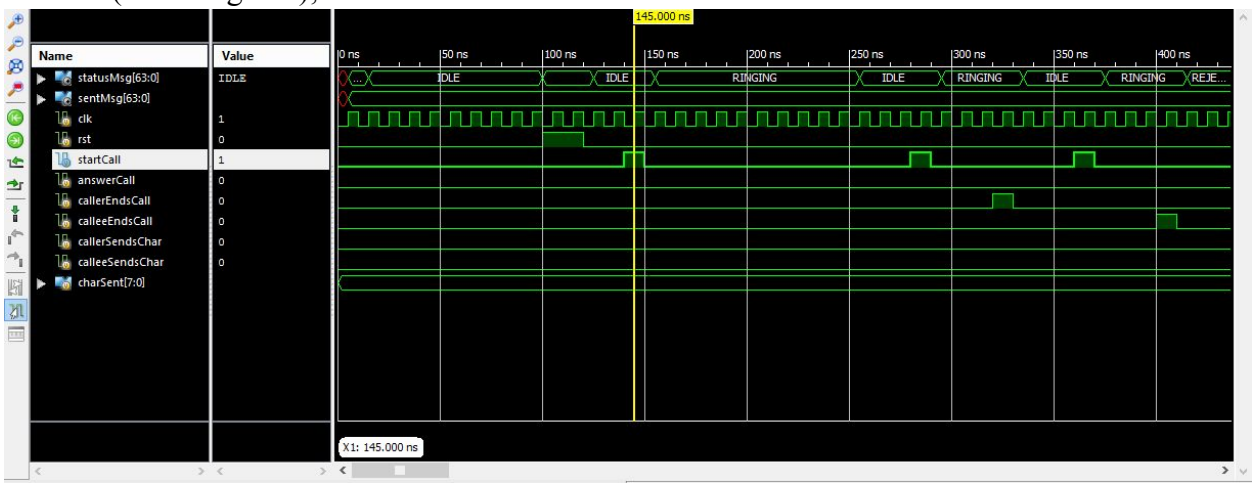
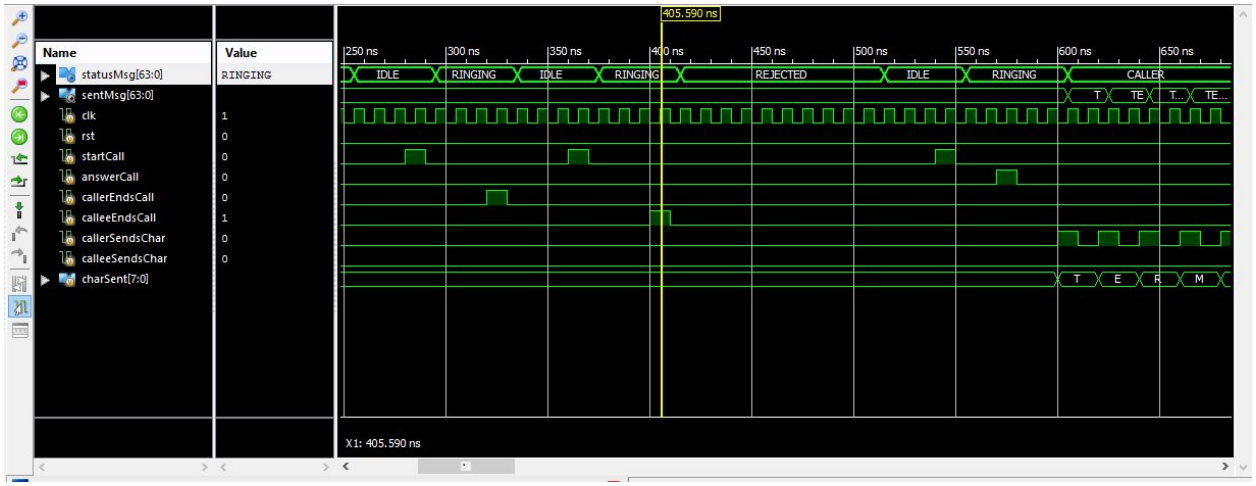


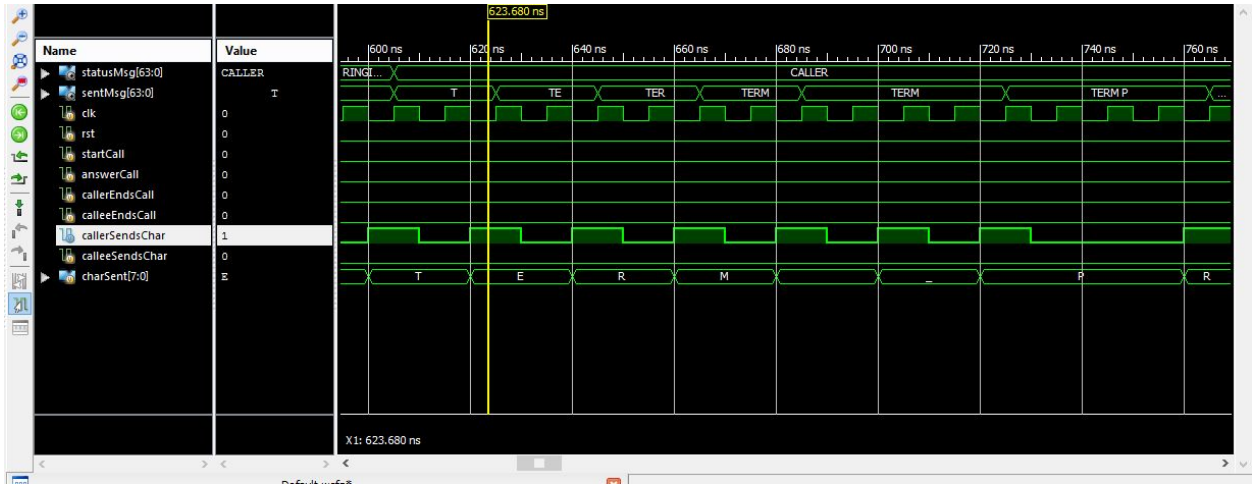
2. Simulation Results

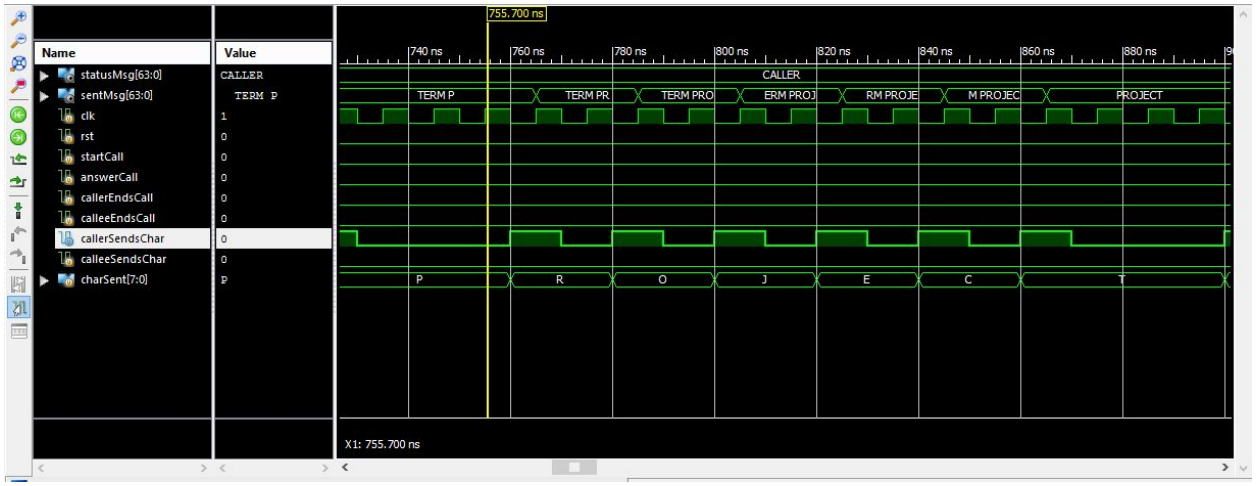
The testbench provided on SuCourse:

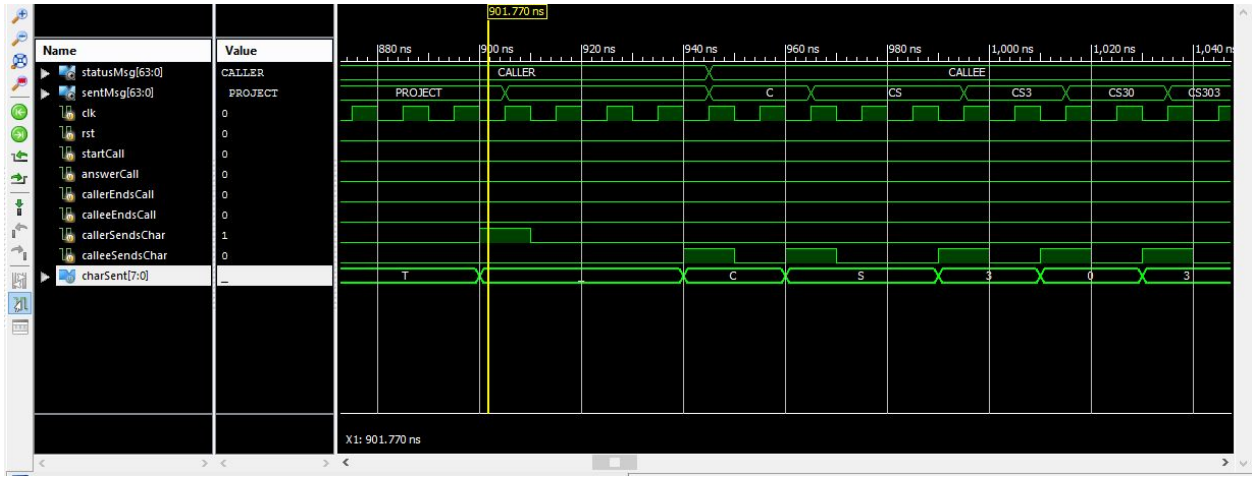
Cost is calculated for characters where for each number cost=+1, the rest valid characters cost=+2 (including 127);

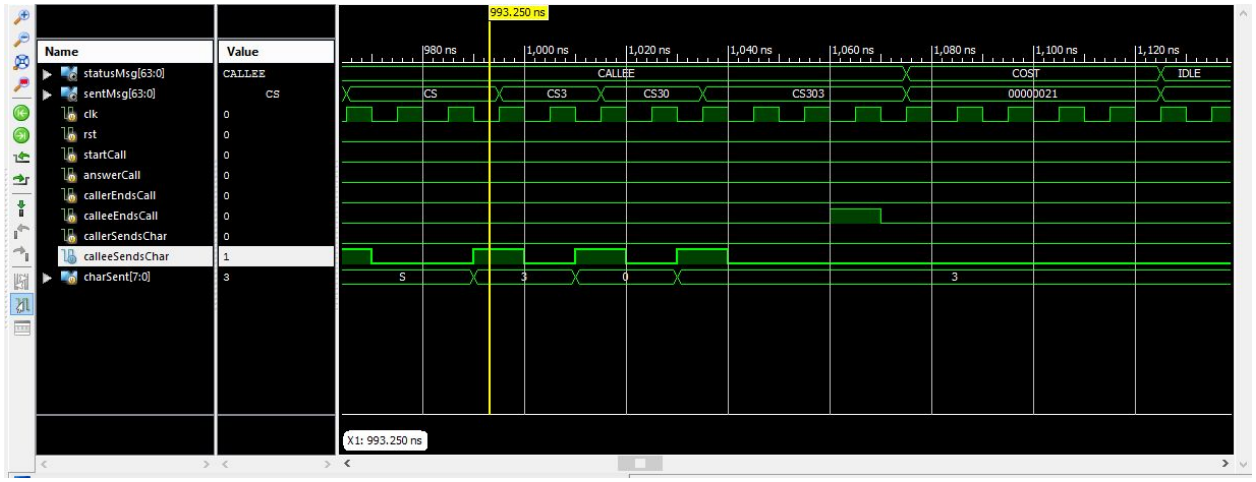







755.700 ns
Name
Value
statusMsg[63:0]
sentMsg[63:0]
clk
rst
startCall
answerCall
callerEndsCall
calleeEndsCall
callerSendsChar
calleeSendsChar
charSent[7:0]
CALLER
TERM P
1
0
0
0
0
0
0
P
740 ns
760 ns
780 ns
800 ns
820 ns
840 ns
860 ns
880 ns
CALLER
TERM P
TERM PR
TERM PRO
ERM PROJ
RM PROJE
M PROJEC
PROJECT
P
R
O
J
E
C
T
X1: 755.700 ns


901.770 ns
Name
Value
statusMsg[63:0]
sentMsg[63:0]
clk
rst
startCall
answerCall
callerEndsCall
calleeEndsCall
callerSendsChar
calleeSendsChar
charSent[7:0]
CALLER
PROJECT
0
0
0
0
0
0
1
0
_
880 ns
900 ns
920 ns
940 ns
960 ns
980 ns
1,000 ns
1,020 ns
1,040 ns
CALLER
CALLEE
PROJECT
C
CS
CS3
CS30
CS303
T
C
S
3
0
3
X1: 901.770 ns


993.250 ns
Name
Value
statusMsg[63:0]
sentMsg[63:0]
clk
rst
startCall
answerCall
callerEndsCall
calleeEndsCall
callerSendsChar
calleeSendsChar
charSent[7:0]
CALLEE
CS
0
0
0
0
0
0
0
1
3
980 ns
1,000 ns
1,020 ns
1,040 ns
1,060 ns
1,080 ns
1,100 ns
1,120 ns
CALLEE
COST
IDLE
CS
CS3
CS30
CS303
00000021
S
3
0
3
X1: 993.250 ns

3. Synthesis Results

The screenshots of **timing** and **space** details are given below:

```
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s100etq144-4

 Number of Slices:                      178  out of    960    18%
 Number of Slice Flip Flops:            131  out of   1920     6%
 Number of 4 input LUTs:                342  out of   1920    17%
 Number of IOs:                         144
 Number of bonded IOBs:                 144  out of    108   133% (*)
 Number of GCLKs:                         1  out of     24     4%

WARNING:Xst:1336 -  (*) More than 100% of Device resources are used
```

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 7.185ns (Maximum Frequency: 139.170MHz)
   Minimum input arrival time before clock: 12.002ns
   Maximum output required time after clock: 4.571ns
   Maximum combinational path delay: No path found

Timing Detail:
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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 7.185ns (frequency: 139.170MHz)
  Total number of paths / destination ports: 2074 / 131
-------------------------------------------------------------------------
Delay:               7.185ns (Levels of Logic = 4)
  Source:            cState_FSM_FFd2 (FF)
  Destination:       sentMsg_61 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: cState_FSM_FFd2 to sentMsg_61
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
```