Record PMOS WSe_2 GAA Performance using Contact Planarization, and Systematic Exploration of Manufacturable, High-yield Contacts

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Abstract

Two-dimensional (2D) transition metal dichalcogenides (TMDs) hold significant promise for both front-end-of-line (FEOL) and back-end-of-line (BEOL) applications. Here, we report new approaches to contact formation in global back gate 2D PMOS transistors using a manufacturable physical vapor deposition (PVD) sputtering process. We present a systematic study of novel sputtered contacts (Sb/Pt, Sb_2Te_3, Bi_2Te_3) to multilayer WSe_2 and through statistical analysis we discover trends of increasing performance with Pt thickness and post-metal anneal. Optimized conditions give R_C down to 1.3 kΩ.µm at N(inv)=1e13cm^{-2} and $I_{d,max}$ = 212 µA/µm at V_d =-1V, the highest performance to date using sputtered contacts. Further, we pioneer a new approach to contact-first gate-all-around (GAA) schemes through contact planarization using chemical mechanical polishing (CMP). This first-of-kind CMP flow demonstrates significant performance gains over non-CMP contacts (4×). CMP Ru contacts to monolayer WSe_2 GAA devices achieve record drive currents > 600 µA/µm and SS = 132 mV/dec.

Keywords: 2D FET, TMD, WSe_2, CMP, GAA

Introduction

Contact resistance to 2D FETs, specifically PMOS, remains one of the greatest challenges to the implementation of 2D materials in future technologies [1-3]. The most commonly used technique for contact formation, electron beam evaporation, is unscalable, necessitating the investigation of alternative techniques such as atomic layer deposition [4] or sputtering (**Fig.1a**). In this work, we utilize sputtering to form contacts with high yield to multilayer global back-gated WSe_2 devices, an applicable strategy for both FEOL and BEOL applications with potentially raised S/D topologies. We also extend our contact investigation to a new planarization scheme using CMP for GAA devices and find significant performance enhancement over evaporated contacts.

Sputtered Contacts to Multilayer WSe_2

Global back-gated devices with room-temperature sputtered contacts are fabricated using a S/D-last process flow (**Fig.1b**) starting from MOCVD-grown multilayer (1-6L) WSe_2 (**Fig.1c**). A bilayer resist stack is used for S/D sputtered contact liftoff, resulting in a channel length bias ~190 nm due to deposition occurring during sputtering in the undercut regions as shown in **Fig.2a**. We first investigate sputtered Pt contacts using Sb as an interlayer to reduce damage during contact formation [5]. **Fig.2b** shows I_d-V_g curves across various L_{ch} for 3nm Sb/10nm Pt-contacted devices. We observe excellent yields (100%) at all L_{ch} except the shortest drawn channels due to shorting issues during S/D develop. TEM cross sections (**Fig.3a-b**) show that damage to the TMD remains low, extending at most to the top layer. We also observe that Sb and Pt signals appear mixed after annealing at 180°C/10min (**Fig.3c**), indicating the possible migration of Sb during annealing allowing Pt to reach the interface with WSe_2.

We next investigate the impact of increasing Pt thickness and observe a clear trend of increasing on-state current (**Fig.4a**). To account for V_t shifting, we compare I_d at a fixed overdrive ($I_{d,FOV}$) of 50V (**Fig.4b**) based on constant-current V_t at 1 nA/µm (**Fig.4c**). Median $I_{d,FOV}$ values increase by 7× from 3nm to 10nm Pt, reflecting an improvement in the contact resistance with thicker Pt.

We find that performance can be improved through annealing on a hot plate at 180°C/10min (**Fig.5a**), although further annealing to 250°C only provides a slight positive V_t shift indicating potential signs of oxidation of the exposed channel. Control samples fabricated with Pt-only sputtered contacts show lower $I_{d,max}$ across all L_{ch} (**Fig.5b**), demonstrating the necessity of the Sb interlayer. I_d-V_g curves of 3nm Sb/10nm Pt-contacted devices after anneal are shown in **Fig.6a** and the best performing device with L_{ch}=60nm is shown in **Fig.6b-c**, achieving $I_{d,max}$=212µA/µm at V_d=-1V, the highest value to date with industry-compatible sputtered contacts. Pseudo-transfer length method (TLM) extractions using the best 10% of devices (**Fig.7a**) indicate a significant reduction in R_C after 180°C annealing down to 1.3 kΩµm at N(inv)=1e13cm^{-2}. We show the SS_{sat} of devices (extracted in the high-current range 100pA/µm-1µA/µm and normalized to the median SS_{sat} before annealing) at each annealing stage (**Fig.7b**) and find a 30% reduction after 180°C annealing, indicating a reduced Schottky barrier after annealing.

One of the benefits of sputtering is the wide range of materials which can be accessed. We demonstrate two such novel materials (Sb_2Te_3 and Bi_2Te_3 [6]) in **Fig.8**, and observe similar trends with increasing Pt thickness and 180°C annealing as with Sb/Pt contacts, with median $I_{d,max}$ up to ~30-50µA/µm after annealing. **Fig.9a** shows TLM extractions using the best 10% of devices for Sb_2Te_3 and Bi_2Te_3 contacts, demonstrating similar R_C values. **Fig.9b** benchmarks the best sputtered contact combinations in this work for R_C and mobility, where we note consistent mobility extractions across all contact combinations.

Record GAA Performance with CMP Contact Flow

We next demonstrate 2D PMOS contact improvements to GAA monolayer WSe_2 transistors through a new integration flow utilizing planarized contacts (**Fig.10**). The use of CMP on PVD Ru gives a better controlled interface after TMD transfer compared to with unpolished, evaporated contacts [3]. This results in substantially improved GAA device performance (**Fig.11a**), with record drive currents of 613 µA/µm and SS = 132 mV/dec at L_{sd} = 20 nm. Comparing to previously reported results, CMP contacts display a 4× improvement in drive current and steeper subthreshold slopes over a larger current range (**Fig.11b-c**), pointing to a lower contact resistance for this integration scheme. We benchmark these GAA results in **Fig.12**, showing the best reported GAA PMOS performance to date.

Summary

This work presents two promising approaches to contact formation for 2D PMOS transistors. Sputtering offers a robust path to investigate a wide range of contact materials, while planarized contacts using CMP provide a controlled contact interface contributing to significantly improved GAA performance. Together, these results provide avenues for new device topologies in the BEOL with low-temperature post-metal annealing, and reduced contact resistance in FEOL.

References

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a) TABLE I. Comparison of different contact formation techniques

	Evaporation	ALD	Sputter
Conformality	Poor	Good	OK
300mm compatibility	Poor	Good	Good
1L compatibility	Good	OK	OK
Performance (R_C)	Good	Poor	?

b)
- Substrate: Si/100 nm SiO_2/WSe_2
- Probe pad patterning + liftoff
- RIE/ICP isolation etch (Cl_2/O_2/SF_6)
- S/D patterning + liftoff
- Sputtered contact + 30 nm evap. Au
- (Optional) PMMA coat, hot plate anneal, PMMA strip

(c)

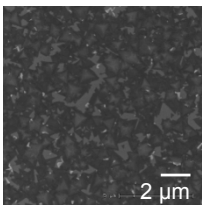


Fig. 1: (a) Comparison of different techniques for forming contacts to TMDs. (b) Process flow for back-gated multilayer WSe_2 transistors with sputtered contacts. (c) Top-down SEM image of starting multilayer WSe_2 growth

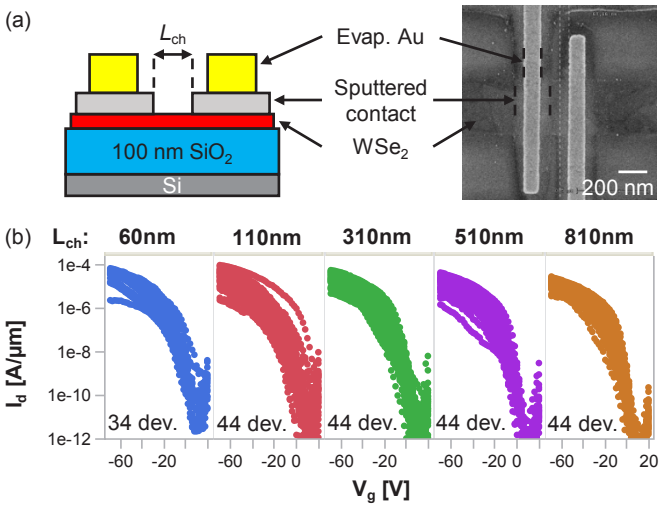


Fig. 2: (a) BEOL-compatible device schematic and SEM image of a back-gated multilayer WSe_2 transistor with L_{ch} = 60 nm (b) I_d-V_g curves of multiple devices across various L_{ch} for sputtered 3nm Sb/10nm Pt-contacted devices at V_d=-1V before annealing. Devices show excellent yields up to 100%.

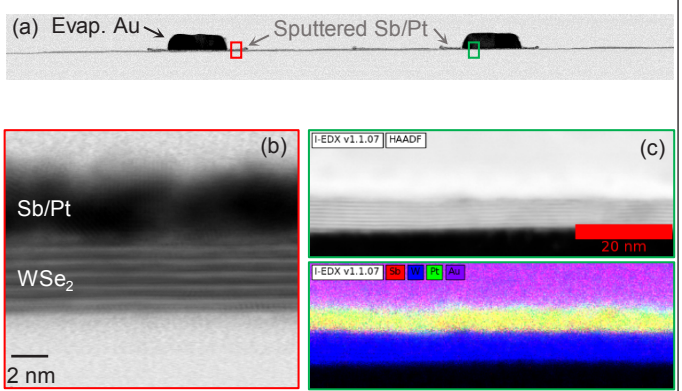


Fig. 3: (a) TEM cross section of a back-gated multilayer WSe_2 transistor with 3 nm Sb/3 nm Pt sputtered contacts + 30 nm evap. Au, with red and green boxes showing regions which indicate (b) low damage caused by sputtering and (c) mixing of Sb and Pt layers after annealing at 180 °C/10 minutes

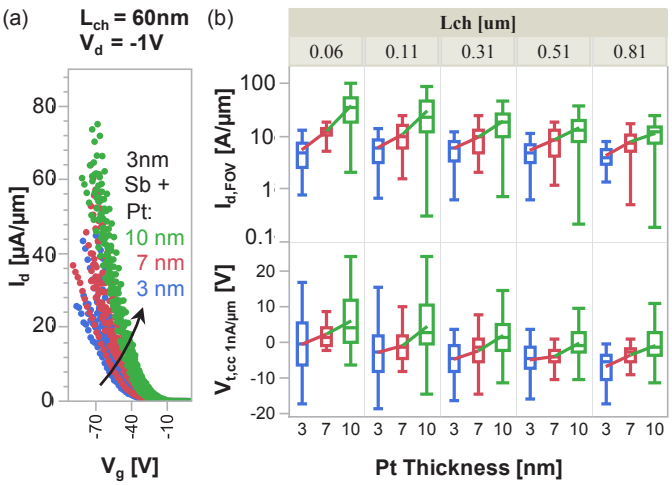


Fig. 4: (a) I_d-V_g curves for L_{ch} = 60 nm, (b) I_d at a fixed overdrive ($V_{tcc,1nA/μm}$ +50V) and $V_{t,cc}$ at 1 nA/μm of sputtered 3 nm Sb/Pt-contacted devices with various L_{ch} at V_d=-1V with increasing Pt thickness from 3–10 nm. Each box represents ~30-40 devices. Thicker Pt improves drive currents up to 7×.

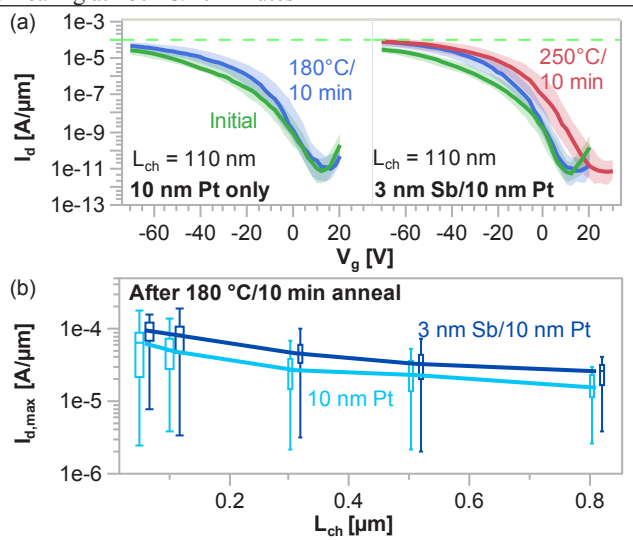


Fig. 5: (a) I_d-V_g for L_{ch} = 110nm and (b) $I_{d,max}$ vs. L_{ch} of Pt-only and Sb/Pt-contacted devices at V_d=-1V after various stages of annealing. Each box represents ~30-40 devices. $I_{d,max}$ of Sb/Pt devices improves by 1.5-2× after 180°C anneal and outperform control Pt-only devices.

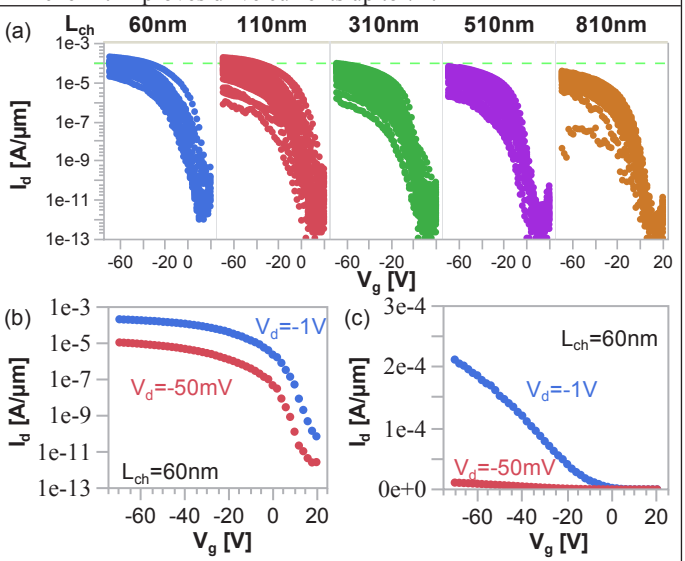


Fig. 6: I_d-V_g for multiple 3nm Sb/10nm Pt-contacted devices at V_d=-1V after 180°C/10min annealing. Highest performing device with L_{ch}=60nm showing $I_{d,max}$ = 212 μA/μm in (b) log and (c) linear scale.

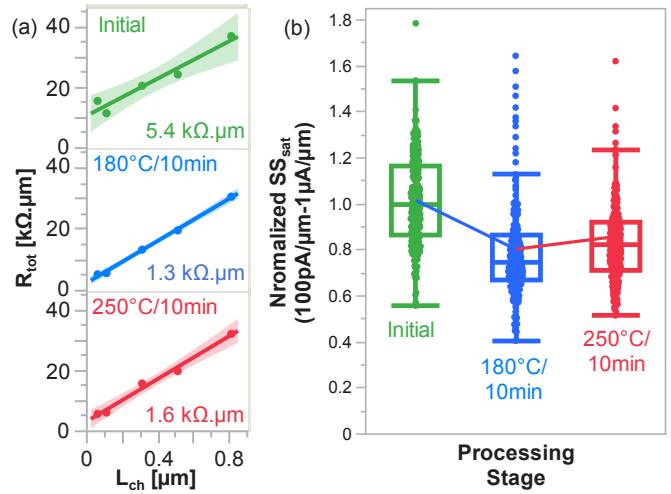


Fig. 7: (a) R_{tot} vs L_{ch} (10th percentile) extracted at V_d=-50mV, N(inv)=1e13 cm^{-2} and (b) SS_{sat} in the 100pA/μm-1μA/μm range normalized to the initial median value for 3nm Sb/10nm Pt-contacted devices after various annealing conditions. SS_{sat} reduces by 25% after 180°C anneal, corroborating reduced R_C down to 1.3 kΩμm.

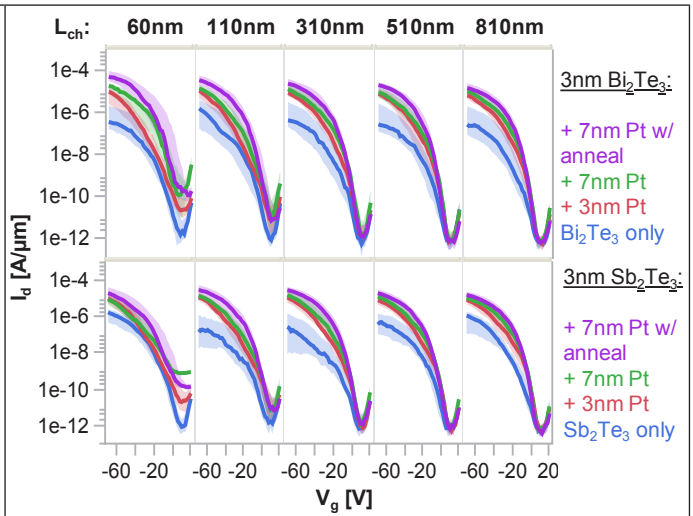
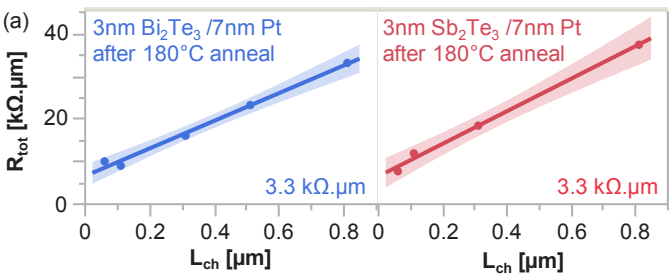


Fig. 8: Median I_d-V_g curves across various L_{ch} at V_d = -1V for sputtered Bi_2Te_3 (top row) and Sb_2Te_3 (bottom row) contact combinations. Each curve represents ~30-40 devices. Similar trends of improved $I_{d,max}$ with increasing Pt thickness, and reduced SS_{sat} after 180°C anneal, are observed for both telluride contacts.



(b) TABLE II. Sputtered contact performance summary

	$R_{C,initial}$	$\mu_{initial}$	$R_{C,180C}$	μ_{180C}
3/10nm Sb/Pt	6.2 ± 1.1	22.3±2.9	1.3 ± 0.4	18.2± 0.5
3/7nm Bi_2Te_3/Pt	12.5 ± 1.8	15.7±2.4	3.3 ± 0.4	19.2±1.1
3/7nm Sb_2Te_3/Pt	12.3 ± 0.8	18±1.5	3.3 ± 0.4	16.3±0.8

Fig. 9: (a) R_{tot} vs L_{ch} (10th percentile) extracted at V_d=-50mV, N(inv)=1e13 cm^{-2} for Bi_2Te_3 and Sb_2Te_3 contacts (b) Summary of R_C (kΩ.μm) and μ (cm^2/Vs) for best-performing sputtered contact combinations before and after 180 °C annealing. All samples show ~4× reduction in R_C after 180 °C annealing, and similar mobilities.

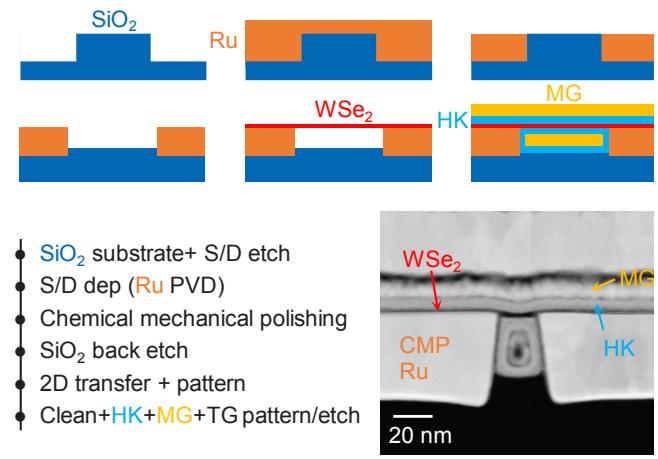


Fig. 10: Device schematics + process flow for GAA 2D FETs using chemical mechanical polishing of PVD Ru S/D contacts, and gate TEM cut of monolayer WSe_2 GAA transistor using CMP Ru contacts with L_{sd} = 20 nm. CMP Ru offers different crystallinity, grain size, thermal stability and topography compared to previous evaporated contacts, providing a more controlled interface to the TMD.

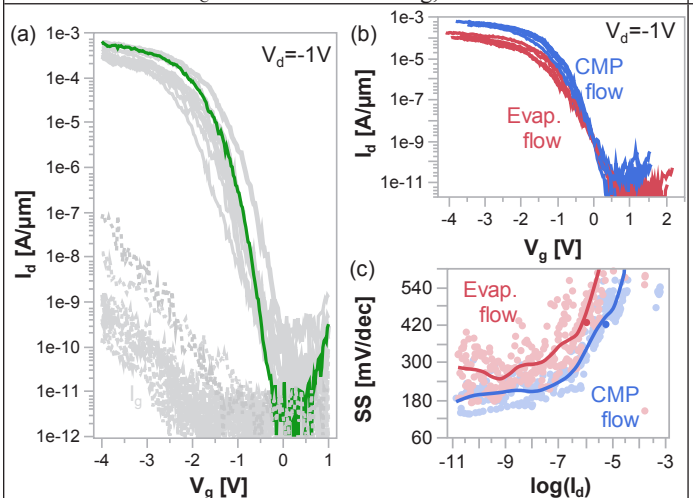


Fig. 11: (a) Multiple I_d-V_g for L_{sd} ranging from 20nm to 80nm, with record SS=132mV/dec and $I_{d,max}$=613μA/μm highlighted in green. (b) I_d-V_g and (c) SS vs. log(I_d) comparison of GAA PMOS using CMP Ru to evap. Ru contacts for multiple devices. CMP contacts show lower SS over a wider current range than evap. contacts.

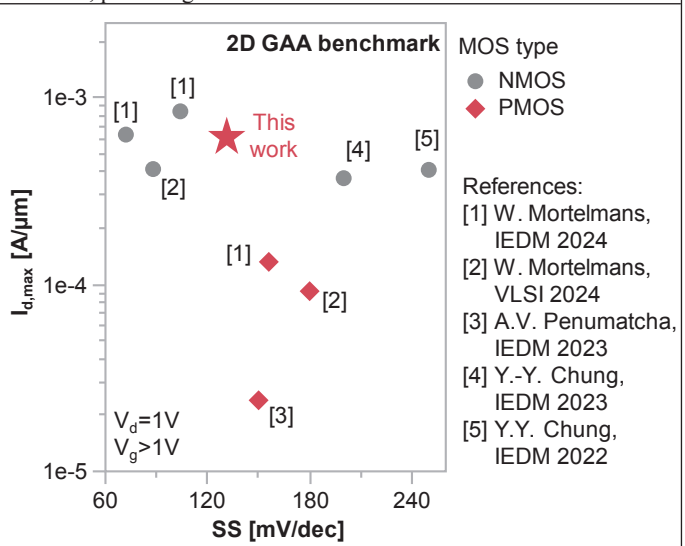


Fig. 12: $I_{d,max}$ vs SS benchmark of GAA 2D CMOS at $|V_d|$ =1V. This work reports record monolayer GAA WSe_2 performance with L_{sd} = 20 nm, SS_{lin} = 132 mV/dec and $I_{d,max}$=613 μA/μm.