Intel 18A Platform Technology Featuring RibbonFET (GAA) and PowerVia for Advanced High-Performance Computing

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Abstract

An advanced Intel 18A technology featuring RibbonFET and PowerVia provides over 30% density scaling and a full node of performance improvement compared to Intel 3. Intel 18A achieved 18%/25% performance (0.75V/1.1V) at iso-power over Intel 3 through an industry-first combination and optimization of advanced interconnects, a Gate-All-Around (GAA) transistor architecture, backside power, and design co-optimization. Intel 18A offers high-performance (HP) and high-density (HD) libraries with full-featured technology design capabilities and enhanced design ease of use.

Introduction

Continued scaling of transistor dimensions as well as the limitations of the FinFET architecture has driven the move to GAA transistors. Backside power provides performance and density scaling in addition to reducing the need to scale interconnect pitch which reduces the cost of frontside metals.

Intel 18A consists of a HP 180nm cell height (180CH) library and an HD 160nm cell height (160CH) library targeted for lower power applications (Fig. 1). Full routed block level studies on an industry standard 180CH logic block demonstrates 18%/25% performance (0.75V/1.1V) improvement at iso-power with 0.72x area scaling (Fig. 2) vs Intel 3 [1]. Performance improvements are achieved by the combination and optimization of three key vectors: transistor, interconnect and backside power. RibbonFET transistors provide higher transistor drives, improved gate control and leakage, lower capacitance, and improved transistor optimization through ribbon width options. Backside power significantly reduces power droop (Fig 2c) and the need for signal interconnect scaling by eliminating the power grid on front side metal layers improving interconnect performance, routing efficiency including 8-10% density improvement through higher utilization (Fig.2b) [2] and design ease of use as seen in Fig 3 [3]. Intel 18A uses fewer signal routing metal layers vs Intel 3 and avoids expensive pitch scaling due to backside power and it is fully compatible with Foveros and EMIB advanced packaging processes for optimized product disaggregation strategies [4].

Technology features

Intel 18A introduces Intel's first RibbonFET transistor (Fig. 4a-b) optimized for high frequency applications and integrated with PowerVia (Fig 4b) for low resistance backside connectivity. The table in Fig. 4 shows key technology features including scaled SRAM bitcells and a range of metal stacks for frontside and backside available for application optimization.

Transistor characteristics are shown in Fig. 5 demonstrating excellent DIBL and subthreshold slope. The transistor contacts and PowerVia integration is optimized to reduce both contact resistance and device capacitance. The transistor supports 8 logic VTs [4NVT+4PVT] spanning a 180mV range attained through integration of N & P dipole work-functions which were required given the space constraint of RibbonFETs.

A typical high performance metal stack is shown in Fig. 6 showing both front side signal interconnects as well as the back side power interconnects with standardized pitches to allow for flexible metal count. The high density MIM [5] is located on the backside between BM4 and BM5. Intel 18A front side metals demonstrate ~12% intrinsic RC improvement and 25%-50% reduced via resistance across the frontside metals vs Intel 3 using advanced metallization and ultra-low k dielectrics (Fig. 7). Carrier wafer bond layers are optimized for thermal conductivity and backside metals are optimized for power droop minimization and thermomechanical strength.

Backside power eliminates the front-side power grid. That along with EUV direct print patterning reduces total mask count and process complexity of the frontside metals. Delivering single pass EUV patterns at M0-M2 pitches was enabled by low-n absorber EUV reticles using dimensional modification. The resulting M0-M2 process simplification offsets the cost of additional mature, low-cost backside metal layers (Fig. 8) and greatly improves design ease of use (Fig. 3).

Reliability and Thermals

Intel 18A wafer level reliability meets industry standard Level 1 certification goals. Fig. 9 shows intrinsic SRAM Vmin aging with defect screening at a stress equivalent to 1000h HTOL meeting SRAM Vmin aging goals with margin. PowerVia exhibits robust chip-package interaction (CPI) reliability as quantified through JEDEC standard TQV stresses (Fig. 9). Both standard (0.91V, 397fF/μm^2) and EHV (1.98V, 157fF/μm^2) high-density MIM capacitors meet TDDB lifetime goals with margin (Fig. 10). The thermal impact from higher power density GAA transistors, technology scaling [6] and heat removal thru the frontside metals is addressed thru benefits such as local cooling enabled by PowerVia & backside metals as well as a full suite of EDA tools to optimally manage thermals at local and global scales to meet the product needs.

SRAM

Intel 18A provides enhanced performance with better Vmin and smaller bitcell area than Intel 3 [1], featuring 0.021mm^2 high-density cells and 0.023mm^2 high current cells. Fig. 11 shows Vmin distributions for SRAM bitcells offered on Intel 18A with and without write assist.

Summary

Intel 18A is in risk-production and offers 18%/25% iso-power performance (0.75V/1.1V) improvement over Intel 3 with over 30% density scaling. Intel 18A provides a high yielding full feature technology capable of both high frequency and low power operation (Fig. 12a) and a full range of analog applications including high speed SerDes (Fig. 12b).

Acknowledgements to Altera Corporation for the collaborative efforts on SerDes work shown in Fig. 12b.

References

[1] W. Hafez, *VLSI 2024.* [2] W. Hafez, *VLSI 2023.* [3] M. Shamanna, *VLSI 2023.* [4] D. B. Ingerly, *IEDM, 2019*. [5] C. Pelto, *VLSI 2024.* [6] C. Landon, *IRPS 2023.*

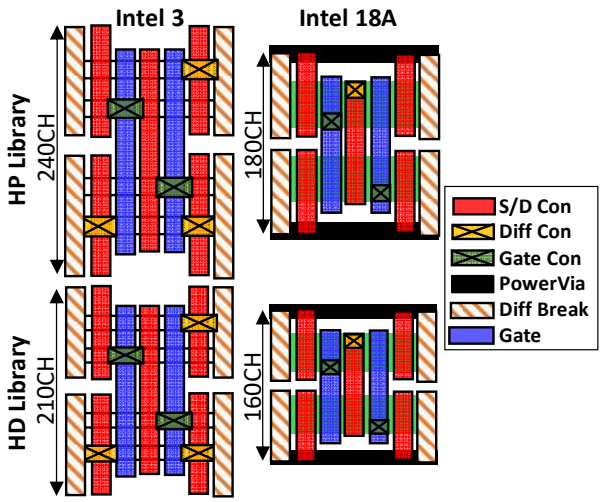


Fig. 1. Standard cell library comparison of Intel 3 versus Intel 18A. Library height scaling achieved by replacing multiple fins with a single ribbon driving the cell size reduction. PowerVia enables power connection at cell boundary.

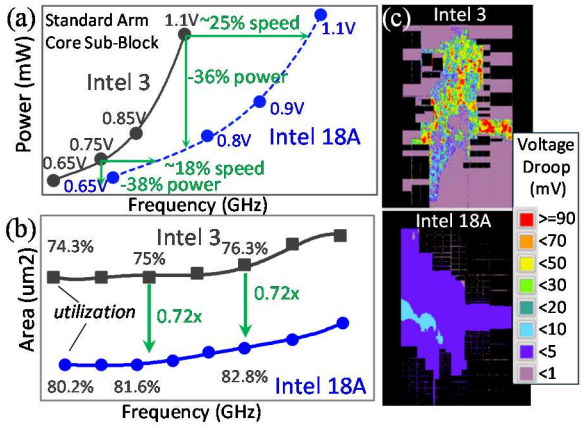
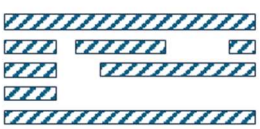


Fig. 2. (a) Intel 18A vs Intel 3, high performance block frequency increases by 18%/25% performance and power decreases by 38%/36% at 0.75V/1.1V. (b) Intel 18A high density block scaling vs Intel 3 is 0.72x with 8-10% benefit in standard cell utilization. (c) Heat maps of industry standard CPU showing 10x worst case IR droop reduction on Intel 18A vs Intel 3 due to back side power (bump to transistor).

(a)

Intel 18A Direct Print EUV Interconnect



Use of direct print EUV patterning below 80P enables no coloring, flexible spacing and leading ease of use.

(b)

Ease of Use Improvements	Intel 18A
Latchup Design Rules	No
Tap Cells Requirement	No
Via Coloring	No
Metal Line Coloring	No
Minimum Via Density DR Simplification	Yes
Flexible Metal ETE Spacing	Yes
Flexible Metal STS Spacing	Yes
Bi-Directional Metal Routing	Yes
Block Integration Simplification	Yes
Layout Drawn Layer Reduction	Yes

Fig. 3. (a) Intel 18A Direct Print EUV at M0-M4 provides ease of use improvements across the entire frontside and backside metal stack seen in the table in (b).

HP/HD Library Height (nm)	180/160
Contacted Poly Pitch (nm)	50
M0 pitch (nm)	32
HCC/HDC SRAM area (um²)	0.023 / 0.021
# of Frontside Metal Layers (ML)	10ML Low cost, 12ML high density, and 14-16ML high perf
# of Backside Metal Layers	3ML + 3ML

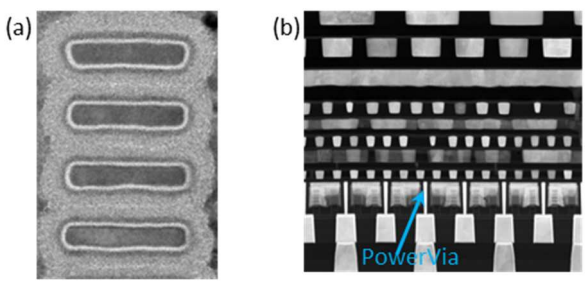


Fig. 4. Table showing Intel 18A technology features and (a) cross-sectional TEM image showing ribbon-cut of a typical RibbonFET and (b) a SEM image showing PowerVia.

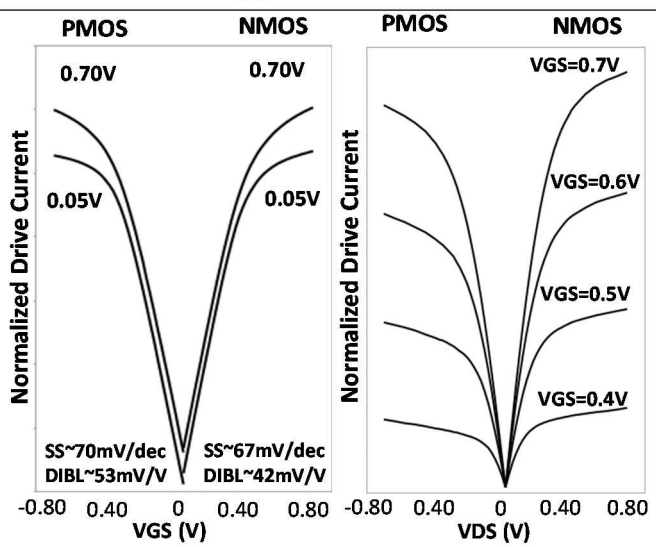
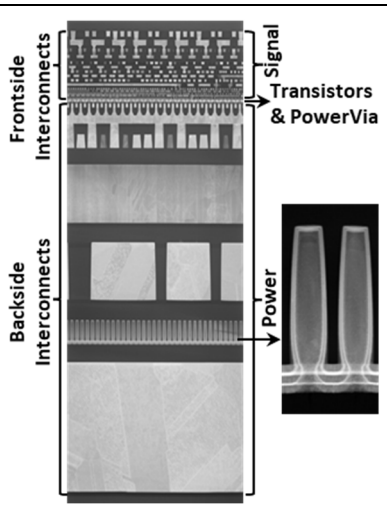


Fig. 5. Intel 18A PMOS and NMOS Id-Vg curves (left) and Id-Vd characteristics (right) showing excellent DIBL and short channel performance.



Intel 18A	
Layer	Pitch (nm)
M13-M14	160
M11-M12	120
M5-M10	80
M3-M4	40
M2	32
M1	50
M0	32
Transistor	50
BM0	160
BM1	300
BM2	480
BM3-BM4	1080
BM5	4000

Fig. 6. Cross-sectional SEM image showing Intel 18A high performance metal interconnect stack (left). Close up of Intel 18A HDMIM (center) and table (right) showing same high performance frontside and backside metals as seen in the left SEM image.

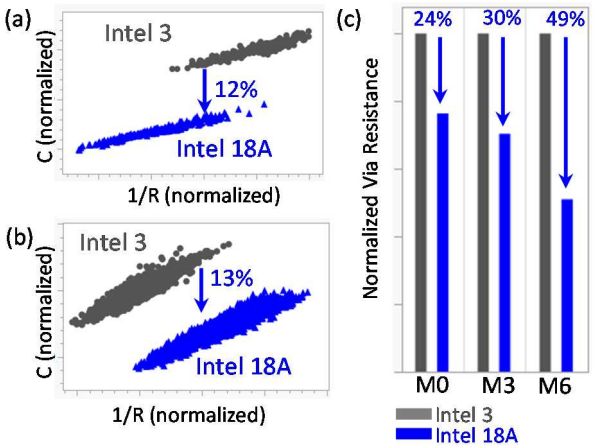


Fig. 7. (a) RC characteristics show improvements of Intel 18A vs Intel 3 metals for (a) ~40nm pitch and (b) ~80nm pitch metals demonstrating 12% to 13% improvement. Min size via resistance improvement is shown in (c) for Intel 18A vs Intel 3 on matched metal layers giving ~25%-50% improvement for min sized vias.

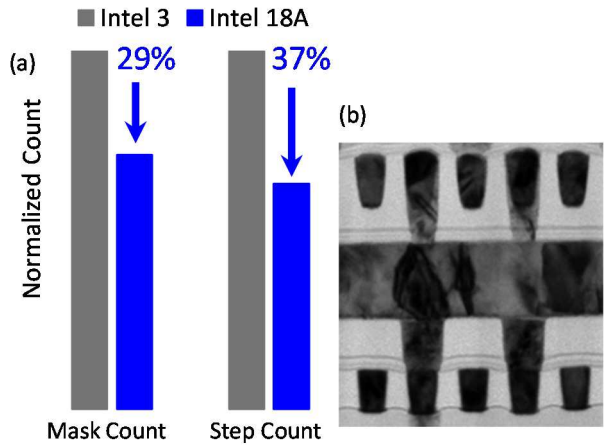
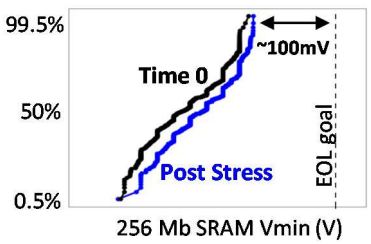


Fig. 8. (a) Innovations in EUV masks and process enabled single trench and single via direct print at M0 to M2 providing 37% fewer steps and 29% fewer masks on Intel 18A vs Intel 3 for those layers. This led to reduced time thru fab, fewer defects, better design ease of use. (b) Cross-sectional SEM image showing Intel 18A M0 to M2.



Stress*	Condition	Duration	Fails/Total Units
Highly Accelerated Stress Test	110°C/85% RH	275 hours	0/352
Bake	165°C	500 hours 1000 hours	0/237 0/98
Temperature Cycling	-55°C – 125°C	750 cycles	0/346

*Units subjected to level 3 preconditioning as per J-STD-20

Fig. 9. Intrinsic SRAM Vmin aging with defect screening at a stress equivalent to 1000h HTOL shows data meeting Vmin aging goals with margin. JEDEC standard CPI stress tests demonstrate robust reliability of the PowerVia feature on Intel 18A shown in table.

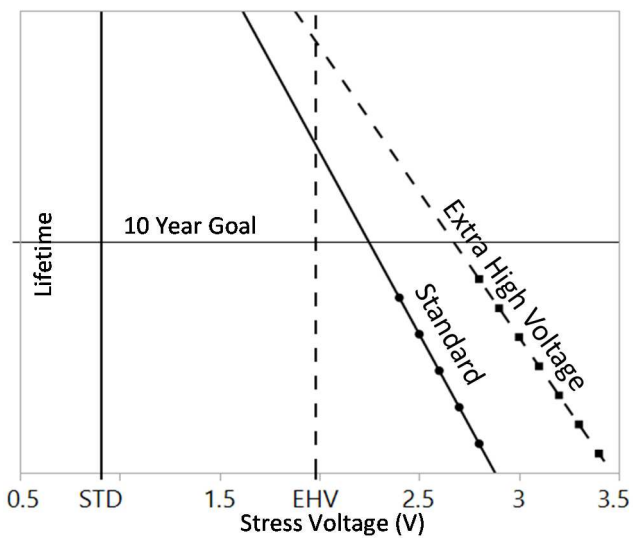


Fig. 10. Intel 18A HDMIM TDDB meets 10-year lifetime goals with margin for both standard (solid) and EHV (dashed) capacitors.

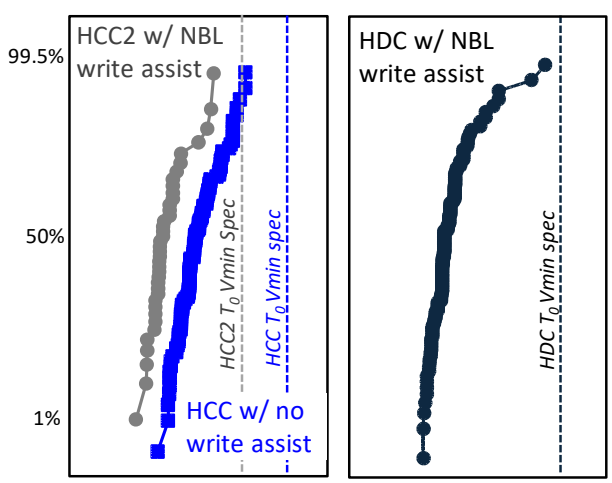


Fig. 11. SRAM VCCmin for Intel 18A 256Mb array. HDC with Negative Bit-Line (NBL) write assist (right), HCC2 with Negative Bit-Line (NBL) write assist (left-grey), and HCC with no write assist (left-blue).

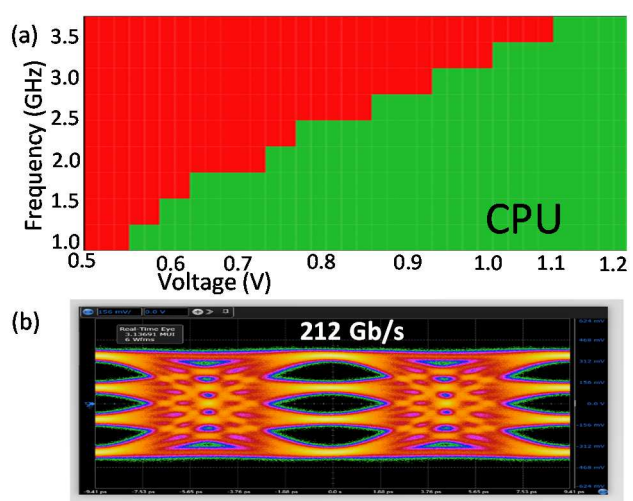


Fig. 12. (a) Intel 18A Shmoo plot of industry standard core on a high-yielding large logic test chip. (b) Measured 212Gb/s PAM4 transmitter eye-diagram of an Ethernet SerDes on Intel 18A.