

# CFS1000

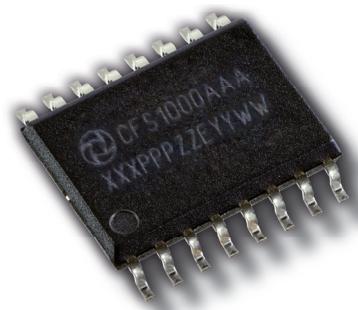
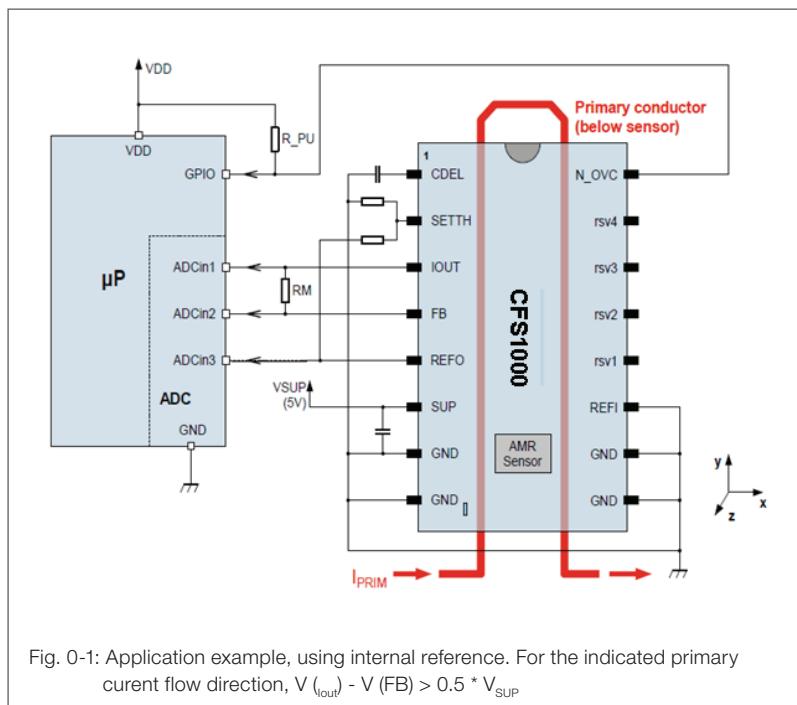
## Integrated MagnetoResistive Current Sensor

The CFS1000 current sensor is designed for highly dynamic electronic measurements of DC, AC, or pulsed currents with integrated galvanic isolation. This current sensor based on the Anisotropic magneto-resistive effect (AMR) enables excellent dynamic response without the hysteresis present in designs using iron-cores. The primary current measured needs to be fed below the sensor on PCB or current rail. Usually a U-shaped conductor is applied to define the magnetic field gradient needed to excite the sensor.

The sensor device includes a high-precision sensor signal conditioner IC providing internal feedback of a compensation current for optimum linearity. The IC-output is an offset calibrated and pre-scaled current which is proportional to the primary current measured. This output is easily converted to a voltage with an external resistor at the post-processing device (usually ADC or amplifier). A precise on-chip voltage reference is generated. Alternatively, an external reference can be used. Total accuracy of a multi-sensor system is improved by sharing one voltage reference for all sensors. Additionally, a fast over-current alarm output allows immediate reaction to overload events independent of controller and software.

### Product Overview

Article Description	Temperature Range	Package
CFS1000 AAA-AE	-40 ... +125 °C	SOIC16w (300mil)



### Features

- Based on the Anisotropic Magnetoresistive (AMR) effect
- Galvanic isolation between primary and measurement circuit
- High immunity against homogeneous magnetic stray fields
- Analog current output
- Internal voltage reference or external reference input
- Measuring range up to threefold nominal current
- Customer programmable sensitivity precision trimming
- Factory programmed zero offset temperature coefficient
- AEC-Q100 qualification pending

### Advantages

- Standard SO16w package (SMD assembly)
- Excellent accuracy
- Negligible hysteresis
- High bandwidth current measurement: DC to 500 kHz
- Fast overcurrent detection with tuneable threshold
- Temperature range from -40 °C to +125 °C

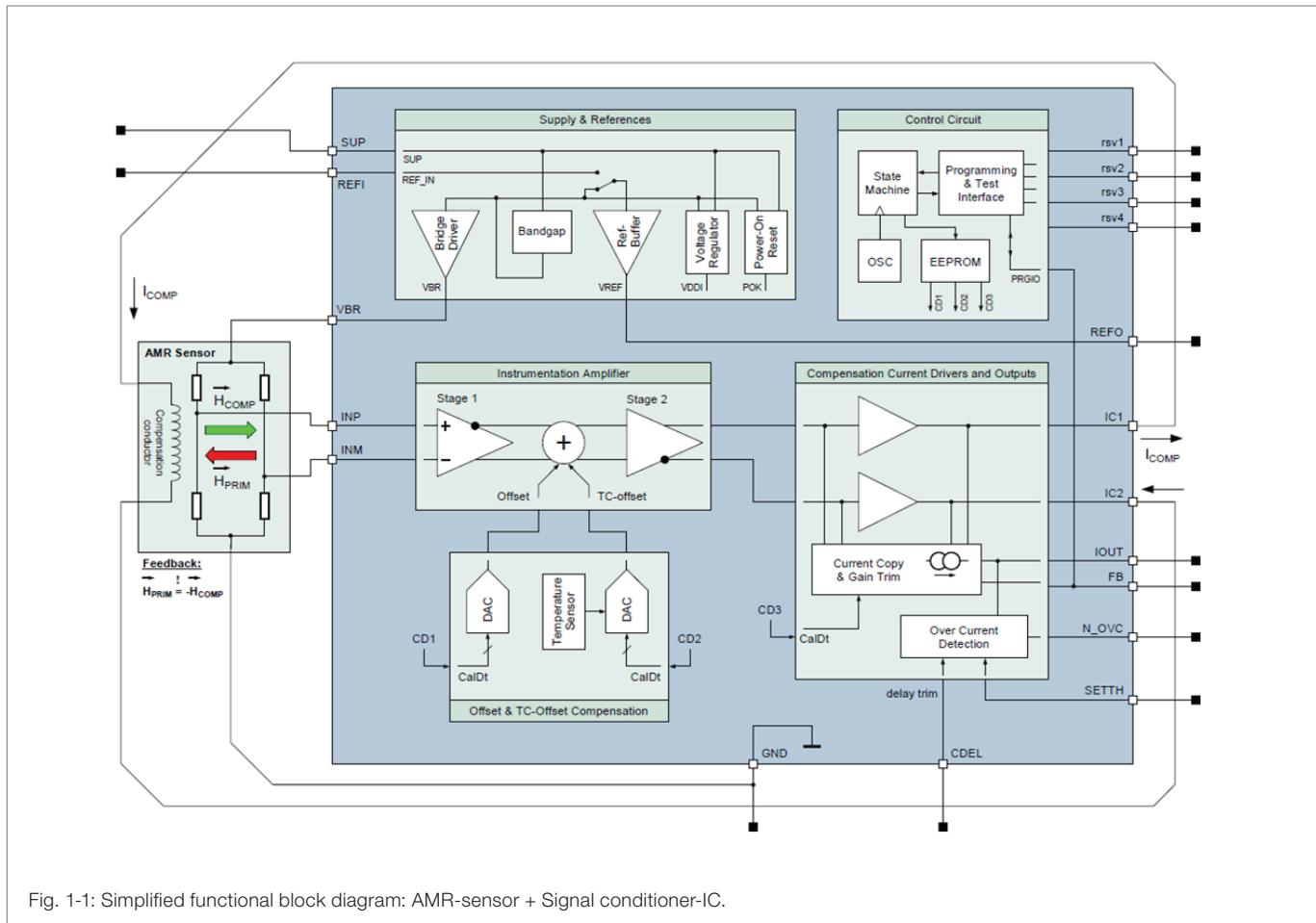
### Applications

- Electrical motor controls
- AC variable speed drives
- Power inverters
- Solar (micro-) inverter
- Switched mode power supplies
- Current measurement for safety switch control
- Battery management
- Laser diode driver



## 1. Principle of Operation

### 1.1. Block Diagram



### 1.2. Brief Functional Description

This component represents a precision current sensing device for contactless measurement using a sensor element based on the Anisotropic MagnetoResistive (AMR) effect. The device comprises the AMR sensor, a signal-conditioning IC and supplementary components for magnetic biasing of the sensor in an SO16 package. The primary current for measurement needs to be fed below the sensing element in a well defined geometrical current path. The magnetic field gradient (component in x-direction, see Fig. 2) is the physical quantity which directly stimulates the AMR sensor. To enable an optimum design of the primary current path a detailed documentation and design tools please contact our sales department.

By integration of the sensor electronics inside a molded plastic package a high isolation voltage (>1kV) with respect to the primary current conductor is achieved, which will be further increased by the PCB between sensor package and primary conductor.

Due to the physical characteristics and the mechanical construction of the sensor, this integrated sensor boasts with negligible hysteresis and low variance of sensitivity to mechanical displacements without the need of magnetic field concentrators. For precise sensitivity calibration the device is prepared for final end-of-line gain trimming (sensor device mounted in a fixed position with respect to the primary conductor).

The signal conditioning ASIC comprises an input amplifier, a differential compensation current driver, a current copy circuit generating the sensor output, trimming stages for offset, offset-TC (temperature coefficient) and gain (sensitivity), calibration interface and NonVolatile Memory (NVM) as well as supporting circuit modules. A low noise, low offset instrumentation amplifier with high bandwidth amplifies the differential input from the AMR-bridge. Measurement of the on-chip temperature is used as an input of the compensation circuit to suppress the thermal offset drift of the AMR-bridge. This offset drift is already calibrated during factory programming of each device in multiple temperature test steps. Additionally, absolute offset errors (from sensor and amplifier) are compensated by appropriate trimming structures in this amplifier stage. Trimming can be performed either during IC factory test or in the final application. The instrumentation amplifier output is passed to a differential current output driver generating the compensation current to the sensor. This compensation current (at pins IC1, IC2) is fed back to the secondary current input of the AMR-sensor bridge. As a consequence of the feedback principle with high loop-gain an excellent linearity of the sensor is achieved because the resistive bridge always operates close to 0mV.

The sensor output is a precise copy of the compensation current. Proper trimming of the measurement sensitivity is achieved by calibration of the current gain of this current-copy output stage. Usually, this final calibration step is performed in the application after assembling the sensor device CFS1000 with the primary current conductor. For permanent storage of the digital calibration data an E<sup>2</sup>PROM as a non-volatile memory is included in the sensor IC. For transfer of calibration data between IC and the external calibration hardware an asynchronous programming interface via pin FB is integrated, which can be accessed in a defined time window after power-on of the device.

As a fast over-current monitor a comparator supervises the sensor output and signals the status at pin N\_OVC. This output is pulled to digital low level whenever the measured current (corresponding to the absolute value at IOUT) exceeds a fraction of the full-scale range defined by the voltage level at SETTH.

Further blocks of the ASIC are reference voltage and reference current generators, the stabilized supply to the sensor bridge and a stabilized supply voltage to the internal blocks. A buffered voltage reference output is provided at pin REFO which is connected either to the precise internal voltage reference (2.5V) or an external reference input REFI. With pin REFI at low level (connected to ground) the internal reference is available at pin REFO and with REFI above a decision threshold, this input voltage is copied to output pin REFO. Also a power-on reset circuit is integrated to suppress any invalid or disturbed sensor output in case of supply voltage VSUP out of its specified range.

## 2. Package Information

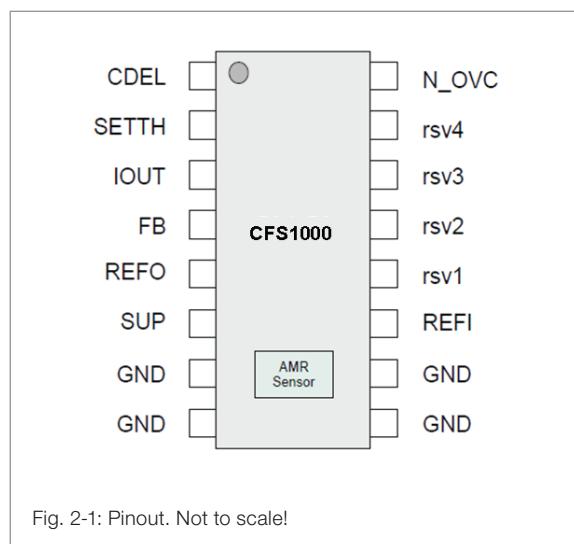
### 2.1. Plastic Package

The product is available in a Pb free, RoHS compliant, 16 lead Small Outline Wide plastic package (SO16w, 300 mil) with about 106 mm<sup>2</sup> (0.165 square inch) footprint area. For dimension details refer to JEDEC standard MS-013-E, version AA.

The device (packaged device only) has been qualified according to JEDEC J-STD-020 for the following soldering profile:

1. (200±5) °C, dwell time (50±5) s
2. (260±5) °C, dwell time <10 s

### 2.2. Pin Configuration



Note:

The magnetically sensitive area of the device is centered on the virtual connecting line between pins 7 and 10 of the package (see also Fig. 7-1).

### 2.3. Pin Description

Pin No.	Pin Name	Type <sup>1)</sup>	Description	Remark
1	CDEL	A IO	Delay setting capacitor for over-current detection	
2	SETTH	A I	Threshold setting input for over-current detection	
3	IOUT	A O	Current output signal	
4	FB	A I	Feedback pin for current output IOUT; in programming mode IC digital IO of ASIF	Connect shunt resistor to IOUT
5	REFO	A O	Reference voltage output	
6	SUP	S	Supply (5V)	
7	GND	S	Ground connection	Multiple ground pins (7 - 10)
8	GND	S	Ground connection	
9	GND	S	Ground connection	
10	GND	S	Ground connection	
11	REFI	A I	Reference select / reference voltage input	Connect to GND for internal reference
12	rsv1	D I	Internally connected. Reserved for factory use.	<sup>2)</sup> <sup>3)</sup>
13	rsv2	-	Internally connected. Reserved for factory use.	Leave open!
14	rsv3	D I	Internally connected. Reserved for factory use.	<sup>2)</sup> <sup>3)</sup>
15	rsv4	-	Internally connected. Reserved for factory use.	<sup>2)</sup>
16	N_OVC	D O	Over-current alarm output; open drain driver	Low active (high-resistive pull-up integrated)

<sup>1)</sup> D = digital, A = analog, S = Supply, I = Input, O = Output, HV = High Voltage.

<sup>2)</sup> Recommend to be connected to GND in the application, may be left open.

<sup>3)</sup> Optionally used in application programming, see section 6.6.2.

### 3. Absolute Minimum/Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

All voltages referred to V(GND). Currents flowing into terminals are positive, those drawn out of a terminal are negative.

No.	Parameter	Condition	Symbol	Min.	Max.	Unit
1	Supply voltage		$V_{SUP}$	-0.3	+6.5	V
2	Voltage at digital I/O pins rsv1, rsv3		$V_{DPIN}$	-0.3	$V_{SUP} + 0.3$	V
3	Input current at digital pins rsv1, rsv3		$I_{DPIN}$	-20	+20	mA
4	Voltage at digital open drain output N_OVC		$V_{N_OVC}$	-0.3	$V_{SUP} + 0.3$	V
5	Current at open drain output OVC	Output driver off	$I_{N_OVC}$	-20	+20	mA
6	Voltage at analog pins IOUT, FB, REFO, SETTH, CDEL		$V_{APIN}$	-0.3	$V_{SUP} + 0.3$	V
7	Input current at analog pins IOUT, FB, REFO, SETTH, CDEL		$I_{APIN}$	-20	+20	mA
8	Voltage at pin REFI		$V_{REFI}$	-0.3	8.0	V
9	Input current at pin REFI		$I_{REFI}$	-20	+2	mA
10	Junction temperature		$T_J$	-40	+150	°C
11	Ambient temperature	packaged in SO16	$T_{AMB}$	-40	+125	°C
12	Storage temperature <sup>1)</sup>	not supplied	$T_{STG}$	-40	+125	°C
13	Power dissipation		$P_{TOT}$		300	mW

<sup>1)</sup> Packing materials such as tapes, reels, dry packs, foils, etc. are not considered. Please contact Sensitec for packing material specifications. Packaged devices before soldering: For moisture sensitive devices refer to JEDEC standard J-STD-033 for handling and using details. Storage temperatures > 90 °C for more than 96 h may affect the solderability of the device.

### 4. ESD Protection

Symbol	Condition	Min.	Type	Max	Unit	Description
$V_{PIN,ESDHBM}$	1)	2			kV	ESD HBM protection at all pins
$V_{PIN,ESDCDM}$	2)	750			V	ESD CDM protection at corner pins
$V_{PIN,ESDCDM}$	2)	500			V	ESD CDM protection at all other pins

<sup>1)</sup> According to AEC-Q 100-002 chip level test.

<sup>2)</sup> According to AEC-Q 100-011 chip level test.

## 5. Recommended Operating Conditions

The recommended operating conditions must not be exceeded in order to ensure proper functionality of the device. All parameters specified in the following sections refer to these recommended operating conditions if not otherwise stated.

All voltages referred to V(GND). Currents flowing into terminals are positive, those drawn out of a terminal are negative.

	Parameter	Condition	Symbol	Min.	Type	Max.	Unit
1	Supply voltage		V <sub>SUP</sub>	4.75	5.0	5.25	V
2	Nominal range of magnetic flux gradient (for nominal output current $I_{OUT}$ )	Permanent (DC) <sup>1)</sup> <sup>2)</sup>	( $\Delta B/\Delta x$ )FS	-2.2		2.2	mT/mm
	Double flux gradient	For maximum 3s, and duty cycle < 1:10 <sup>1)</sup>	( $\Delta B/\Delta x$ )2FS	-4.4		4.4	mT/mm
	Triple flux gradient	For maximum 50ms, duty cycle < 1:100 <sup>1)</sup>	( $\Delta B/\Delta x$ )3FS	-6.6		6.6	mT/mm
3	Storage temperature (not supplied)	For less than 10 years	T <sub>STG</sub>	-40		+85	°C
		For maximum 5000 h during lifetime		+85		+125	°C
4	Junction Temperature	Normal operation	T <sub>J</sub>	-40		+125	°C
		For max. 500 h over life time	T <sub>J</sub>	+125		150	°C
5	Load resistor between pins I <sub>OUT</sub> and FB	For triple output current range ( $I_{OUT}$ )	R <sub>M_triple</sub>	100	270	300	Ω
		For nominal output current range ( $I_{OUT}$ )	R <sub>M_nom</sub>	300		900	Ω

<sup>1)</sup>

Limitations to exposure times to magnetic field input (and resulting output) are due to the resulting power dissipation generated mainly by the sensor compensation current (see ch. 6.2.2) producing thermal heat inside the SO16-package. Sensor calibrated in sensitivity.

<sup>2)</sup>

Note: An excess homogenous in-plane magnetic field in x- and y direction (see fig. 2) superimposing the effective flux gradient should be kept below  $B_{x,y} < 0.6$  mT by design of the application.

## 6. Functional Description and Electrical Parameters

### 6.1. Supply and References

#### 6.1.1. Electrical Parameters

( $V_{SUP} = 4.75V \dots 5.25V$ ,  $T_{AMB} = -40^{\circ}C \dots +125^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{SUP} = 5.0V$  and  $T_{AMB} = 25^{\circ}C$ . Positive currents are flowing into the device pins.)

Table 1: Supply and references block electrical parameters.

No.	Symbol	Condition	Min.	Type	Max	Unit	Description
1	$I_{SUP(Q)}$	Zero field ( $\partial B_x / \partial x = 0$ ) <sup>2)</sup>	-	21	28	mA	Quiescent supply current
2	$V_{SUP(POR)}$	Falling supply	3.7		4.4	V	Power-on reset threshold
3	$V_{SUP(POR,HYS)}$	(Rising – falling) supply <sup>1)</sup>	0.2		0.4	V	Power-on reset hysteresis
4	$V_{REFO,25}$	$I_{REF} = \pm 1.5mA$ $ V_{REF}  < 0.3V$ $T_{AMB} = 25^{\circ}C$	2.485	2.50	2.515	V	Internal reference output voltage @ room temperature
5	$V_{REFO}$	$I_{REF} = \pm 1.5mA$ $ V_{REF}  < 0.3V$	2.465		2.535	V	Internal reference output voltage
7	$d_{VREFO}$	$V_{REFO}(I_{REFO}) - V_{REFO}(0)$ $I_{REFO} = -1.5 \dots +1.5mA$ $ V_{REF}  < 0.3V$ <sup>1)3)</sup>	-2		+2	mV	Load regulation internal reference
8	$V_{REFI(TH)}$	Decreasing $V_{REFI}$ until $V_{REFO}$ increases from $V_{REFI}$ to 2.5V	0.5		1.0	V	Decision threshold for switching from internal to external reference at input REFI
9	$V_{REFI(RANGE)}$	<sup>1)4)</sup>	1.2	2.5	2.6	V	Range of external reference
10	$V_{REFO(OS),25}$	$V_{REFI} = 2.5V$ $I_{REFO} = 0mA$ $T_{AMB} = 25^{\circ}C$	-4		+4	mV	Offset voltage (REFO - REFI) @ room temperature
11	$V_{REFO(OS)}$	$V_{REFI} = V_{REFI(RANGE)}$ $I_{REFO} = 0mA$	-5		+5		Offset voltage (REFO - REFI)
12	$I_{REFI(LK)}$	$V_{REFI} = 2.5V$	-1		1	µA	REFI input leakage current
13	$t_{PON}$	$V_{SUP}$ surpasses 4.75, $I_{OUT}$ settles to error band < 2% <sup>1)</sup>			4.0	ms	Power-on delay until output settled
14	$t_{INIT}$	See Fig. 6-2	0.40	0.51	0.62	ms	Initialization time from power-on to ASIFEN = 1
15	$t_{ASIFEN}$	See Fig. 6-2	2.2	2.5	2.8	ms	ASIF activation time during start-up sequence
16	$T_{OFF}$	Increasing T until OVC falls to 0	155		180	°C	Over-temperature shut-down threshold
17	$T_{HYS}$	Decreasing temperature	10		30	°C	Over-temperature threshold hysteresis

<sup>1)</sup> Defined by design. Not subject to production test.

<sup>2)</sup> Measurement condition: SETTH = REFI = 0V; N\_OVC = CDEL = REFO = open (hi-Z).

Note: The current consumption depends on sensor input (B-field). Typically,  $I_{SUP}$  increases by approximately  $13 * |I_{OUT}|$

<sup>3)</sup> Load capacitance  $C_{REFO} \leq 1.5nF$

<sup>4)</sup> It has to be avoided by external circuitry when using an external reference, the voltage  $V_{REFI}$  could rise above the supply  $V_{SUP}$ .

### 6.1.2. Description

This block includes voltage regulators for the excitation of the AMR sensor bridge and to supply the internal digital and analog blocks of the signal conditioning IC. Both are generated from a precision bandgap voltage reference circuit. Also a buffer amplifier for the reference voltage output REFO which is selected from the internal voltage reference (bandgap) or an external reference input, a power-on reset monitor and a over-temperature monitor are part of this block.

#### 6.1.2.1. Reference Voltage Generation

The IC includes an internal bandgap based reference voltage of 2.5V (V2V5). An additional reference buffer feeds the reference to the output REFO in two different operation modes (see Fig. 6-1):

- If  $V_{REFI} < V_{REFI(TH)}$ : buffering internal V2V5 to the output at pin REFO, or
- If  $V_{REFI} \geq V_{REFI(TH)}$ : buffering an external reference voltage applied at REFI to output pin REFO

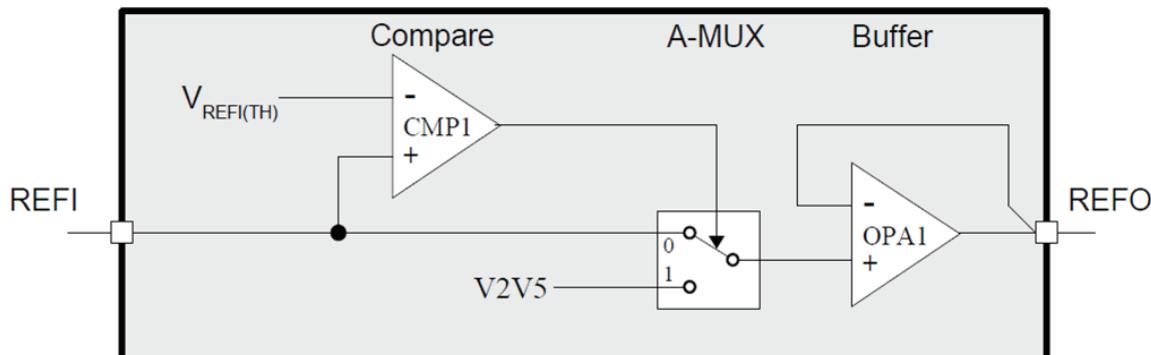


Fig. 6-1: REFO reference buffering.

This means, the input REFI is used simultaneously as a reference voltage input and for the level based decision which reference to be fed to the output.

At least two application cases for external reference voltage can be considered:

- Use a reference lower than the internal 2.5V to define an asymmetric output signal (kind of “unipolar mode”)
- Use the same reference for several sensors to suppress the influence of mismatches of different references from different devices. E.g. in a 3-phase current measurement system the reference output REFO of one sensor can be used as input of the two other sensors or one very precise external reference would be used as input to all three sensor channels.

### 6.1.2.2. Reset Block

The IC contains an internal reset comparator, which observes the internal supply voltage. Due to the voltage drop at the regulator, the reset threshold  $V_{PON} = V_{SUP(POR)} + V_{SUP(POR,HYS)}$  for rising supply voltage  $V_{SUP}$  shows a slightly wider spread than the threshold spread directly at the regulated voltage, but power up within the specified supply range is ensured. The reset comparator has a hysteresis  $V_{SUP(POR,HYS)}$ .

The general behavior of the reset block is depicted in Fig. 6-2. With rising supply after  $V_{SUP}$  surpasses the power-on threshold, the IC copies the adjustment data from E<sup>2</sup>PROM to the corresponding data registers. This process is completed after  $t_{INIT}$ . Subsequently, for a duration  $t_{ASIFEN}$  the pins FB and IOUT are held in tri-state to allow for a log-in to the asynchronous programming interface (ASIF) via the pin FB, which is operated in as a digital interface-I/O in this mode. This interface is described in more detail in another section below.

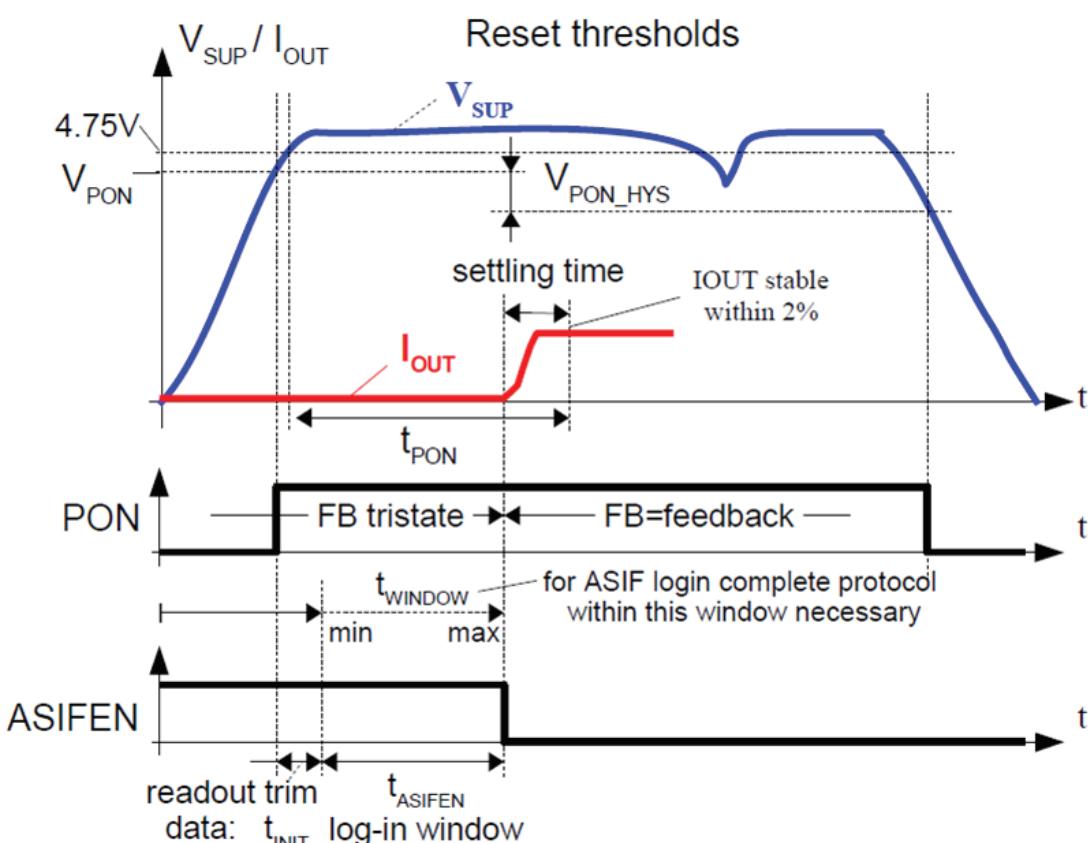


Fig. 6-2: Power-on timing and ASIF enable function.

### 6.1.2.3. Overtemperature Monitor

To protect the IC from excessive heating by internal power sources a temperature sensor is integrated. If the junction temperature exceeds the temperature threshold  $T_{OFF}$ , the following actions are initiated :

- Compensation coil driver at pins IC1 and IC2 are switched off, and
- Due to the switch off of the compensation current also the output current  $I_{OUT}$  will be zero:  
 $V_{IOUT} \approx V_{FB} \approx V_{REF0}$  (only differing by offset voltages in between), and
- Pin N\_OVC output is pulled to Low

The over-temperature monitor has built in a hysteresis  $T_{HYS}$ , which ensures the IC can return to normal operation only, when the junction temperature has cooled down below  $T_{OFF} - T_{HYS}$ .

## 6.2. General Sensor Performance

### 6.2.1. Electrical Parameters

( $V_{SUP}$  = 4.75V ... 5.25V,  $T_{AMB}$  = -40°C ... +125°C, unless otherwise noted.

Typical values are at  $V_{SUP}$  = 5.0V and  $T_{AMB}$  = 25°C. Positive currents are flowing into the device pins).

Table 2: Sensor operating characteristics.

Symbol	Condition	Min.	Type	Max	Unit	Description
Output characteristics						
$I_{IOUT(L)}$	$V_{IOUT} = 0.5V$ $V_{FB} = V_{REFO} + 100mV$	6	7	-	mA	Output low current drive capability
- $I_{IOUT(H)}$	$V_{IOUT} = V_{SUP} - 0.5V$ $V_{FB} = V_{REFO} - 100mV$	6	7	-	mA	Output high current drive capability
BW	$RM = 330\Omega$ <sup>1)</sup> $T_{AMB} = 25^\circ C$ <sup>2)</sup>	400	500	-	kHz	Signal bandwidth (-3dB)
$V_{FB(OS)}$	$I_{IOUT} = 0mA$ $RM = 330\Omega$ <sup>1) 2)</sup>	-5	-	5	mV	Offset FB to REFO (closed loop operation)
$P_{PSRIOUT}$	$RM = 330\Omega$ <sup>1)</sup> $f_{SUP} \leq 5kHz$ $B_x = \text{const.}$ <sup>2)</sup>	50	-	-	dB	Power supply rejection PSR= $\Delta V_{SUP} / \Delta V_{IOUT}$
$R_{IOUT(PD)}$	IOUT to GND <sup>2)</sup>	4.7	-	-	kΩ	Output load resistance
$R_{IOUT(PU)}$	IOUT to SUP <sup>2)</sup>	4.7	-	-	kΩ	Output load resistance
Pre-programming target (RM = 330Ω) <sup>1)</sup>						
$I_{IOUT(OS)PRE}$	$(\Delta B / \Delta x) = 0 mT/mm$ , $V_{REFO} = 2.5V$ , 4), 12) $T_{AMB} = 25^\circ C$	-10 (-0.5%)	-	+10 (0.5%)	µA ( $I_{OUT(IFS)}$ )	Pre-programmed output offset current
	$T_{AMB} > 85^\circ C$	-25 (-1.2%)	-	+25 (1.2%)	µA ( $I_{OUT(IFS)}$ )	
	$T_{AMB} - 40^\circ C$	-35 (-1.7%)	-	+35 (1.7%)	µA ( $I_{OUT(IFS)}$ )	
$S_{X,PRE}$	$T_{AMB} = 25^\circ C$ <sup>3) 4)</sup>	-	1.0	-	mA / (mT/mm)	Pre-programmed sensitivity
Offset current output calibration (RM = 330Ω) <sup>1)</sup>						
$N_{OS,DAC}$			8	-		Offset current output calibration bits
$LSB_{OS}$	Sensitivity = $S_{X, PRE}$ $T_{AMB} = 25^\circ C$ <sup>5)</sup>		3.5	5.6	µA	Average current output step size (offset LSB value)
$ERR_{OUT(OS)}$	$T_{AMB} = 25^\circ C$ <sup>6)</sup>	-0.85 (-4.8µA)	-	+0.85 (+4.8µA)	LSB <sub>OS</sub>	Offset current output calibration resolution
Sensitivity calibration, Lateral field gradient in x-direction $B_X = 2.0 mT/mm$ (RM = 330Ω) <sup>1) 4)</sup>						
$N_{GAIN,DAC}$		-	8			Sensitivity calibration bits
$L_{SBSX}$ $S_{X,MAX/SX,MIN}$	$I_{OUT} \gg 2mA$ , $T_{AMB} = 25^\circ C$ $T_{AMB} = 25^\circ C$ <sup>7)</sup>	1.67	0.3	0.5 2.0	% $I_{OUT}$	Step size of sensitivity calibration Gain calibration range
$S_X$	$T_{AMB} = 25^\circ C$ <sup>4)</sup>	0.88	1.0	1.0	mA / (mT/mm)	Range of sensitivity trimming ensured by gain calibration

Symbol	Condition	Min.	Type	Max	Unit	Description
Output ranges and error components						
$I_{OUT(FS)}$	$(\Delta B/\Delta x) = 2 \text{ mT/mm}$	-	$\pm 2.0$	-	mA	Nominal output range (after calibration)
$I_{OUT(PEAK)}$	$(\Delta B/\Delta x) = 6 \text{ mT/mm}$	-	$\pm 6.0$	-	mA	Peak output range (after calibration)
$TC_{SX}$	$T_{AMB} = -40 \dots +125^\circ C$ <sup>2) 8)</sup>	-80	-	80	ppm/ $^\circ C$	Thermal drift of sensitivity
$\Delta I_{OUT(OS, REF)}$	$(\Delta B/\Delta x) = 0 \text{ mT/mm}$ , $I_{OUT}(1.2V) - I_{OUT}(2.5V)$ , $T_{AMB} = 25^\circ C$ <sup>4) 13)</sup>	10 (-0.5%)	-	+10 (0.5%)	$\mu A$	Offset shift due to variation of $V_{REFI}$ (external reference)
$LIN_{ERR(NOM)}$	Nominal range: <sup>2) 9)</sup> $I_{OUT} = I_{OUT(FS)}$	-6	-	6	$\mu A$	
$LIN_{ERR(PEAK)}$	Peak output range: <sup>9)</sup> $I_{OUT} = 3 * I_{OUT(FS)}$	-30	-	+30	$\mu A$	Linearity sensitivity error
$I_{OUT(NOISE)}$	BW = 1Hz - 500kHz BW = 1Hz - 20kHz BW = 1Hz - 1kHz	-	2.5 2.0 0.5	-	$\mu ARMS$ $\mu ARMS$ $\mu ARMS$	Output noise
Over current detection						
$V_{SETTH}$	<sup>2)</sup>	0.5	-	$V_{REFI}$ -0.2	V	Over current detection threshold
$R_{SETTH(PU)}$		400	600	1000	k $\Omega$	Pull-up resistor to supply
$V_{OVC(HYS)}$	Rising edge N_OVC <sup>2)</sup> (back to passive)	20	-	100	mV	Over current detection voltage hysteresis
$\Delta V_{IOUT(OVC)}$	$V_{REFI} = 2.5V$ <sup>10)</sup>	-30	-	30	mV	Accuracy of over current detection (voltage level)
$V_{OVC(L)}$	OVC detection active $I_{OVC} = 5mA$	-	-	0.5	V	OVC output low level
ROVC(PU)		75	125	200	k $\Omega$	Pull-up resistor to supply
tOVC(D,0)	Falling edge <sup>2) 11)</sup> $C_{DEL} = 0$ , $V_{SETTH} = 1.0V$		-	500	ns	OVC propagation delay, intrinsic delay
$\Delta tOVC(D)$	$V_{SETTH} = 1.0V$ <sup>2) 11)</sup>	15	20	25	ns/pF	Additional OVC delay by use of CDEL capacitor
tOVC(D,F)	$V_{CDEL} = 0V$	10	15	20	$\mu s$	Maximum delay (time-out) at OVC when CDEL at GND

<sup>1)</sup> Output feedback IOUT to FB established with resistor RM. It is recommended to use a low TC-type resistor RM.

<sup>2)</sup> Defined by design. Not subject to production test.

<sup>3)</sup> Raw device characteristics before calibration.

<sup>4)</sup> Gradient of the magnetic field applied lateral in the sensor plane (x-direction, see Fig. 1) generated by the primary current.

<sup>5)</sup> Average current step size defined as  $\{ I_{OUT}(D\_OS = 0x7F) - I_{OUT}(D\_OS = 0x80) \} / 254$ .  
(The spread of the average LSB results from sensitivity spread of the internal sensor).

<sup>6)</sup> Due to the differential non-linearity (DNL) of the offset-DAC (e.g. at MSB change) the residual error after offset calibration can be larger than the ideal  $0.5 \cdot \text{LSB}$ .

<sup>7)</sup> The gain trimming range for maximum ( $D\_GAIN = 0x7F$ ) and minimum ( $D\_GAIN = 0x80$ ) gain settings are expressed by this Fig.  
(The mid setting of gain is taken for  $D\_GAIN = 0x00$ ).

<sup>8)</sup> Temperature coefficient of sensitivity:

$$TC_{SX} = \frac{S_x(T_2) - S_x(T_1)}{S_x(25^\circ C) \cdot (T_2 - T_1)} \text{ with } T_2 = 125^\circ C, T_1 = -40^\circ C.$$

<sup>9)</sup> BFSL method ("best fit straight line").

<sup>10)</sup> Over current detection voltage level:  $V_{IOUT(OVC)} = |V_{IOUT} - V_{FB}| - |V_{REFI} - V_{SETTH}|$ .

<sup>11)</sup> Delay time from passing the (absolute) threshold level defined by  $V_{SETTH}$  at  $I_{OUT}$  and output falling below 1.0V. Total delay is given by the sum of intrinsic delay and additional delay defined by capacitor at CDEL:  $t_{OVC(D,0)} + CDEL * \Delta t_{OVC(D)}$ .

<sup>12)</sup> The offset can drift as much as  $\pm 20\mu A$  (equivalent  $\pm 1\%$  of nominal output  $I_{OUT(FS)} = 2mA$ ) over the lifetime of this product.

<sup>13)</sup> When operated at reference levels different from the (internal) default of 2.5V, an additional offset shift can occur due to the limited common rejection (CMR) of the amplifier. This offset shift can be canceled by re-calibration of the offset at  $V_{REFI}$ .

### 6.2.2. Description

By construction this AMR sensor is sensitive to magnetic field gradients in x-direction (parallel to the transversal axis of the IC). Therefore, current measurement in one conductor line requires the primary conductor to be fed forward and back below the sensor to create the differential field in the sensor plane ("U-shape"). The measurement based on evaluation of the magnetic field gradient (i.e. difference) makes the sensor insensitive to homogenous magnetic stray fields superimposed. But, to ensure very good sensor performance magnetic field components in x- and y-direction in the sensor plane should be smaller than 0.6 mT. The base width of the magnetic sensor, i.e. the distance between the two legs of the magneto-resistive bridge, is 1.24 mm. The magnetic sensitivity orthogonal to the chip plane (z-direction) is negligible.

(See Fig. 1 for a definition of the Cartesian coordinate system relative to the device in SO16-package.)

The principle of operation of the magneto-electrical loop as depicted in Fig. 6-3 can be described as follows:

- The field (difference) HPRIM generates a bridge output VIN across the IC input pins INP and INM.
- This IC-input voltage VIN is amplified ( $G_1 * G_2$ ) and corrected with adjustment inputs for offset and (linear) temperature coefficient of offset (TCO).
- This offset corrected output is amplified further amplified by ( $G_3$ ) and V-I-converted by a transmission factor  $1/R_{SENSE}$  into an output current  $I_{COMP}$ , which is then driven to the compensation wire of the sensor (resistance  $R_{COMP}$ ).
- At the AMR sensor this compensation current  $I_{COMP}$  generates a differential magnetic field HCOMP with opposite polarity as the primary input field HPRIM and thereby closes the (negative) feedback loop.
- Due to a high loop gain  $A_{LOOP}$  the primary input HPRIM is perfectly compensated ( $H_{COMP} = -H_{PRIM}$ ) and  $I_{COMP}$  is a highly linear representation of the primary input current  $I_{PRIM}$ .
- Finally, the output signal  $I_{OUT}$  is generated as a linear copy of the compensation current  $I_{COMP}$ . The reciprocal of this gain  $I_{OUT}/I_{COMP}$  in the following is denoted as „current copy ratio“  $F_{CC}$ .

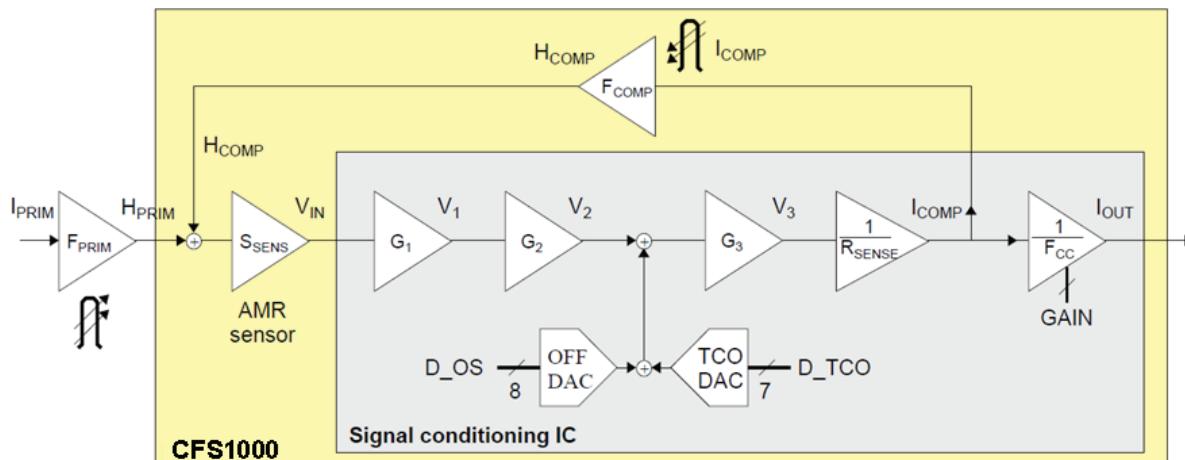


Fig. 6-3: Sensor signal path (model).

The following equations are used to describe the sensor transfer characteristic:

$$I_{\text{OUT}} = \frac{F_{\text{PRIM}}}{F_{\text{COMP}}} \cdot \frac{1}{F_{\text{CC}}} \cdot I_{\text{PRIM}} ; \text{ with } A_{\text{LOOP}} \gg 1.$$

Where F<sub>PRIM</sub> describes the coupling factor of primary current I<sub>PRIM</sub> to magnetic field H<sub>PRIM</sub> at sensor given by the geometry of the primary conductor beneath the sensor.

According to Fig. 6, the loop gain is defined as:

$$A_{\text{LOOP}} = S_{\text{SENS}} \cdot F_{\text{COMP}} \cdot G_1 \cdot G_2 \cdot G_3 \cdot \frac{1}{R_{\text{SENSE}}} .$$

(With the magnetic sensitivity of the bridge S<sub>SENS</sub> and F<sub>COMP</sub> being the sensor internal field coupling factor of I<sub>COMP</sub>.)

Adjustment of system offset, offset thermal drift (TCO) and the gain (or sensitivity), respectively are described below.

### 6.2.2.1 Offset Adjustment

In Fig. 6-3 two DA-converters are shown which are employed for trimming of the system offset and the temperature coefficient of this offset independently from each other. The major offset contribution is introduced by the AMR-sensor bridge itself, but also some offset contribution from the input amplifier of the signal conditioning IC exists.

The offset-DAC adds a multiple of a voltage LSB after the fixed gain input stages (G1 and G2) into the signal path, which is generated on-chip appropriately to the requirements of the sensor bridge. The resulting offset current at the output shows some minor parametric dependence on the sensor parameters (proportional to 1/ [SSENS \* FCOMP] ) due to the closed loop structure described above (Fig. 6-3). The corresponding output referred LSB is specified as LSBOS (see Ch. 6.2, Table 2). With an 8-bit calibration word, the resulting offset range with this LSBOS is suited to calibrate for all expected offset contribution of sensor and amplifier path.

The value of the adjust byte D\_OS[7:0] has to be interpreted as follows:

- D\_OS[7]: sign of offset compensation (0 = positive; 1 = negative).
- D\_OS[6:0]: unsigned integer with absolute value of offset compensation.

The table below gives an overview of the typical offset current setting as a function of D\_OS [7:0].

D_OS <sub>DEC</sub> [6:0]	D_OS <sub>HEX</sub> [6:0]	Output offset <sup>1)</sup> I <sub>OUT,OS</sub> [ $\mu$ A]	
		D_OS[7] = 0	D_OS[7] = 1
0	0x00h	0	0
1	0x01h	+3.5	-3.5
2	0x02h	+7.0	-7.0
...	...	...	...
127	0x7Fh	+445	-445

<sup>1)</sup> Typical values at 25°C with sensitivity trimmed to nominal setting SENS<sub>X,PRE</sub> (see table 2).

The sensor CFS1000 is pre-calibrated to zero-offset by production sequence at component delivery, but it can be re-trimmed later in the application environment. For optimum accuracy it is recommended to perform a final calibration of offset and sensitivity (Ch. 6.2.2.2) together with a run-in sequence in an application environment.

A second DAC for compensation of the offset drift in temperature (TCO) is used exclusively during Sensitec production sequence to trim the overall offset drift to zero. This trimming module cannot be accessed regularly by the external programming interface (Ch. 6.6).

### 6.2.2.2 Current Output and Gain Adjustment

The output driver provides an output current between pins IOUT and FB which is proportional to the input signal. For conversion to voltage output a resistor RM is connected from pin IOUT to FB.

As described above, as a consequence of the feedback employed, the compensation current ICOMP is a precise image quantity of the primary current IPRIM, (generating a magnetic field, detected by the AMR sensor bridge). From this compensation current ICOMP, which is still quite large and cannot fit the necessary output range directly, an output current IOUT is generated with a current copy function with constant “current copy gain” (1/FCC) and high linearity, with FCC defined as:

$$F_{CC} = \frac{I_{COMP}}{I_{OUT}} \quad (\text{"current copy ratio" = inverse of "current copy gain"}).$$

To compensate for process variations of the AMR bridge itself and to allow a precise gain trimming, FCC is adjustable with an 8-bit gain control DA-converter.

Fig. 6-4 below depicts the simplified schematic of the current copy function. In a first stage (G5) the compensation current ICOMP is sensed by resistor RSENSE and the drop is amplified and converted to a single-ended output. Then, a voltage-to-current converter (VIC) using op-amp OP1 generates the output signal IOUT .

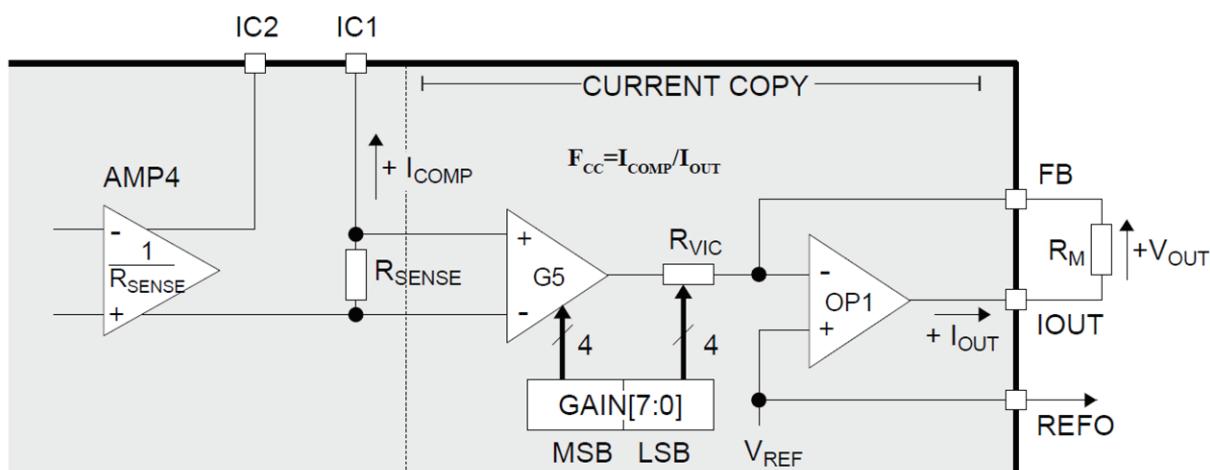


Fig. 6-4: Current copy schematic.

The programmable gain control realized as part of this block is distributed onto two 4-bit DACs:

- Most significant nibble GAIN[7:4] controls the gain of the differential amplifier G5 (“coarse gain trimming”).
- Least significant nibble GAIN[3:0] controls integrated resistor RVIC (“fine gain trimming”).

Due to this distributed concept for trimming of the gain, the DAC characteristic may be neither totally monotone nor strictly linear, but a maximum adjustment step LSBSX is defined which allows for a specified gain calibration precision.

Note:

For precision applications it is recommended to adjust the gain only after assembly of the sensor device to the application, where the distance and relation to the primary current coil are mechanically fixed.

### 6.2.2.3. Over-Current Alarm Output

For detection of an over-current violation two comparators are employed, which are observing the output level at pin IOUT. The over-current detection level is defined by the voltage level applied at pin SETTH. Both polarities of over-current are observed by this function, i.e. the over current alarm output N\_OVC is activated, whenever the absolute value of output current exceeds the limit defined by SETTH, as follows:

$$|I_{\text{OUT}}| = I_{\text{OUT},\text{max}} > \frac{V_{\text{REFO}}}{R_M} \cdot \left( 1 - \frac{V_{\text{SETTH}}}{V_{\text{REFO}}} \right) \rightarrow N_{\text{OVC}} \text{ activated (pulled to logic Low)}$$

(RM denotes the feedback resistor connected between pins IOUT and FB)

The detection level VSETTH is most efficiently defined by a resistive divider to pin REFO (see Fig. 1). A pull-up resistor RSETTH(PU) between SETH and REFO is integrated to cover cases where pin SETTH is high impedance erroneously ("open"). This would set the over-current threshold to zero, i.e. over-current alarm practically always on, and will avoid spontaneous alarm events generated at N\_OVC due to a floating detection threshold. In the timing diagram below the behavior of the over-current alarm and definition of the detection thresholds is shown.

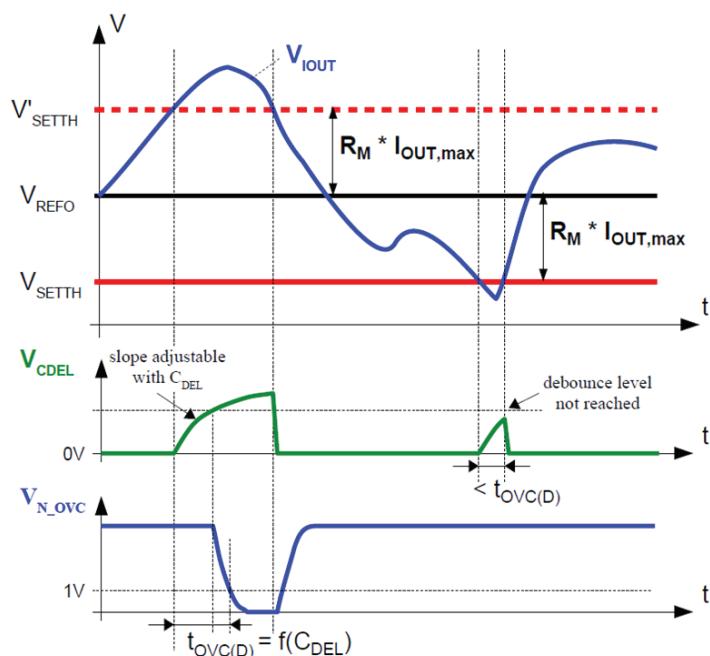


Fig. 6-5: Over-current alarm: thresholds and debounce behavior.

An additional debouncing delay which can be configured by connection of a capacitor to pin CDEL is implemented in the design of the over-current alarm. The delay can be calculated by the following approximation formula:

$$t_{\text{OVC}(D)} = t_{\text{OVC}(D,0)} + C_{\text{DEL}} (\text{pF}) \cdot \Delta t_{\text{OVC}(D)} \quad (\text{e.g. with } C_{\text{DEL}} = 50\text{pF}: t_{\text{OVC}(D)} \approx 0.5\mu\text{s} + 1.0\mu\text{s} = 1.5\mu\text{s})$$

Where  $t_{\text{OVC}(D,0)}$  is the intrinsic delay and  $\Delta t_{\text{OVC}(D)}$  the specific increase with a capacitor  $C_{\text{DEL}}$  connected (see Table 2). By this debouncing delay, alarm output events shorter than the delay time will be suppressed (not propagated to the alarm output N\_OVC). A maximum delay  $t_{\text{OVC}(D,F)}$  (integrated time-out) ensures an over-current event will be propagated to N\_OVC also in cases where CDEL is connected to GND erroneously.

Finally, an over-temperature event is logically combined (OR) to the alarm output N\_OVC (see Ch. 6.1.2.3). An over-temperature event can be distinguished from over-current, by the output IOUT at zero and N\_OVC pulled low.

The over-current alarm output is constructed as an open-drain driver as depicted in Fig. 6-6. Although a pull-up resistor  $R_{OVC(PU)}$  with quite high impedance is already integrated, it is recommended to use an external pull-up to the supply of the logic input connected (typically a few k $\Omega$ ) to ensure a fast reaction of the alarm output.

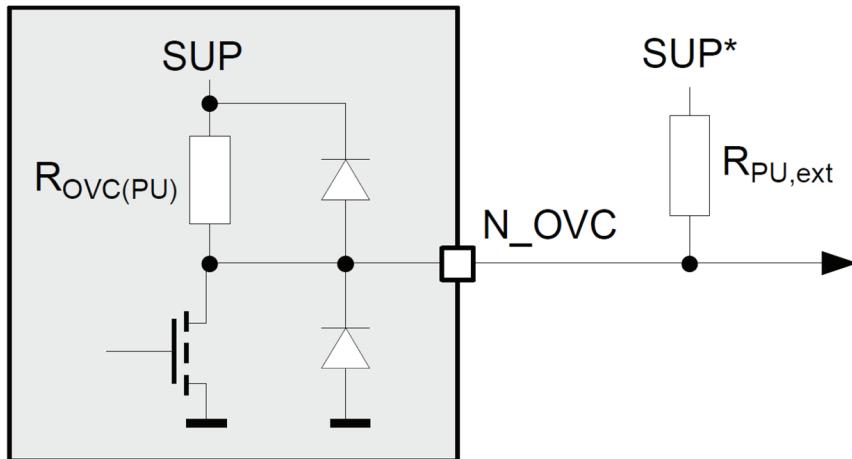


Fig. 6-6: Over-current output driver.

### 6.3. Typical Characteristics

The transfer function of the device is shown in Fig. 6-7. For time limits for the 2 time nominal resp. 3 time nominal primary current IP refer to chapter 5 (Recommended Operating Conditions).

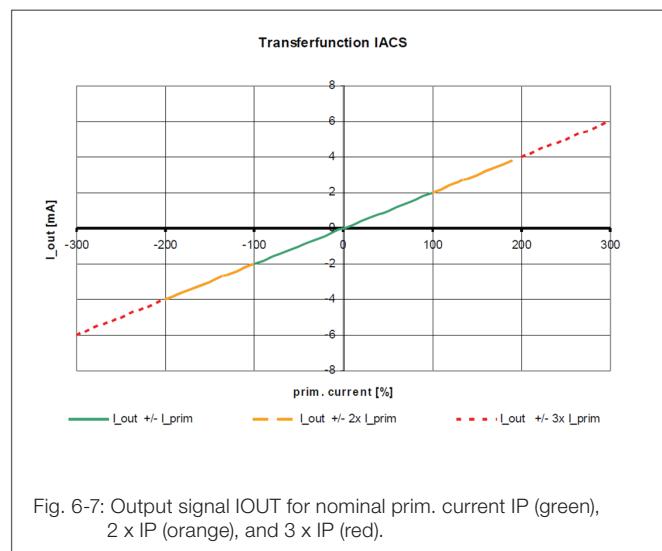


Fig. 6-7: Output signal  $I_{OUT}$  for nominal prim. current IP (green),  $2 \times IP$  (orange), and  $3 \times IP$  (red).

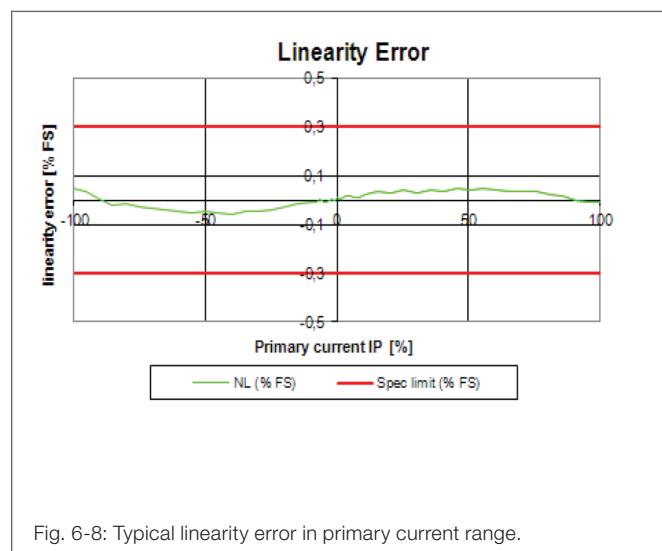


Fig. 6-8: Typical linearity error in primary current range.

Fig. 6-8 shows the typical measured linearity error of a 200 A application in % of the primary current. The red lines indicate the linearity sensitivity error specification limits from the section Electrical Parameters.

#### 6.4. Accuracy

The error bands for offset and sensitivity error are shown in Fig. 6-9 and Fig. 6-10. The deviations are referred to the values at 25°C.

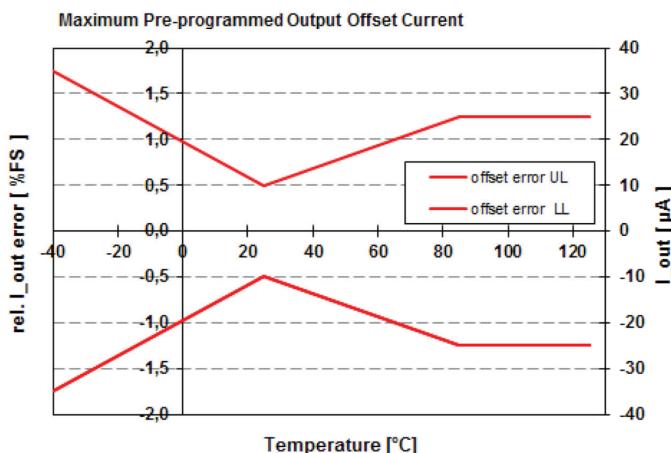


Fig. 6-9: Specified error bands for offset error. <sup>1)</sup>

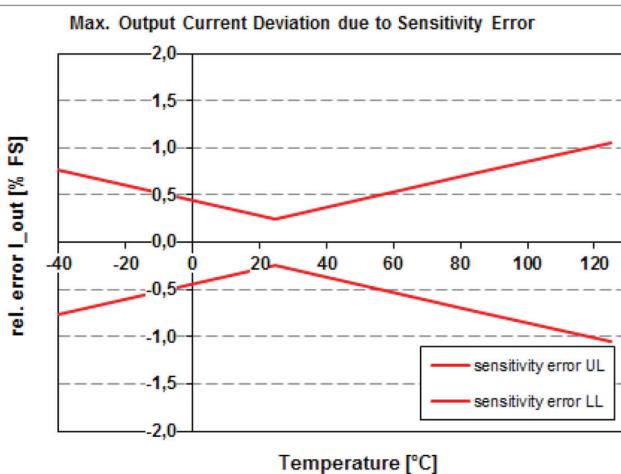


Fig. 6-10: Specified error bands due to sensitivity error. <sup>2)</sup>

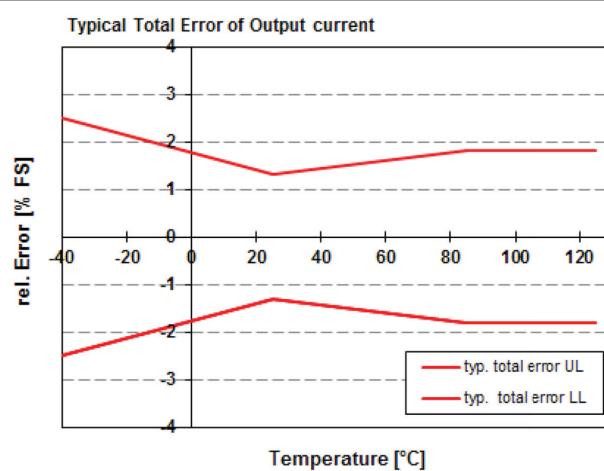


Fig. 6-11: Typical maximum range of total error after calibration. <sup>2),3)</sup>

Notes:

- 1) UL – upper limit / LL – lower limit).
- 2) Impact from thermal properties of application, eg. PCB materials not included.
- 3) Based on a weighted superposition of contributions from gain, offset, linearity and temperature dependance.

## 6.5 E<sup>2</sup>PROM

### 6.5.1 Electrical Parameters

( $V_{SUP} = 4.75V \dots 5.25V$ ,  $T_{AMB} = -40^{\circ}C \dots +125^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{SUP} = 5.0V$  and  $T_{AMB} = 25^{\circ}C$ . Positive currents are flowing into the device pins.)

Table 3: E<sup>2</sup>PROM data retention parameters

Symbol	Condition	Min.	Type	Max	Unit	Description
$N_{PROG}$	$TJ \leq 125^{\circ}C$ <sup>1)</sup>	1000			1	Number programming cycles
$t_{DR1}$	$TJ \leq 85^{\circ}C$	20			yr	data retention <sup>1) 2)</sup>
$t_{DR2}$	$85^{\circ}C \leq TJ \leq 105^{\circ}C$	3			yr	data retention <sup>1) 2)</sup>
$t_{DR3}$	$105^{\circ}C \leq TJ \leq 125^{\circ}C$	1			yr	data retention <sup>1) 2)</sup>
$t_{DR4}$	$125^{\circ}C \leq TJ \leq 150^{\circ}C$	500			h	data retention <sup>1) 2)</sup>

<sup>1)</sup> Defined by design. Not subject to production test. E<sup>2</sup>PROM is qualified according to AEC-Q100, grade 0.

<sup>2)</sup> Figures specified are guaranteed data retention times at the given temperature and must not be cumulated. For a specific temperature profile in operating life time (OLT), the specific exposure times for cumulation can be calculated on demand.

### 6.5.2 Description

The IC contains an E<sup>2</sup>PROM memory for application specific calibration data (GAIN & OFFSET) and further adjustment data (TC-Offset, and IC-specific adjustments). Only the lower 4 bytes (address 0x00h ... 0x03h) of this NVM are generally accessible via the ASIF (see section 6.6 ), while the addresses above 0x03h are read-only and cannot be modified after production test sequence.

After power-on, the E<sup>2</sup>PROM bytes for the adjustment information bits are read out and copied into the corresponding registers. The following table summarizes the memory mapping of the E<sup>2</sup>PROM (general accessible section):

Table 4: E<sup>2</sup>PROM register allocation

EEPROM address	Register name	Access	Description
0 x 00 h	FREE0	R/W	- unused register - (free use for application data)
0 x 01 h	FREE1	R/W	- unused register - (free use for application data)
0 x 02 h	OFFSET	R/W	Offset adjustment (8 bit), internal name: D_OS
0 x 03 h	GAIN	R/W	Sensitivity adjustment (8 bit)

## 6.6. Programming Interface and Digital Controls

### 6.6.1. Electrical Parameters

( $V_{SUP} = 4.75V \dots 5.25V$ ,  $T_{AMB} = -40^{\circ}C \dots +125^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{SUP} = 5.0V$  and  $T_{AMB} = 25^{\circ}C$ . Positive currents are flowing into the device pins.)

Table 5: Programming interface electrical parameters.

Symbol	Condition	Min.	Type	Max	Unit	Description
$R_{FB(PU)}$	ASIFEN=1	1.8	3.3	5.3	kΩ	ASIF pull-up resistor at FB
$V_{FB(N,Hi)}$	ASIFEN=1	4.0	-	VSUP	V	ASIF input Hi level at FB
$V_{FB(N,Lo)}$	ASIFEN=1	0.0	-	0.8	V	ASIF input Lo level at FB
$V_{FB(OUT,LO)}$	IFB = 1mA, ASIFEN=1	0.0	-	0.5	V	ASIF output Lo level at FB
$R_{rsv(PD)}$		14	20	26	kΩ	Pull-down resistor at pins rsv1, rsv3
$V_{rsv(Hi)}$		4.1	-	VSUP	V	Digital input Hi level at pins rsv1, rsv3
$V_{rsv(Lo)}$			-	0.8	V	Digital input Lo level at pins rsv1, rsv3
$t_{IF_DLY}$	Rising edge rsv1 / rsv3 to 1st falling edge at FB see fig. 6-15 <sup>1)</sup>	110	-	-	μs	Delay between enabling ASIF (ASIFEN = 1) via rsv1 / rsv3 and start of 1st protocol
$C_{FB(LD)}$	<sup>1)</sup>		-	150	pF	Load capacitance during ASIF-operation (interface)
$t_{BIT_RX}$	see fig. 6-16	85	100	115	μs	Valid ASIF bit length for receiving at pin FB
$t_{HBIT_RX}$	see fig. 6-16	0.45	0.50	0.55	tBIT_RX	Valid ASIF half bit length for receiving
$t_{RX}$	see fig. 6-18	- (0.94)	11 (1.10)	- (1.26)	tBIT_RX (ms)	Length of valid receiving protocol
$t_{BIT_TX}$	see fig. 6-16	90	100	110	μs	ASIF bit length for transmitting at pin FB
$t_{HBIT_TX}$	see fig. 6-16	0.47 (42)	0.50 (50)	0.53 (59)	tBIT_TX (μs)	ASIF half bit length for transmitting
$t_{TX}$	see fig. 6-18	- (0.98)	11 (1.10)	- (1.22)	tBIT_TX (ms)	Length of transmission protocol
$t_{FB_rise}$	from 20% to 80% <sup>1)</sup>	-	-	2	μs	Digital input rise time at pin FB for RX and TX
$t_{FB_fall}$	from 80% to 20% <sup>1)</sup>	-	-	2	μs	Digital input fall time at pin FB for RX and TX
$t_{RX_DLY}$	see fig. 6-18	3 (330)	-	-	tBIT_TX (μs)	Valid delay between reception of two protocols
$t_{TX_DLY}$	see fig. 6-18	2 (180)	-	3 (330)	TBIT_TX (μs)	Delay between command protocol and response
$t_{PRG_DLY}$	see fig. 6-18	16	-	21	ms	Delay between data protocol and confirmation protocol after programming

<sup>1)</sup> Defined by design. Not subject to production test.

## 6.6.2. Description

A digital state machine controls the complete IC and provides the following functions:

- ASIF (asynchronous serial interface) as data interface for calibration in the application and data read-back
- E<sup>2</sup>PROM control (NVM for storage of calibration data)
- Read-out of calibration data from E<sup>2</sup>PROM to the corresponding registers after power-on
- Control of the test interface and test modes (production test; restricted access)

This chapter concentrates on the description of the ASIF and its use as the most important feature for the application of the CFS1000. Because this interface uses the pin FB as digital I/O it is not possible to run the normal sensor application simultaneously in the programming mode via ASIF. This implies, the calibration measurements required to determine the calibration data (GAIN, OFFSET) need to be done in a sequence with the data I/O via ASIF.

### 6.6.2.1. Calibration Adjustment

For the specified precision of the AMR current sensor in its application environment, the IC CFS1000 needs adjustment. Therefore, the respective adjustment data are stored during the calibration process in an integrated E<sup>2</sup>PROM (non-volatile memory = NVM).

The adjustment can only partially be done before packaging or assembly of the device into its application environment. Especially the GAIN-adjustment determining the precise sensitivity of the CFS1000 is recommended to be executed after soldering the device in order to ensure precise mechanical fixing with respect to the primary current conductor. Optionally, also the final trimming of the OFFSET can be done in this phase, while other calibration data (e.g. thermal coefficient of the offset) are completely performed during the sensor production test sequence.

For E<sup>2</sup>PROM programming an asynchronous serial interface (ASIF) is implemented, which uses the pin FB as a bidirectional digital-I/O. To enter the interface mode (ASIFEN = 1: "interface enabled") just after power-on during a certain time interval an ASIF-command has to be sent to FB. This interval with ASIFEN=1 opens after  $t_{INIT}$  for the login time  $t_{ASIFEN}$  (see Fig. 6-2, Table 1) and the login command (0xD5, see Table 6) has to be transmitted completely in this interval. In the time directly after power-on the pin FB does not operate as an analog I/O as described above (Section 6.2.2.2), but as a digital I/O with an integrated pull-up  $R_{FB(PU)}$ . If the IC is transmitting, an open-drain low-side driver is employed to drive the logic Low level (Fig. 15). A similar structure is recommended to drive data the ASIF (receive-mode RX).

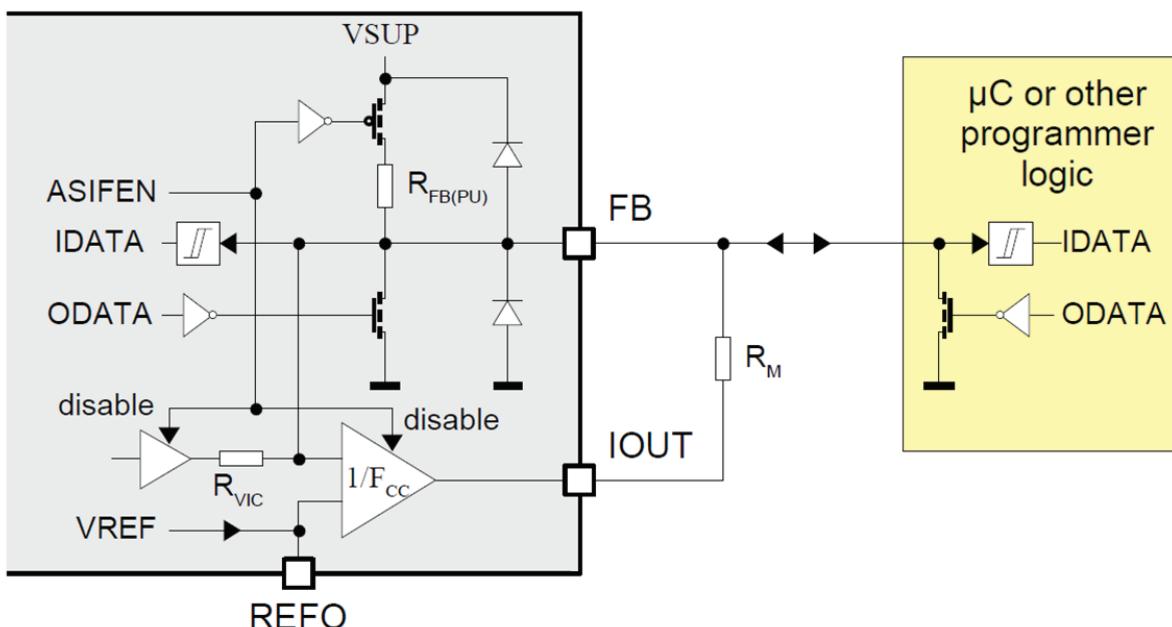


Fig. 6-12: Asynchronous serial interface (ASIF), circuit concept.

Because of the low-impedance connection between FB and IOUT in the application circuit (normal sensor operation), also the output driver at IOUT is switched to high impedance during “ASIF active” (ASIFEN=1) to allow for safe data transmission into FB (RX-mode). In Fig.16 below an exemplary application circuit is depicted which can be employed to adjust the CFS1000 via ASIF.

Because this interface uses the pin FB, it is not possible to operate simultaneously the normal sensor application mode during ASIF-programming mode and vice versa. Because log-in to ASIF mode is possible only after power-on a quite fast reset, which is operated synchronously to the external programming logic is needed.

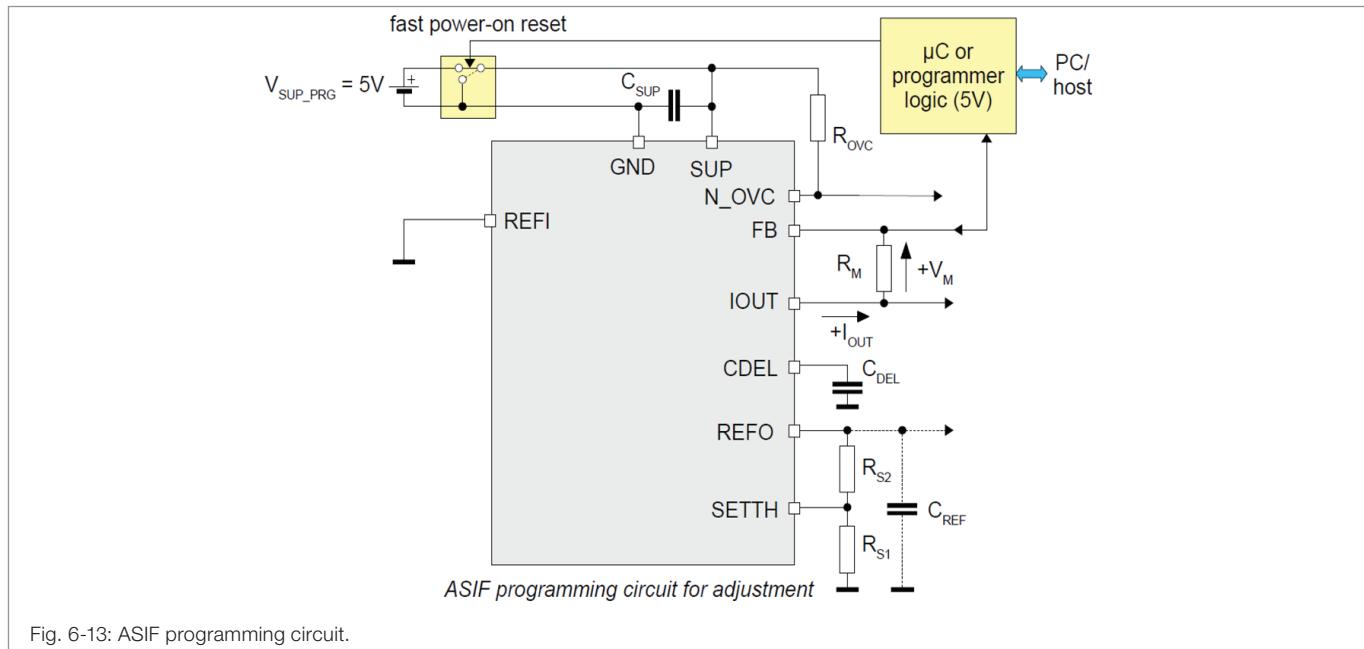


Fig. 6-13: ASIF programming circuit.

If also access to the test interface pins rsv1, rsv3 is available, the alternative programming circuit example depicted in Fig. 17 should be used. Rather than using a power-on reset via supply pin SUP, to enable the ASIF the pins rsv1 and rsv3 need to be pulled to logic high level simultaneously.

On the other hand, the pull-up of pins rsv1 and rsv3 has to be avoided imperatively during normal operation, because it would immediately affect the regular analog circuit function at pins IOUT / FB.

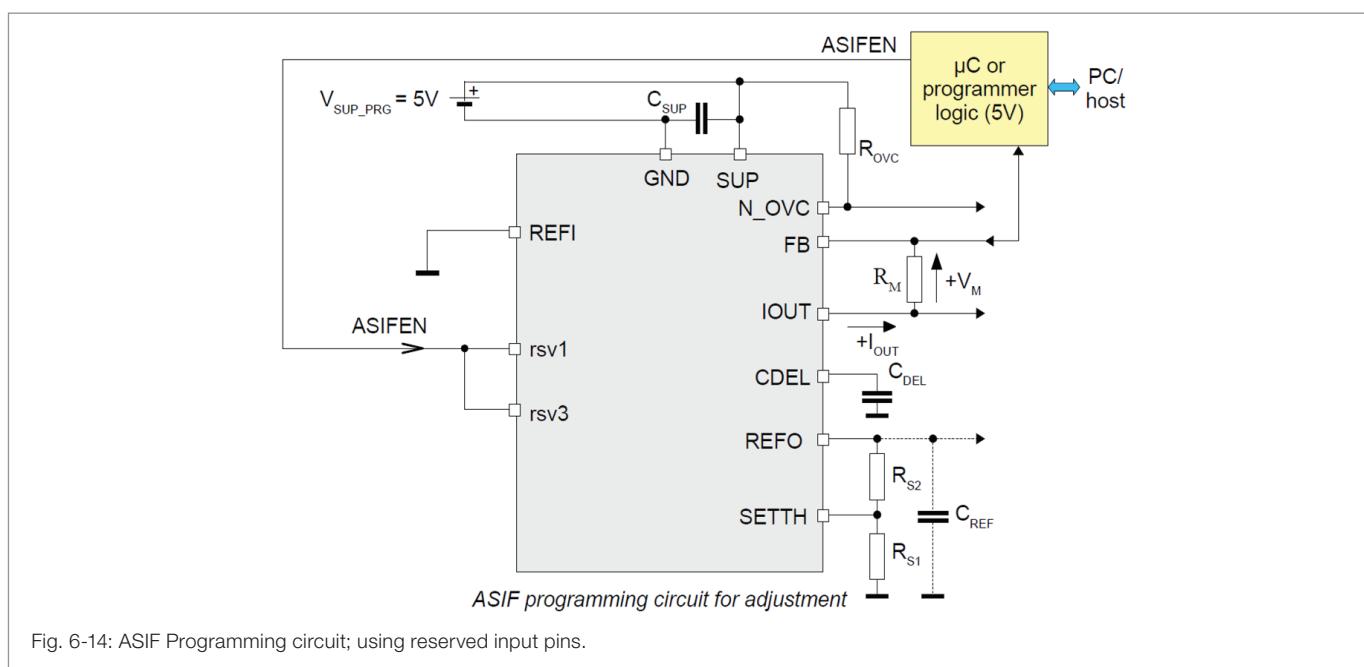


Fig. 6-14: ASIF Programming circuit; using reserved input pins.

In Fig. 6-15 below the log-in timing to enter ASIF-mode is depicted when access to pins rsv1 and rsv3 is possible. No restricted time interval after power-on needs to be observed here, but only a minimum wait time  $t_{IF\_DLY}$  before data transmission may start is to be ensured. The ASIF remains active as long as pins rsv1 and rsv3 are kept at logic high level.

During data communication via ASIF the load capacity  $C_{FB(LD)}$  at pin FB must be limited to meet the specified timing (see Table 5).

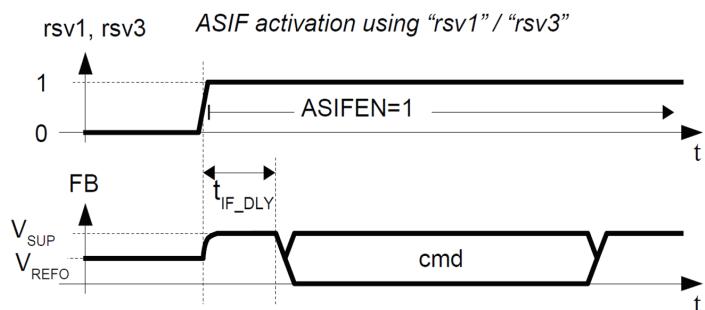


Fig. 6-15: Log-in to ASIF with access to pins rsv1 and rsv3.

### 6.6.2.2 ASIF Protocol and Encoding

This sub-chapter describes the bit coding and the protocol construction of the ASIF.

Manchester coding is used for data transmission as shown in Fig. 6-16. The necessary timing parameters for receive (RX) and transmit (TX) are specified as  $t_{BIT\_RX/TX}$ ,  $t_{HBIT\_RX/TX}$ ,  $t_{rise}$  and  $t_{fall}$  (see Table 6).

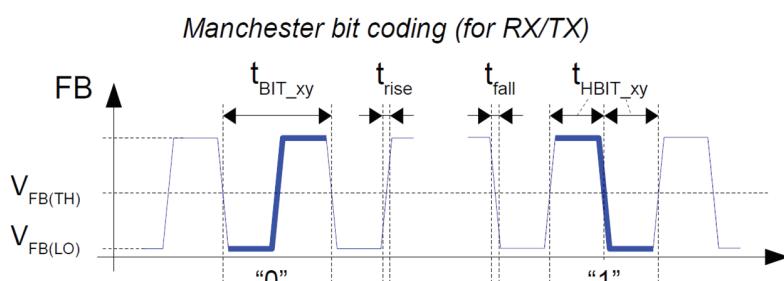


Fig. 6-16: Manchester bit coding and bit timing for transmit and receive.

The transmission protocol consists of 11 bits in total: 2 start-bits followed by 8 data bits or command bits, and 1 parity bit which indicates the end of a protocol. The command or data byte within the protocol starts with MSB first. An example for read out of an ID-byte is shown in the picture below (Fig. 6-17).

In case of a parity failure (i.e. no odd parity detected within all 11 bits), or a start-bit-error, or any other error be detected, within a protocol frame, the protocol will be ignored.

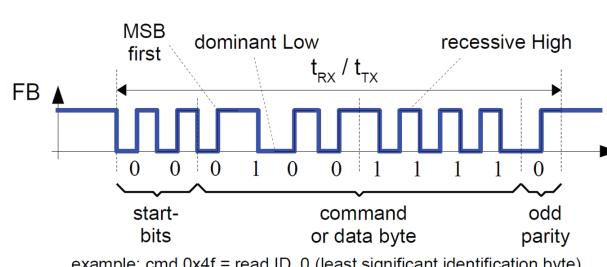


Fig. 6-17: ASIC protocol format and example.

### 6.6.2.3 ASIF Commands

The ASIF-commands consist of a sequence of 2 or 3 interface protocols as described in the last section. Two general types of ASIF-commands are depicted in fig. 6-18 below.

Each ASIF-command starts with a command byte send from an external logic to the CFS1000. In the first command format shown in Fig. 6-18 the IC response contains the requested data, or a confirmation data byte, if no data requested.

The second command format is used for E<sup>2</sup>PROM programming. Here, the command includes the E<sup>2</sup>PROM address and is followed by the data byte to be programmed to the E<sup>2</sup>PROM of the CFS1000. After an interval tPRG\_DLY required for E<sup>2</sup>PROM-programming, the IC transmits the data byte read back from the corresponding E<sup>2</sup>PROM address to the programming module externally connected at the ASIF interface.

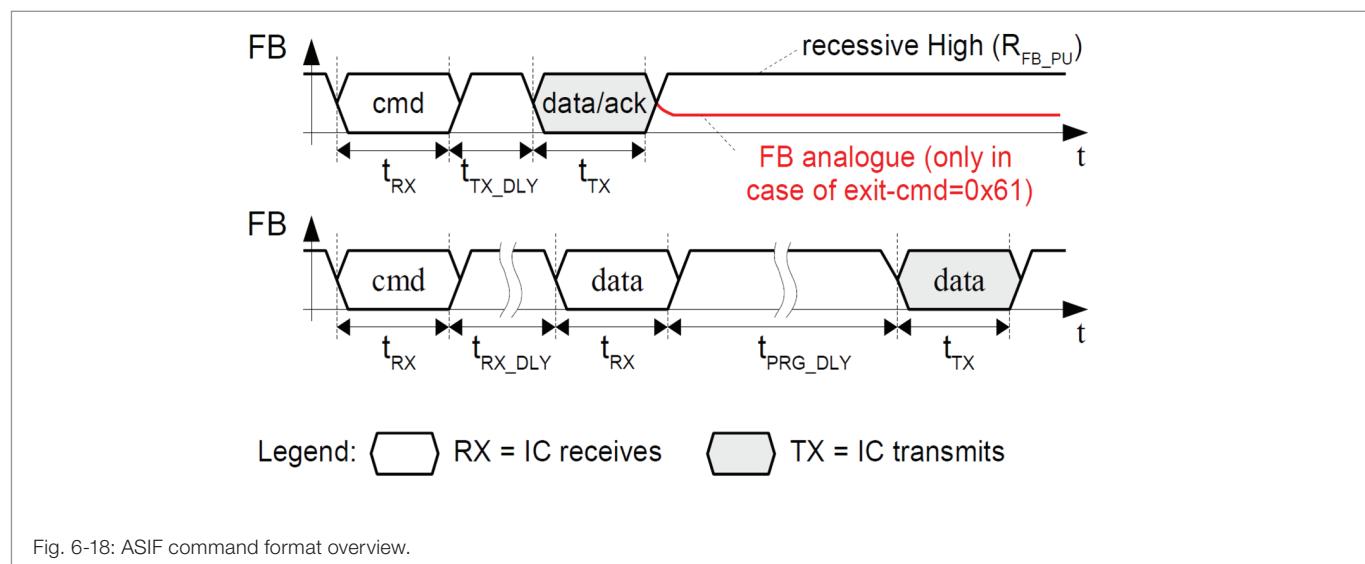


Fig. 6-18: ASIF command format overview.

The specified time delays tTX , tRX , tPRG\_DLY , tTX\_DLY , and tRX\_DLY (see Table 5) have to be considered for proper communication in order to avoid the pin FB is driven simultaneously from the external and the integrated transmitter. Hard driver conflicts are avoided by defining this interface as Low dominant / High recessive, i.e. open-drain drivers with pull-up resistor.

The table below summarizes the ASIF-commands which are implemented in CFS1000.

Table 6: ASIF-commands overview:

Code	ASIF-instruction	next I/O-operation	3rd I/O-operation
0x4Y	read E <sup>2</sup> PROM address <Y> <sup>1)</sup>	TX read out data byte	none
0x51	write unused E <sup>2</sup> PROM byte	RX data byte to program	TX read back data byte
0x52	write OFFSET	RX data byte to program	TX read back data byte
0x53	write GAIN	RX data byte to program	TX read back data byte
0x60	update all adjustment registers from E <sup>2</sup> PROM	TX confirmation data byte 0x00	none
0x61	exit programming mode to application mode	TX confirmation data byte 0x01	none
0xD5	log-in to programming mode	TX confirmation data byte 0x05	none (programming mode is entered, FB at "High" with pull-up)
all other	(undefined command)	TX confirmation data byte 0xE1 or 0xE2 <sup>2)</sup>	none

<sup>1)</sup> Wildcard "Y" stands for any address 0x00 ... 00xF of the E<sup>2</sup>PROM memory map (see Table 4).

<sup>2)</sup> Depending on the code of the "undefined command", two different error codes are sent.

Legend: TX = transmit from IC to external modules; RX = CFS1000 receives protocol data.

## 7. Package Information

The CFS1000 is available in a Pb free, RoHs compliant, SO16 plastic package according to JEDEC MS-013-E, variant AA.

The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260 + 5)°C.

Note: Thermal resistance junction to ambient RTH,JA is 80 °C/W, based on standard JESD-51-7.

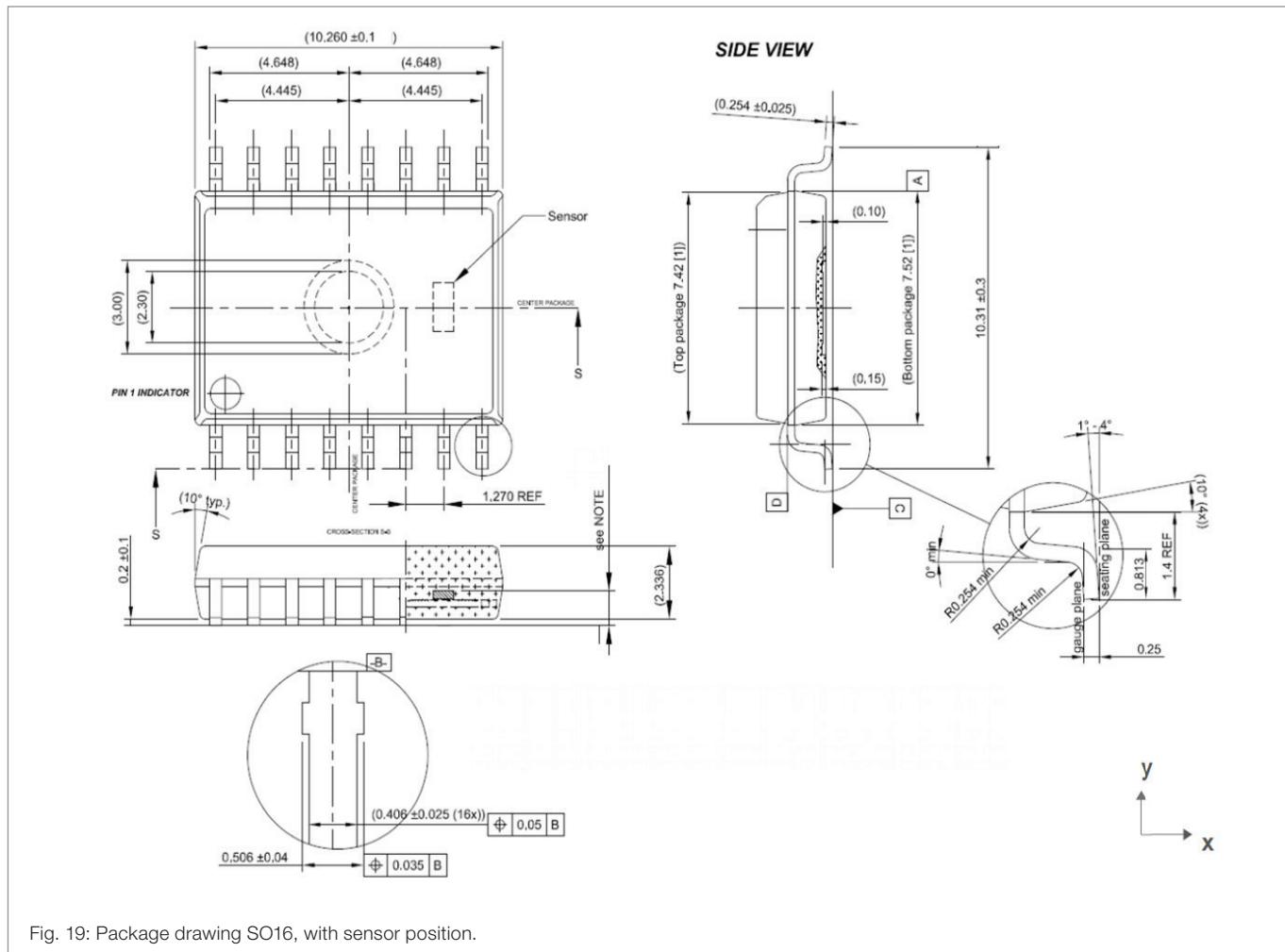


Fig. 19: Package drawing SO16, with sensor position.

### Notes:

- All Dimensions in mm
- Position of sensitive area in x is indicated by connecting line between pins 7 and 10; position in y is centered around the middle axis of the package, vertical position of sensitive area is typically 1.1 mm above seating plane of the package.

## 8. Customer Specific Marking

Table 7: CFS1000 Top side marking content

Top side marking content
--------------------------

 CFS1000AAA  
XXXPPPZZEYYWW

where

Signature	Explanation
E / M / T	Volume production / prototype / test circuit
CFS1000AAA	Product name
XXX	Order number
PPP	Production lot number
ZZ	Assembly subplot code
E	Assembler code
YYWW	Year and week of assembly

## General Information

### Product Status

Article	Status
CFS1000 AAA-AE	The product is under development, qualification is on going. Deliverables have a sample status. The datasheet is preliminary.
Note	The status of the product may have changed since this data sheet was published. The latest information is available on the internet at <a href="http://www.sensitec.com">www.sensitec.com</a> .

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### Sensitec GmbH

Georg-Ohm-Str. 11 · 35633 Lahnau · Germany  
Tel. +49 6441 9788-0 · Fax +49 6441 9788-17  
[www.sensitec.com](http://www.sensitec.com) · [sensitec@sensitec.com](mailto:sensitec@sensitec.com)

