# **HEF4543B**

# BCD to 7-segment latch/decoder/driver Rev. 05 — 27 October 2009

Product data sheet

#### General description 1.

The HEF4543B is a BCD to 7-segment latch/decoder/driver for liquid crystal and LED displays. It has four address inputs (D0 to D3), an active LOW latch enable input (LE), an active HIGH blanking input (BL), an active HIGH phase input (PH) and seven buffered segment outputs (Qa to Qg).

The circuit provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder/driver. It can invert the logic levels of the output combination. The phase (PH). blanking (BL) and latch enable ( $\overline{\text{LE}}$ ) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays, a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the device are directly connected to the segments of the liquid crystal.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$ (usually ground). Unused inputs must be connected to VDD, VSS, or another input. It is also suitable for use over the full industrial (-40 °C to +85 °C) temperature range.

#### 2. **Features**

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the full industrial temperature range -40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

# **Applications**

Industrial

#### 4. Ordering information

#### Table 1. **Ordering information**

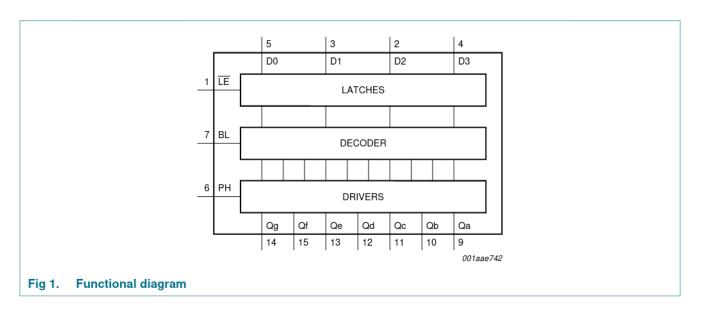
All types operate from -40 °C to +85 °C

Type number	Package	Package							
	Name	Description	Version						
HEF4543BP	DIP16	plastic dual in-line package; 16-leads (300 mil)	SOT38-4						
HEF4543BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1						

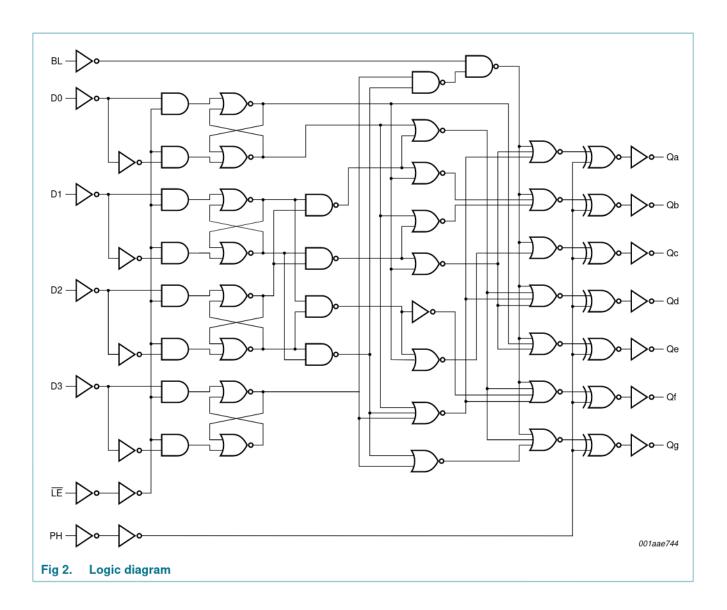


BCD to 7-segment latch/decoder/driver

# 5. Functional diagram



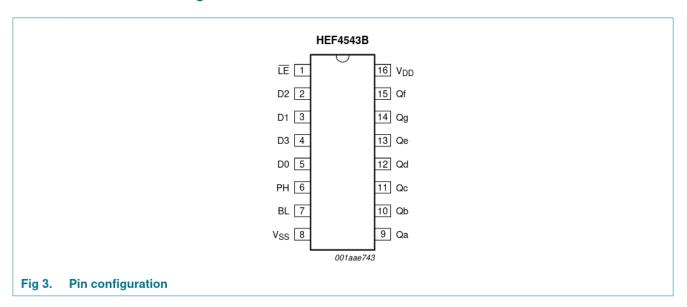
# BCD to 7-segment latch/decoder/driver



# BCD to 7-segment latch/decoder/driver

# 6. Pinning information

# 6.1 Pinning



# 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
LE	1	latch enable input (active LOW)
D0 to D3	5, 3, 2, 4	address (data) input
PH	6	phase input (active HIGH)
BL	7	blanking input (active HIGH)
V <sub>SS</sub>	8	ground supply voltage
Qa to Qg	9, 10, 11, 12, 13, 15, 14	segment output
$V_{DD}$	16	supply voltage

# BCD to 7-segment latch/decoder/driver

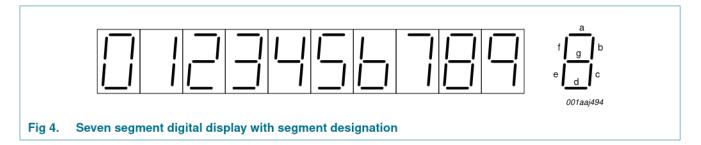
# 7. Functional description

Table 3. Function table [1]

Input	s						Outp	uts						
LE	BL	PH [2]	D3	D2	D1	D0	Qa	Qb	Qc	Qd	Qe	Qf	Qg	Display
Χ	Н	L	Χ	Χ	Χ	Χ	L	L	L	L	L	L	L	blank
Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	L	0
Н	L	L	L	L	L	Н	L	Н	Н	L	L	L	L	1
Н	L	L	L	L	Н	L	Н	Н	L	Н	Н	L	Н	2
Н	L	L	L	L	Н	Н	Н	Н	Н	Н	L	L	Н	3
Н	L	L	L	Н	L	L	L	Н	Н	L	L	Н	Н	4
Н	L	L	L	Н	L	Н	Н	L	Н	Н	L	Н	Н	5
Н	L	L	L	Н	Н	L	Н	L	Н	Н	Н	Н	Н	6
Н	L	L	L	Н	Н	Н	Н	Н	Н	L	L	L	L	7
Н	L	L	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	8
Н	L	L	Н	L	L	Н	Н	Н	Н	Н	L	Н	Н	9
Н	L	L	Н	L	Н	Χ	L	L	L	L	L	L	L	blank
Н	L	L	Н	Н	Χ	Χ	L	L	L	L	L	L	L	blank
L	L	L	Χ	Χ	Χ	Χ	n.c.							n.c
as ab	ove	Н	as ab	ove			invers	se of abo	ove					as above

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level; X = don't care,: n.c. = no change.

<sup>[2]</sup> For liquid crystal displays, apply a square-wave to PH; For common cathode LED displays, select PH = LOW; For common anode LED displays, select PH = HIGH.



# 8. Limiting values

### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$V_{I}$	input voltage		-0.5	$V_{DD} + 0.5$	V
I <sub>I/O</sub>	input/output current		-	±10	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+85	°C

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# BCD to 7-segment latch/decoder/driver

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
P <sub>tot</sub>	total power dissipation	DIP16 package	<u>[1]</u> -	750	mW
		SO16 package	[2] _	500	mW
Р	power dissipation	per output	-	100	mW

<sup>[1]</sup> For DIP16 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.

# 9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_{I}$	input voltage		0	-	$V_{DD}$	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5 V$	-	-	3.75	∝s/V
		$V_{DD} = 10 \text{ V}$	-	-	0.5	∝s/V
		$V_{DD} = 15 \text{ V}$	-	-	0.08	∝s/V

# 10. Static characteristics

Table 6. Static characteristics

 $V_{SS} = 0 \ V$ ;  $V_I = V_{SS} \ or \ V_{DD} \ unless \ otherwise \ specified.$ 

Symbol	Parameter	Conditions	$V_{DD}$	T <sub>amb</sub> =	–40 °C	T <sub>amb</sub> =	25 °C	T <sub>amb</sub> = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
$V_{\text{IH}}$	HIGH-level input voltage	I <sub>O</sub>   < 1 ∝A	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V <sub>IL</sub> LOW-level input voltage	LOW-level input voltage	$ I_O  < 1 \propto A$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V <sub>OH</sub> HIGH-level output voltage			5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	I <sub>O</sub>   < 1 ∝A	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_{O} = 2.5 \text{ V}$	5 V	-1.7	-	-1.4	-	-1.1	-	mA
		$V_{O} = 4.6 \text{ V}$	5 V	-0.52	-	-0.44	-	-0.36	-	mA
		$V_{O} = 9.5 \text{ V}$	10 V	-1.3	-	-1.1	-	-0.9	-	mA
		$V_{O} = 13.5 \text{ V}$	15 V	-3.6	-	-3.0	-	-2.4	-	mA

<sup>[2]</sup> For SO16 package: Ptot derates linearly with 8 mW/K above 70 °C.

# BCD to 7-segment latch/decoder/driver

Table 6. Static characteristics ...continued

 $V_{SS} = 0$  V;  $V_{I} = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	T <sub>amb</sub> =	-40 °C	T <sub>amb</sub> =	25 °C	T <sub>amb</sub> = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
$I_{OL}$	LOW-level output current	$V_0 = 0.4 \ V$	5 V	0.52	-	0.44	-	0.36	-	mA
	$V_{O} = 0.5 V$	10 V	1.3	-	1.1	-	0.9	-	mΑ	
		$V_{O} = 1.5 V$	15 V	3.6	-	3.0	-	2.4	-	mΑ
II	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	∝A
$I_{DD}$	supply current	$I_O = 0 A$	5 V	-	20	-	20	-	150	∝A
			10 V	-	40	-	40	-	300	∝A
			15 V	-	80	-	80	-	600	∝A
$C_{I}$	input capacitance		-	-	-	-	7.5	-	-	рF

# 11. Dynamic characteristics

Table 7. Dynamic characteristics

 $V_{SS} = 0 \ V; T_{amb} = 25 \ ^{\circ}C;$  For test circuit see <u>Figure 7</u>;unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula[1]	Min	Тур	Max	Unit
t <sub>PHL</sub>	HIGH to LOW	Dn to Qn;	5 V	153 ns + (0.55 ns/pF) $C_L$	-	180	360	ns
	propagation delay	see Figure 5	10 V	64 ns + (0.23 ns/pF) C <sub>L</sub>	-	75	150	ns
			15 V	47 ns + (0.16 ns/pF) C <sub>L</sub>	-	55	110	ns
		LE to Qn;	5 V	143 ns + (0.55 ns/pF) C <sub>L</sub>	-	170	340	ns
		see Figure 5	10 V	69 ns + (0.23 ns/pF) $C_L$	-	80	160	ns
		15 V	52 ns + (0.16 ns/pF) $C_L$	-	60	120	ns	
		BL to Qn;	5 V	118 ns + (0.55 ns/pF) C <sub>L</sub>	-	145	290	ns
		see Figure 5	10 V	54 ns + (0.23 ns/pF) $C_L$	-	65	130	ns
		15 V	$37 \text{ ns} + (0.16 \text{ ns/pF}) \text{ C}_{\text{L}}$	-	45	90	ns	
$t_{PLH}$	PLH LOW to HIGH propagation delay	Dn to Qn;	5 V	153 ns + (0.55 ns/pF) $C_L$	-	180	360	ns
		see <u>Figure 5</u>	10 V	64 ns + (0.23 ns/pF) $C_L$	-	75	150	ns
			15 V	47 ns + (0.16 ns/pF) $C_L$	-	55	110	ns
		LE to Qn;	5 V	163 ns + (0.55 ns/pF) $C_L$	-	190	380	ns
		see <u>Figure 5</u>	10 V	69 ns + (0.23 ns/pF) $C_L$	-	80	160	ns
			15 V	52 ns + (0.16 ns/pF) $C_L$	-	60	120	ns
		BL to Qn;	5 V	98 ns + (0.55 ns/pF) $C_L$	-	125	250	ns
		see Figure 5	10 V	54 ns + (0.23 ns/pF) $C_L$	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF) $C_L$	-	40	80	ns
t <sub>t</sub>	transition time	pin Qn;	5 V	10 ns + (1.00 ns/pF) $C_L$	-	60	120	ns
		see Figure 5	10 V	9 ns + (0.42 ns/pF) $C_L$	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF) $C_L$	-	20	40	ns
t <sub>su</sub>	set-up time	Dn to LE;	5 V		40	20	-	ns
		see Figure 6	10 V		20	5	-	ns
			15 V		15	0	-	ns

### BCD to 7-segment latch/decoder/driver

Table 7. Dynamic characteristics ...continued

 $V_{SS}$  = 0 V;  $T_{amb}$  = 25 °C; For test circuit see Figure 7;unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula <sup>[1]</sup>	Min	Тур	Max	Unit
$t_h$	hold time	$D_n$ to $\overline{LE}$ ;	5 V		0	-15	-	ns
		see Figure 6	10 V		15	0	-	ns
			15 V		20	5	-	ns
$t_W$	pulse width	pin LE HIGH; minimum width; see <u>Figure 6</u>	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns

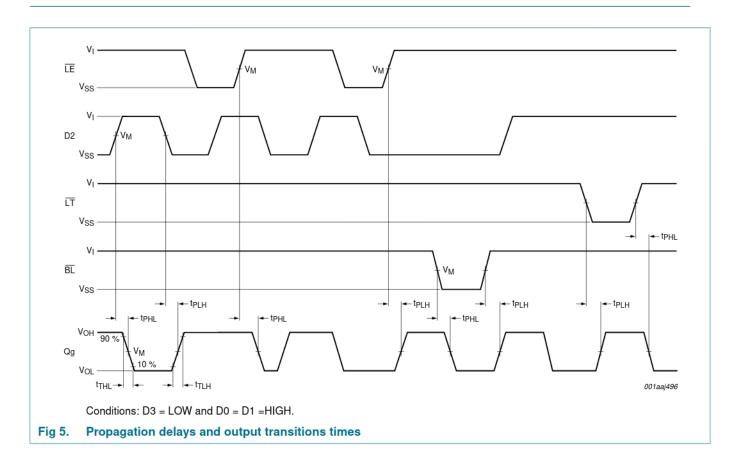
<sup>[1]</sup> The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C<sub>L</sub> in pF).

Table 8. Dynamic power dissipation P<sub>D</sub>

 $P_D$  can be calculated from the formulas shown.  $V_{SS} = 0$  V;  $t_r = t_f \le 20$  ns;  $T_{amb} = 25$  °C.

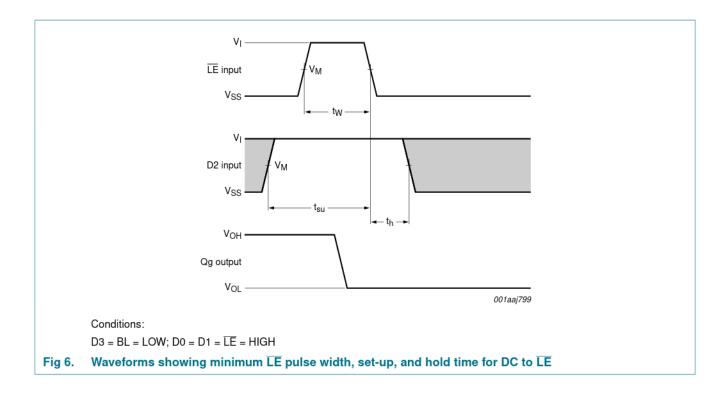
Symbol	Parameter	$V_{DD}$	Typical formula for P <sub>D</sub> (∝W)	where:
$P_{D}$	dynamic power	5 V	$P_D = 2200  \cdot  f_i + \Sigma (f_o  \cdot  C_L)  \cdot  V_{DD}{}^2$	$f_i$ = input frequency in MHz,
	dissipation	10 V	$P_D = 10400  \cdot  f_i + \Sigma (f_o  \cdot  C_L)  \cdot  V_{DD}{}^2$	fo = output frequency in MHz,
		15 V	$P_D = 33000 ~\cdot~ f_i + \Sigma (f_o ~\cdot~ C_L) ~\cdot~ V_{DD}{}^2$	$C_L$ = output load capacitance in pF,
				$V_{DD}$ = supply voltage in V,
				$\Sigma(C_L \cdot f_0)$ = sum of the outputs.

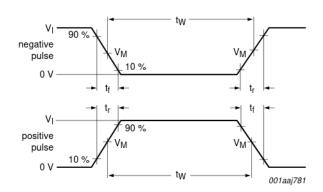
# 12. Waveforms



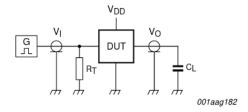
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# BCD to 7-segment latch/decoder/driver





### a. Input waveforms



#### b. Test circuit

Test data is given in Table 9.

Definitions for test circuit:

R<sub>L</sub> = Load resistance;

C<sub>L</sub> = Load capacitance including jig and probe capacitance;

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig 7. Test circuit for switching times

Table 9. Test data

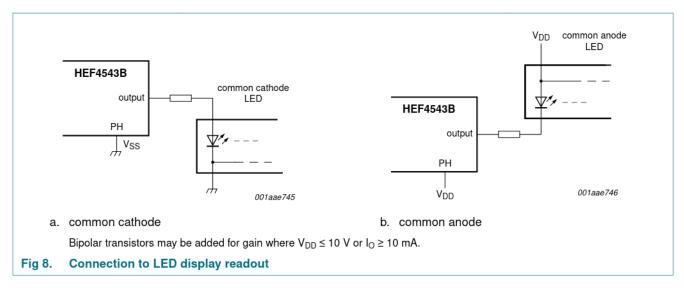
Supply voltage	Input	Load		
	VI	V <sub>M</sub>	t <sub>r</sub> , t <sub>f</sub>	CL
5 V to 15 V	$V_{DD}$	0.5V <sub>1</sub>	≤ 20 ns	50 pF

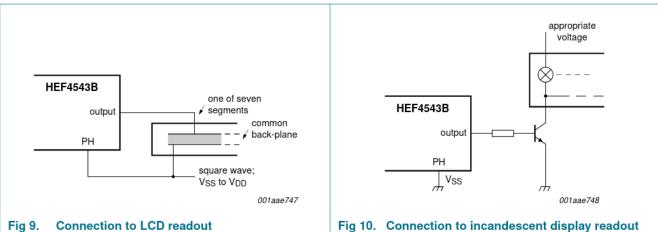
# 13. Application information

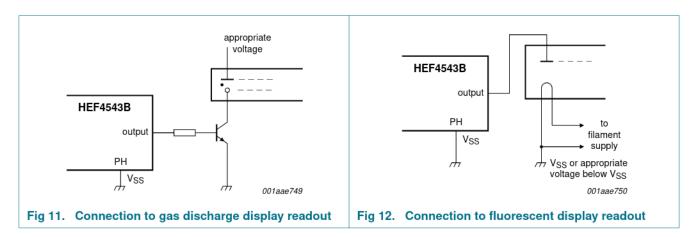
Some examples of applications for the HEF4543B are:

- · Driving LCD displays
- · Driving LED displays
- · Driving fluorescent displays
- · Driving incandescent displays
- · Driving gas discharge displays

### BCD to 7-segment latch/decoder/driver



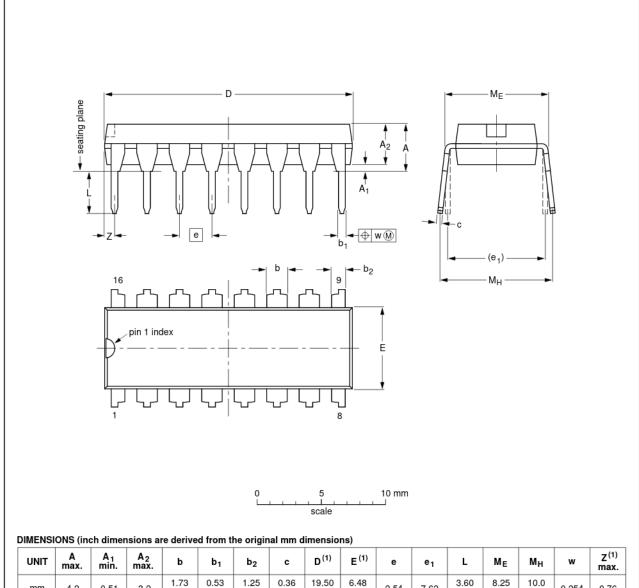




# 14. Package outline

# DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	e <sub>1</sub>	L	ME	Мн	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

### Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT38-4						<del>95-01-14</del> 03-02-13	

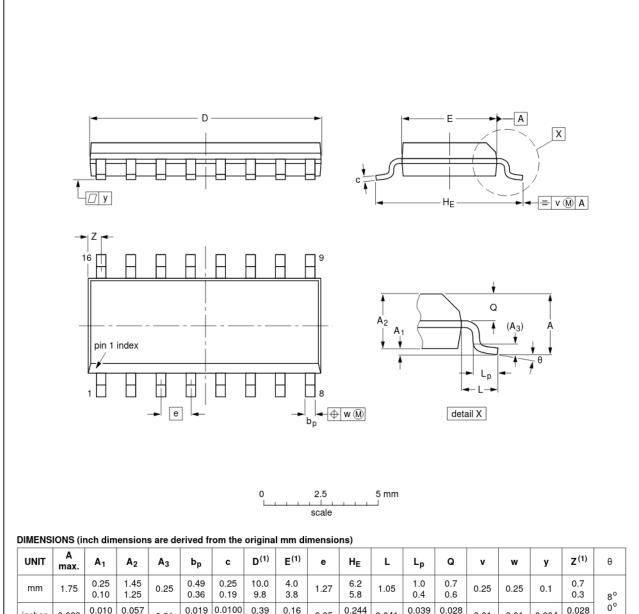
Fig 13. Package outline SOT38-4 (DIP16)

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**HEF4543B NXP Semiconductors** 

# SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075		0.16 0.15	0.05	0.244 0.228	0.041		0.028 0.020	0.01	0.01	0.004	0.028 0.012	0°

### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT109-1	076E07	MS-012				<del>99-12-27</del> 03-02-19	

Fig 14. Package outline SOT109-1 (SO16)

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# BCD to 7-segment latch/decoder/driver

# 15. Abbreviations

### Table 10. Abbreviations

Acronym	Description
DUT	Device Under Test

# 16. Revision history

# Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4543B_5	20091027	Product data sheet	-	HEF4543B_4
Modifications:	Section 9 "F	Features" ESD entry remove Recommended operating co "Abbreviations" ESD entries	nditions" Δt/ΔV values ι	updated.
HEF4543B_4	20090317	Product data sheet	-	HEF4543B_CNV_3
HEF4543B_CNV_3	19950101	Product specification	-	HEF4543B_CNV_2
HEF4543B_CNV_2	19950101	Product specification	-	-

### BCD to 7-segment latch/decoder/driver

# 17. Legal information

### 17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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**HEF4543B NXP Semiconductors** 

# BCD to 7-segment latch/decoder/driver

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