Dependency of Transient Current Behavior on Oxide Thickness in Trench Structure MIS TDs

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Presenter: Jian-Yu Lin

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Outline

- **Introduction**
  - ➢**Metal-Insulator-Semiconductor Tunnel Diode (MIS TD)**
  - ➢**Transient Current in MIS TDs**
- **Results and Discussion**
  - ➢**Experiments**
  - ➢**TCAD Simulation**
- **Conclusion**

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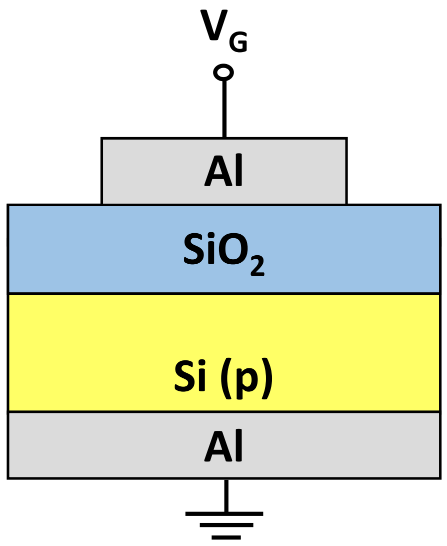
What is MIS TD?

***Metal-insulator-semiconductor tunnel diode (MIS TD)**

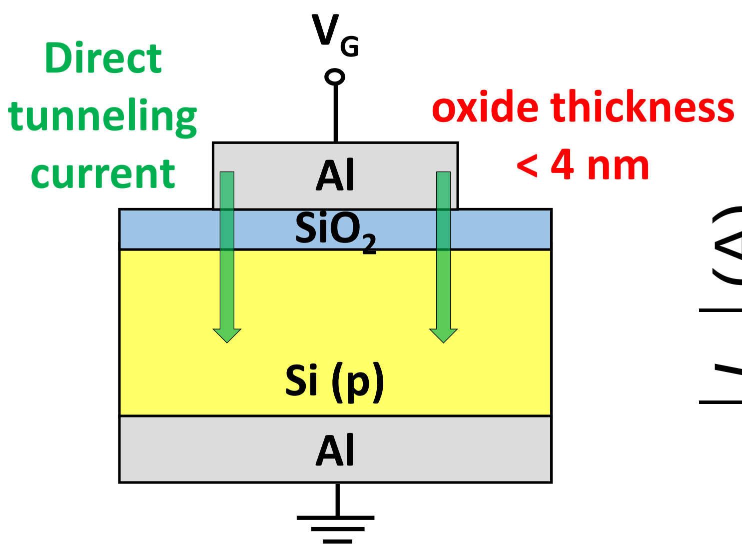
MOS capacitor

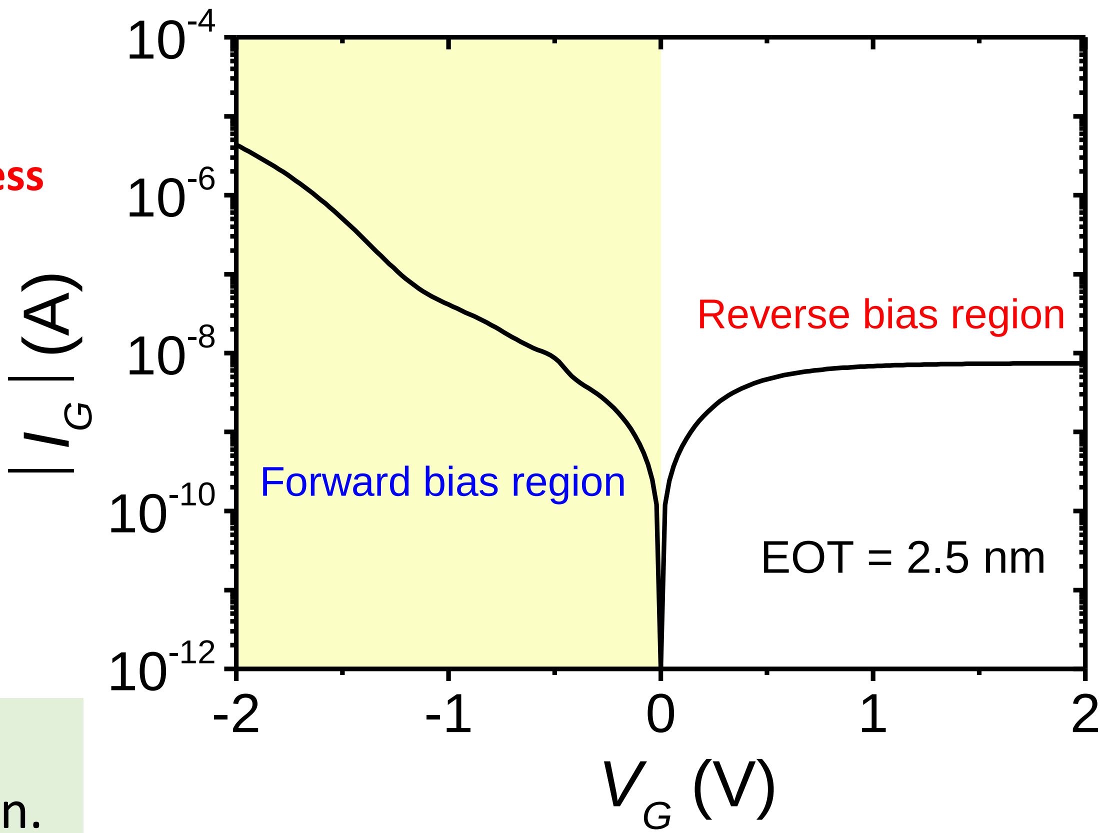


What is MIS TD?

***Metal-insulator-semiconductor tunnel diode (MIS TD)**

MIS tunnel diode (TD)



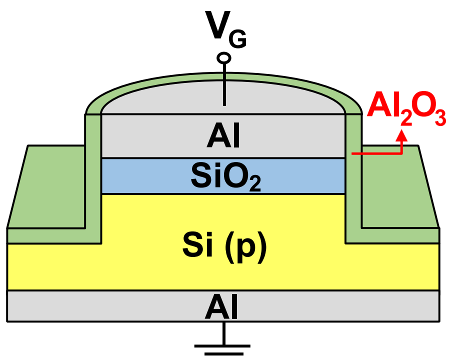


- Diode-like I–V curve.
- $V_G < 0$: forward bias region.
- $V_G > 0$: reverse bias region.

Transient Current in MIS TDs

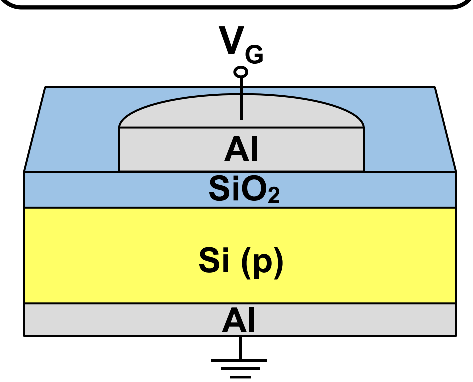
Trench structure MIS (Trench MIS)

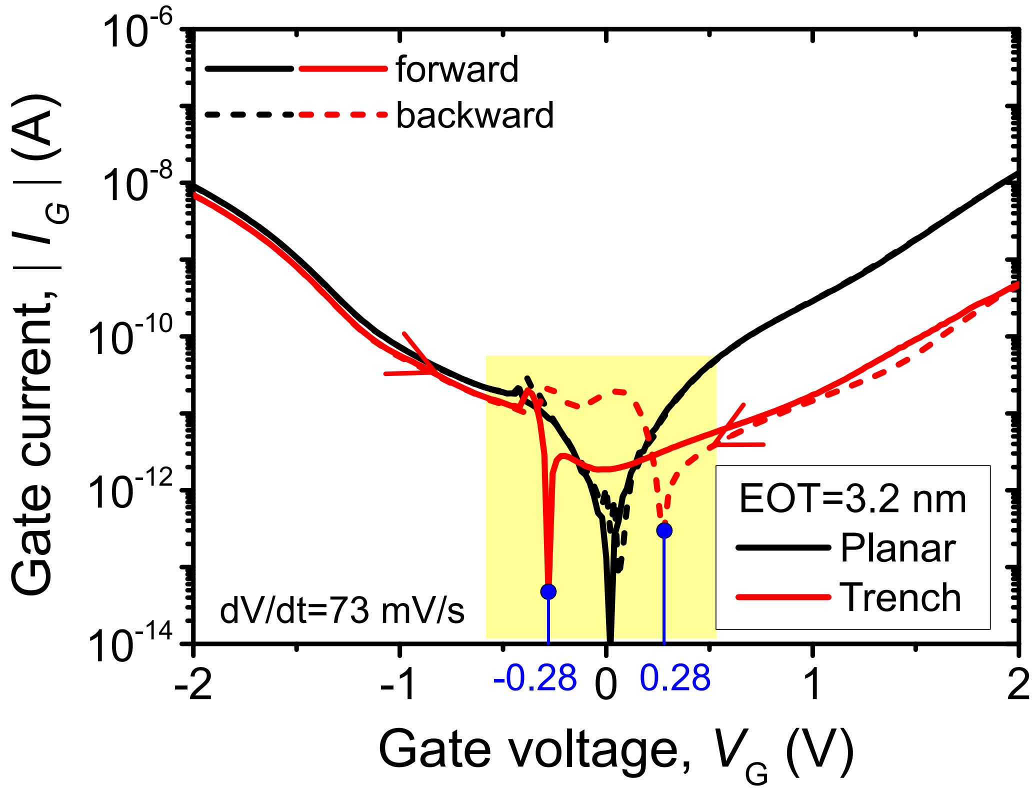
New special structure



Planar structure MIS (Planar MIS)

Normal structure

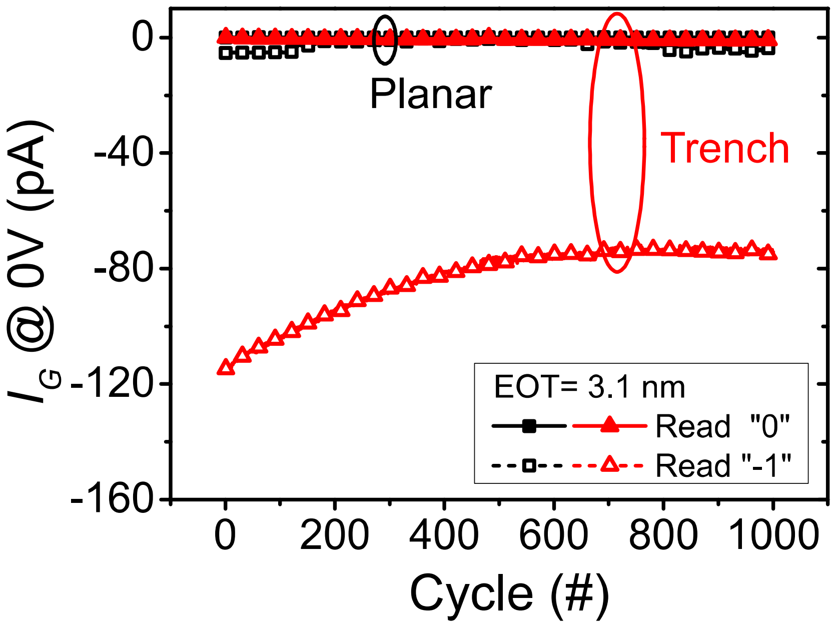


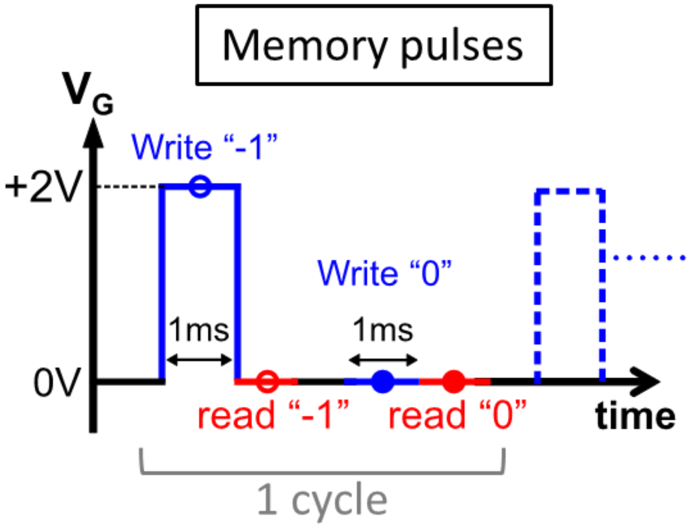


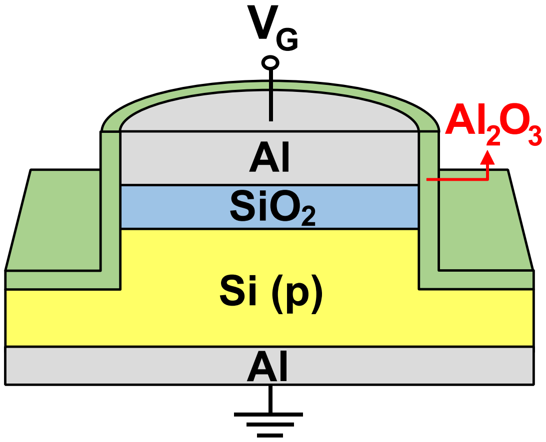
- Trench MIS TDs
  - *I-V* more obvious **hysteresis**.
  - **Stronger transient current**.

Transient Current in MIS TDs (cont.)

Endurance Property





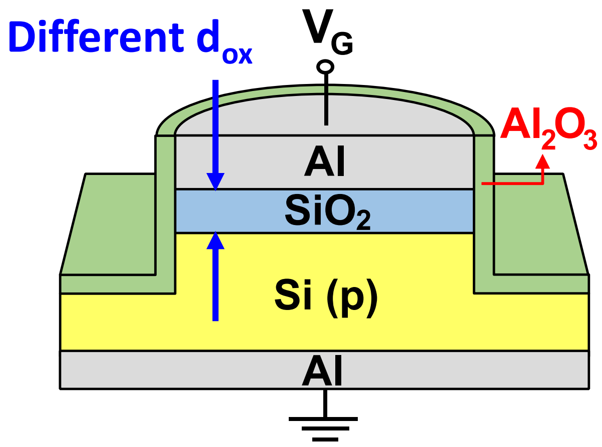


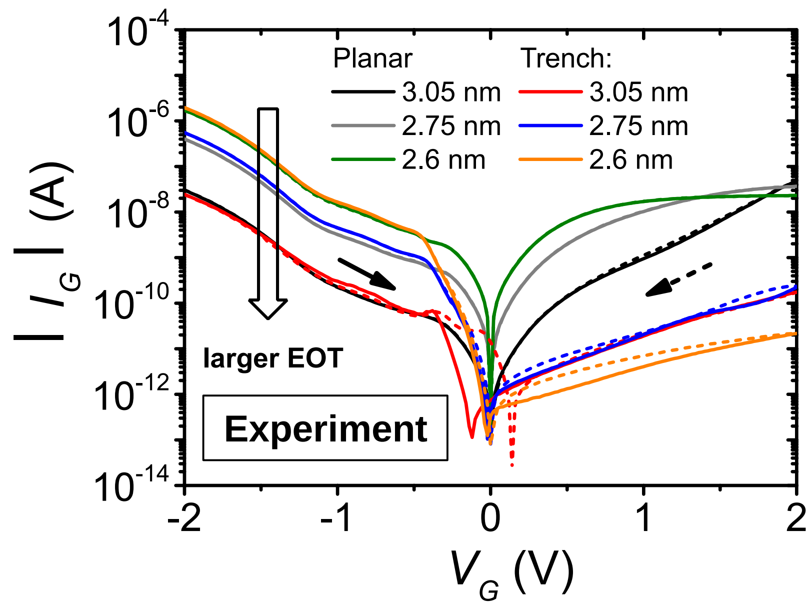
- **Transient current** behavior
  - ➢ Store **two memory states.**
- **Trench MIS TDs:**
  - ➢ potential for **memory devices.**

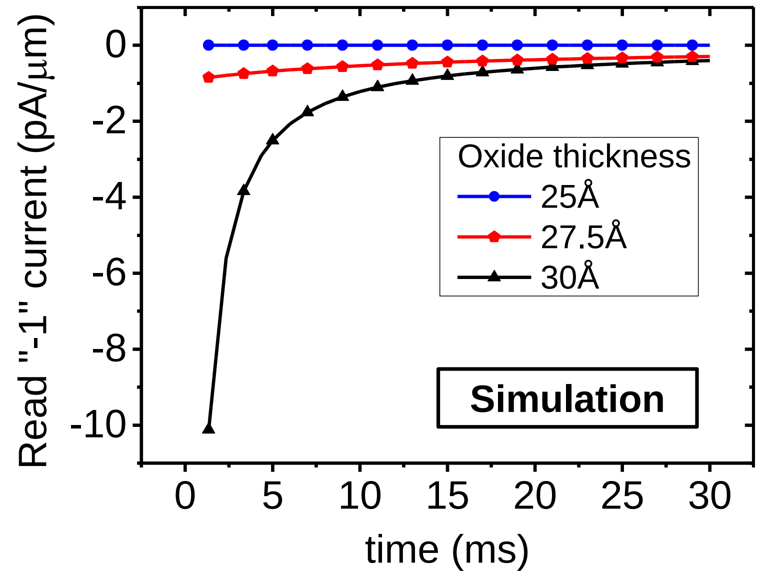
J. -Y. Lin and J. -G. Hwu, *IEEE Transactions on Electron Devices* **68**, 4189-4194 (2021)

In This Work…

Trench structure MIS
(Trench MIS)







Investigate the dependency of

- **transient current**.
- on the **tunneling oxide thickness (d_{ox})**

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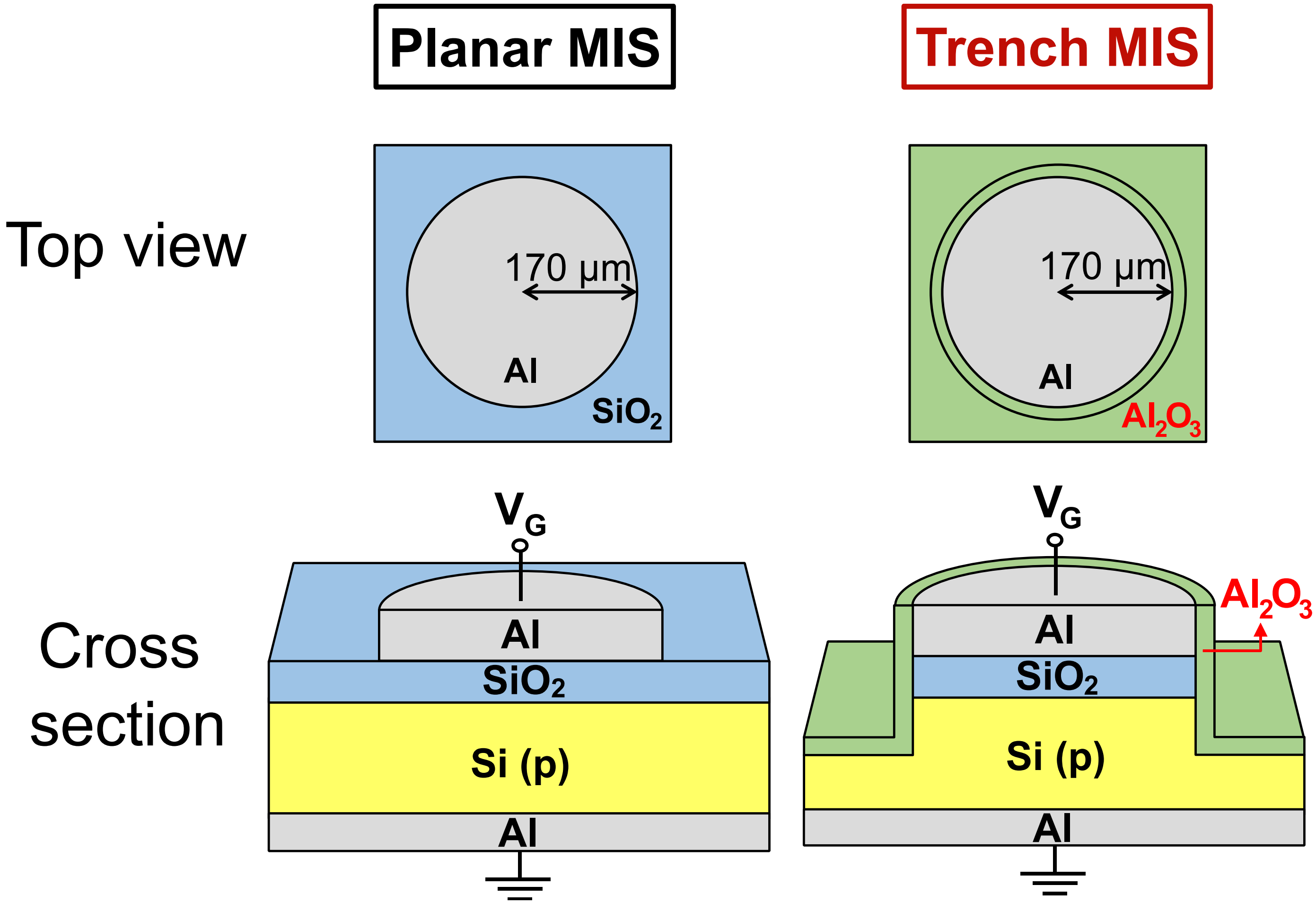
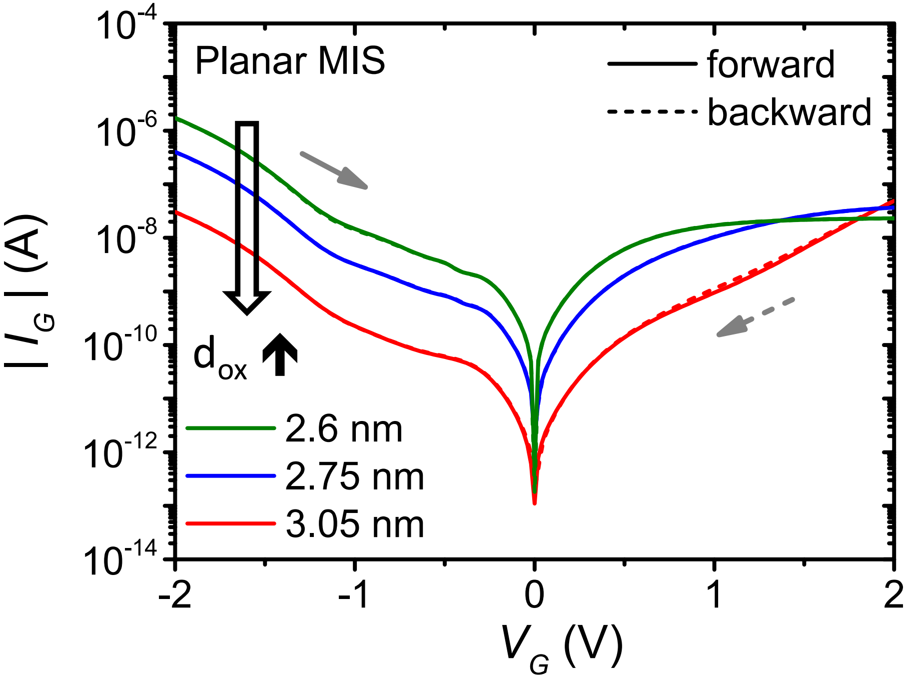
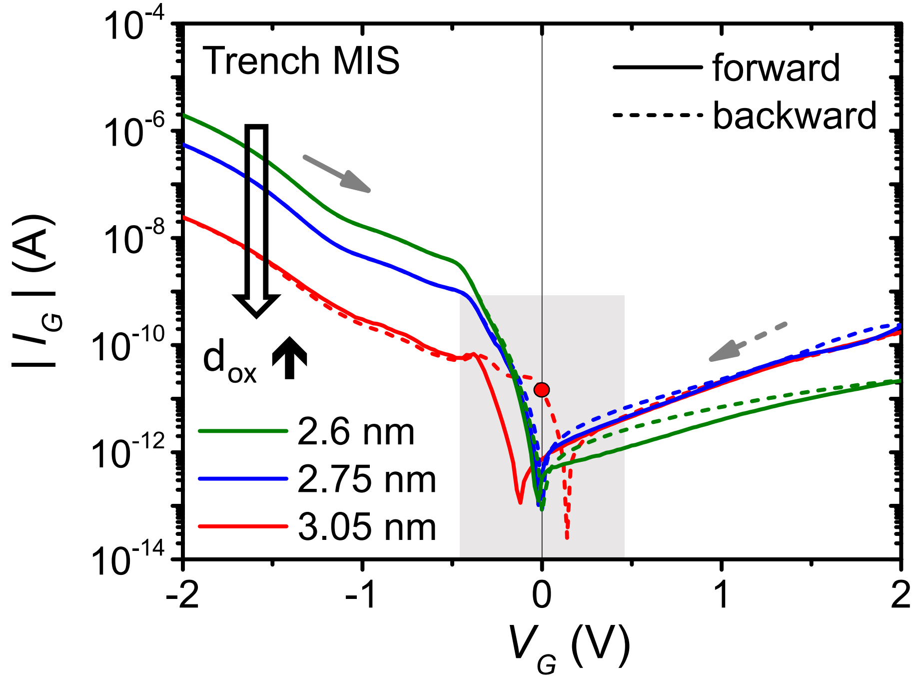
Device Structure

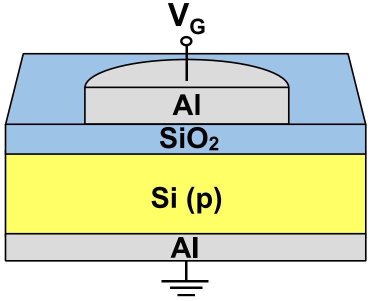


*Detailed fabrication process can be found in
IEEE Transactions on Electron Devices **68**, 4189-4194 (2021)

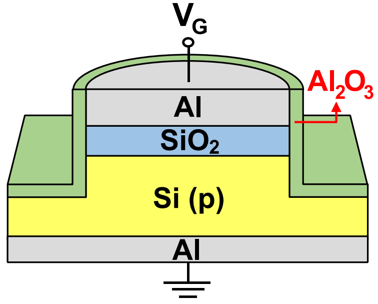
I-V Curves with Different d_{ox}



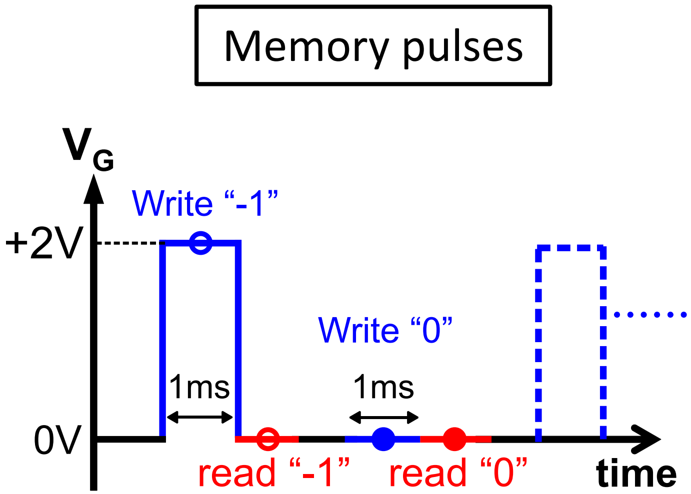


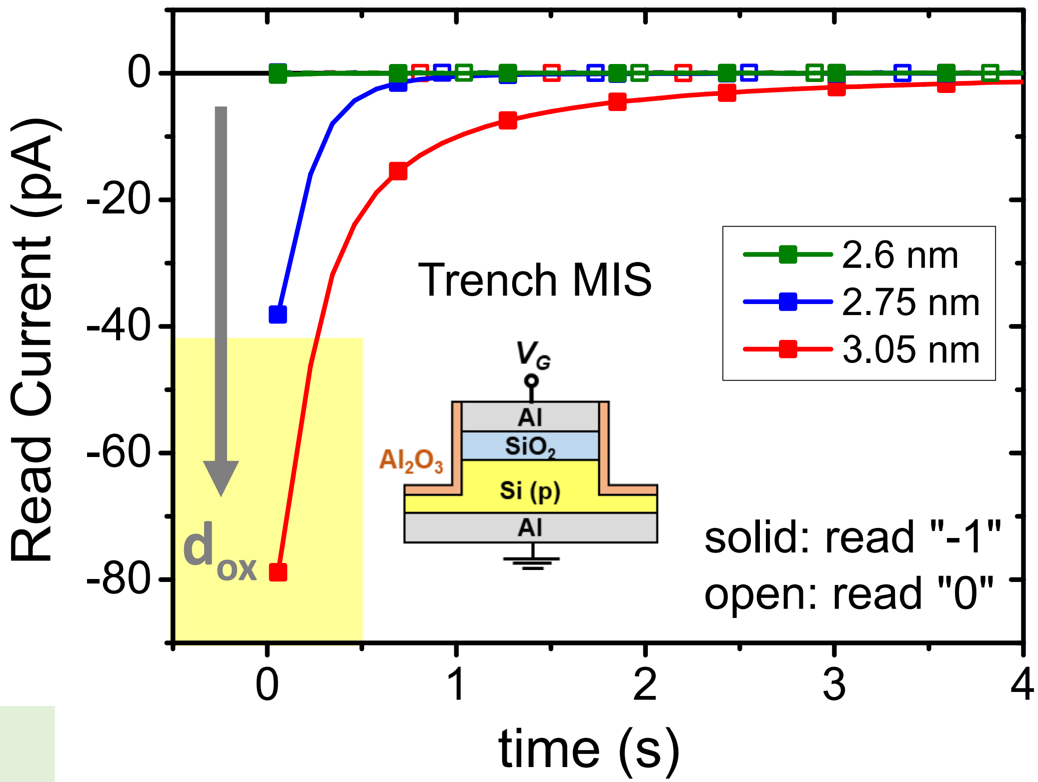


- For **Trench MIS,** when **d_{ox}** ↑
  - more apparent hysteresis.
  - **stronger transient current.**



Memory Retention Measurement



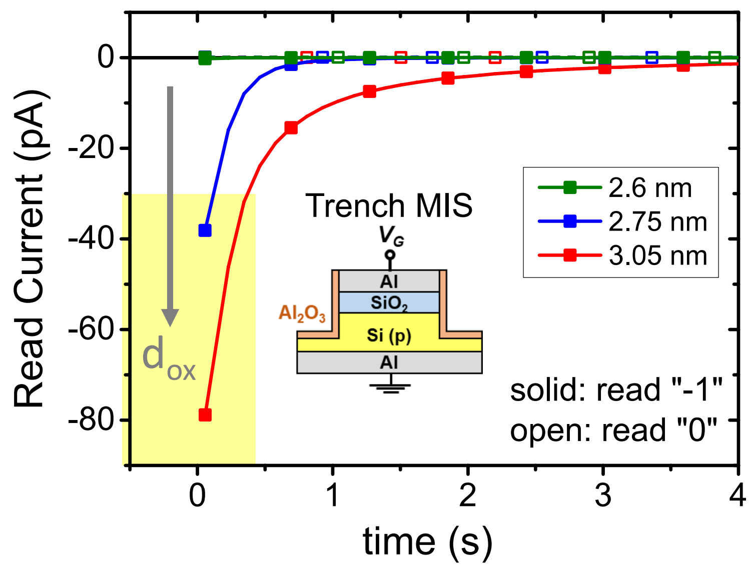


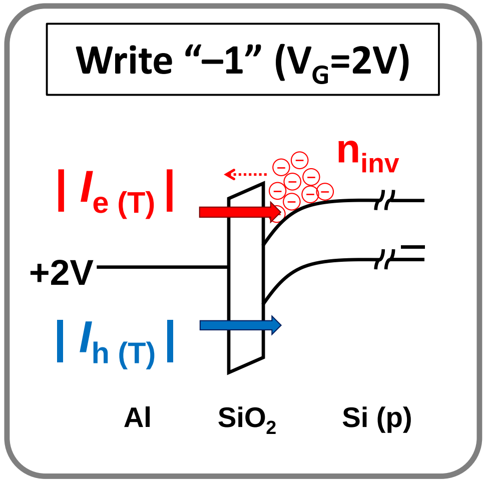
- Solid: read "-1".
- For **Trench MIS,** when **d_{ox}** ↑
  - **Stronger transient current** (i.e. **|read "-1" current|** ↑).

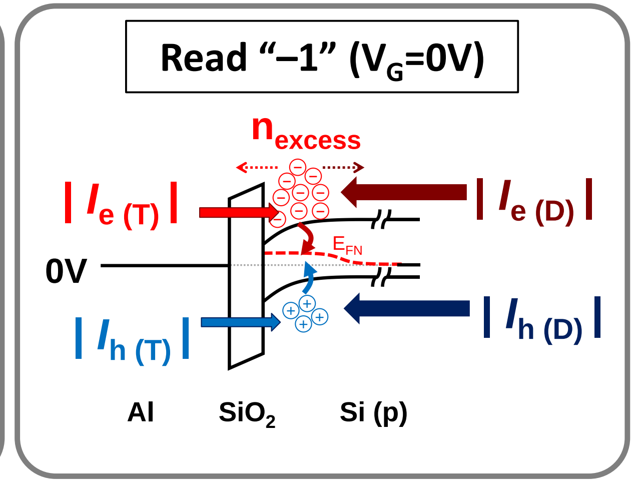
Where does "transient current" come from?

The Origin of Read "-1" Transient Current

*solid arrows: current flow







*n_{inv} : inversion carriers

*n_{excess} : excess electrons

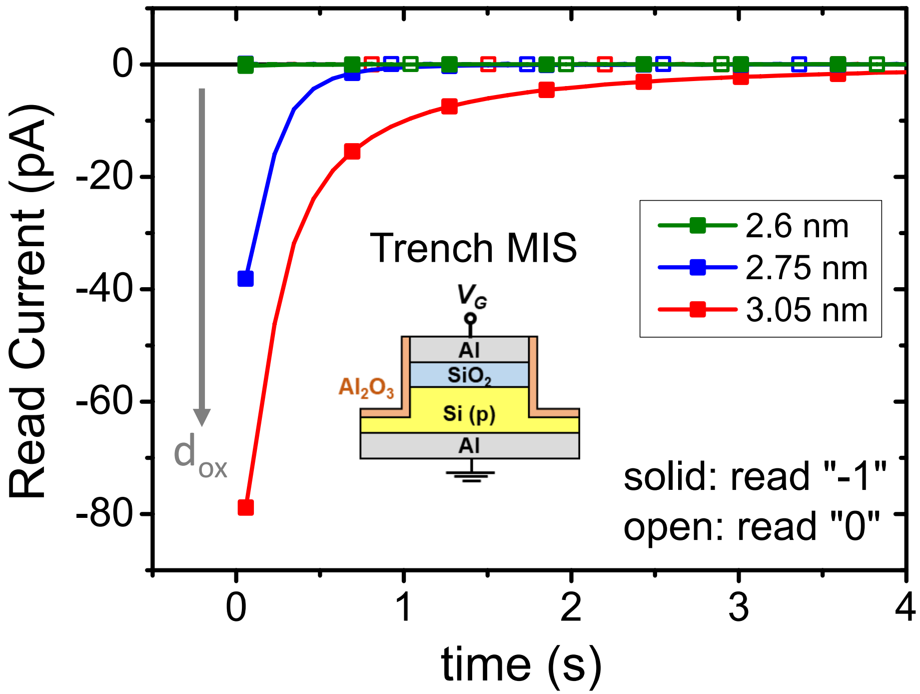
*$n_{excess} \approx n_{inv}$ (@V_G = +2V) – n_{inv} (@V_G = 0V)

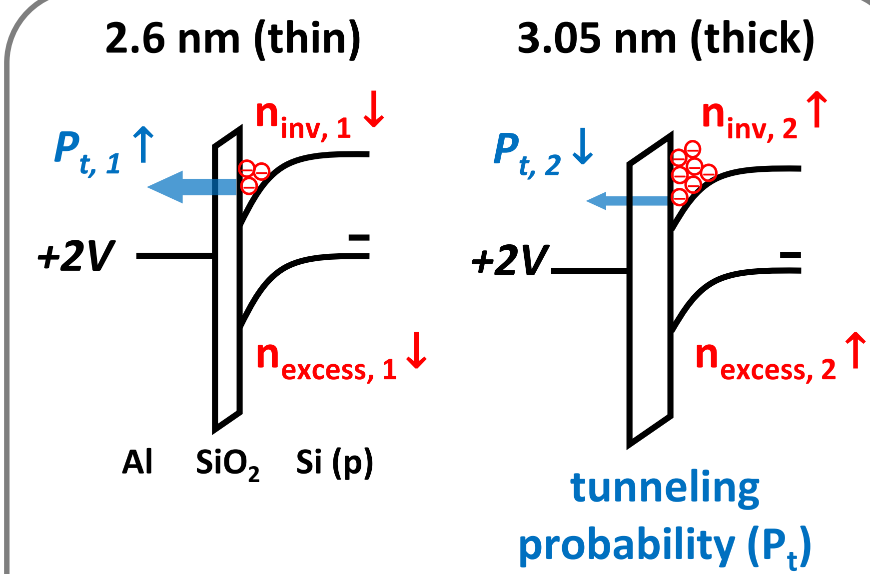
$$I_{read\,\text{“}-1\text{”}} = (|I_{e\,(T)}| + |I_{h\,(T)}|) - (|I_{e\,(D)}| + |I_{h\,(D)}|)$$

$\Rightarrow$ $|$ read "-1" current $| \propto n_{excess} \propto n_{inv}$ (@V_G=2V)

d_{ox} and Transient Current

| read "-1" current | ∝ n_{excess} ∝ n_{inv} (@V_G=2V)





$P_{t,1} > P_{t,2}$

$n_{inv,1} < n_{inv,2}$

$n_{excess,1} < n_{excess,2}$

| read "-1" $|_1$ < | read "-1" $|_2$

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Silvaco TCAD Simulation Setting

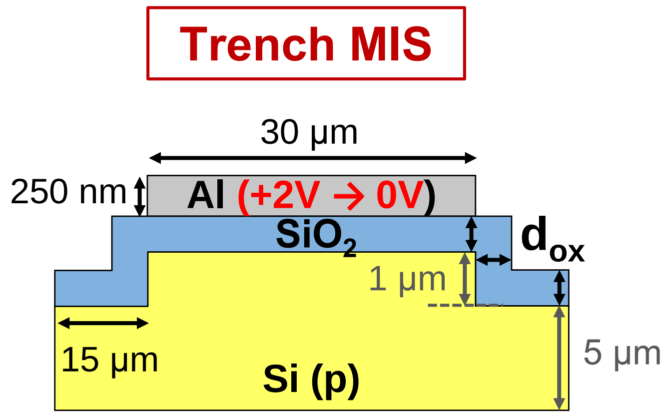
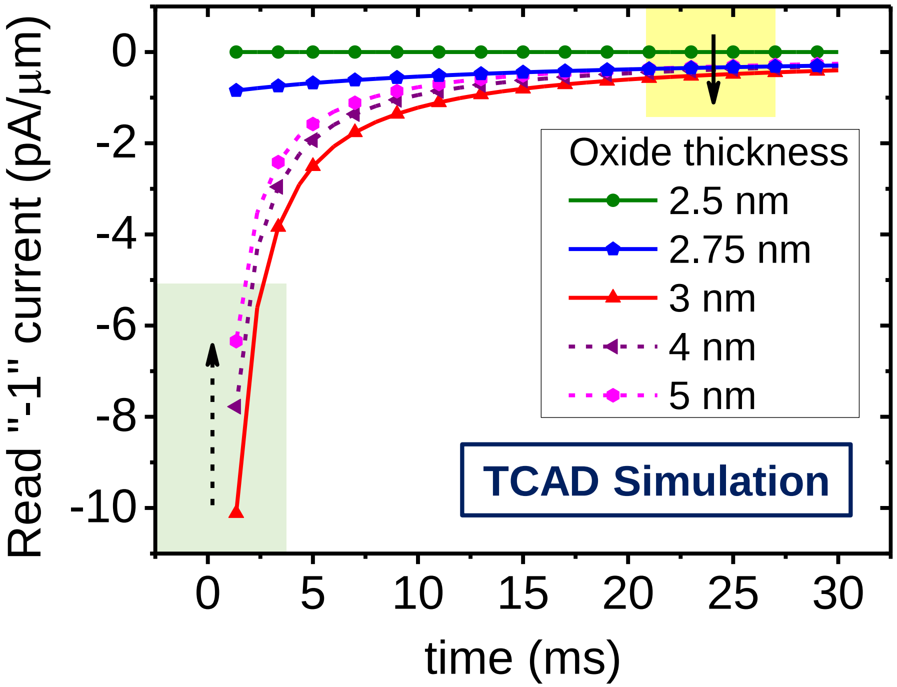


Fig. Simulated structure of Trench MIS.



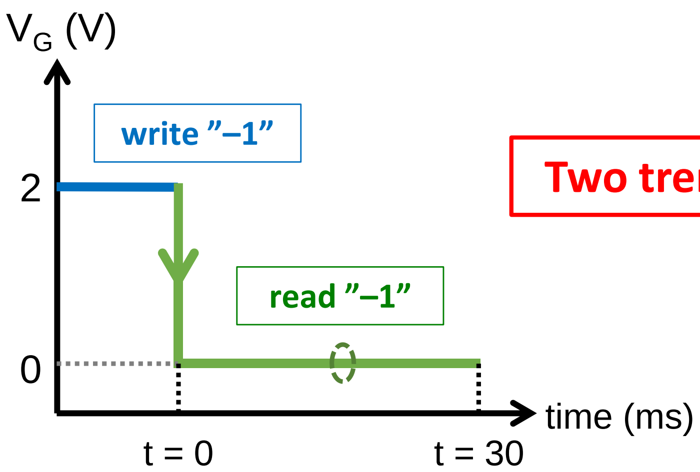


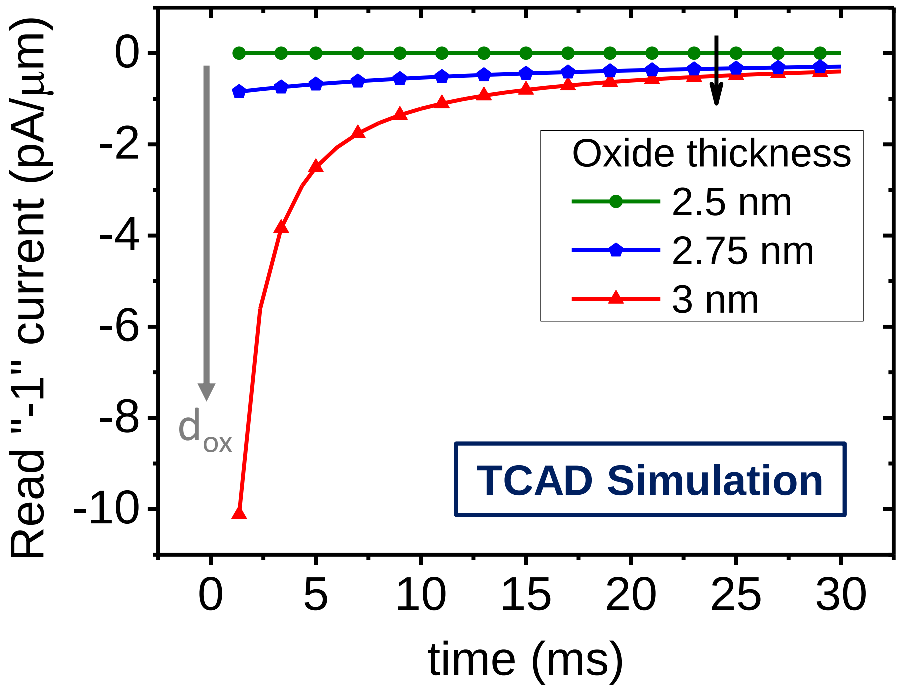
Fig. Silvaco TCAD simulation process.

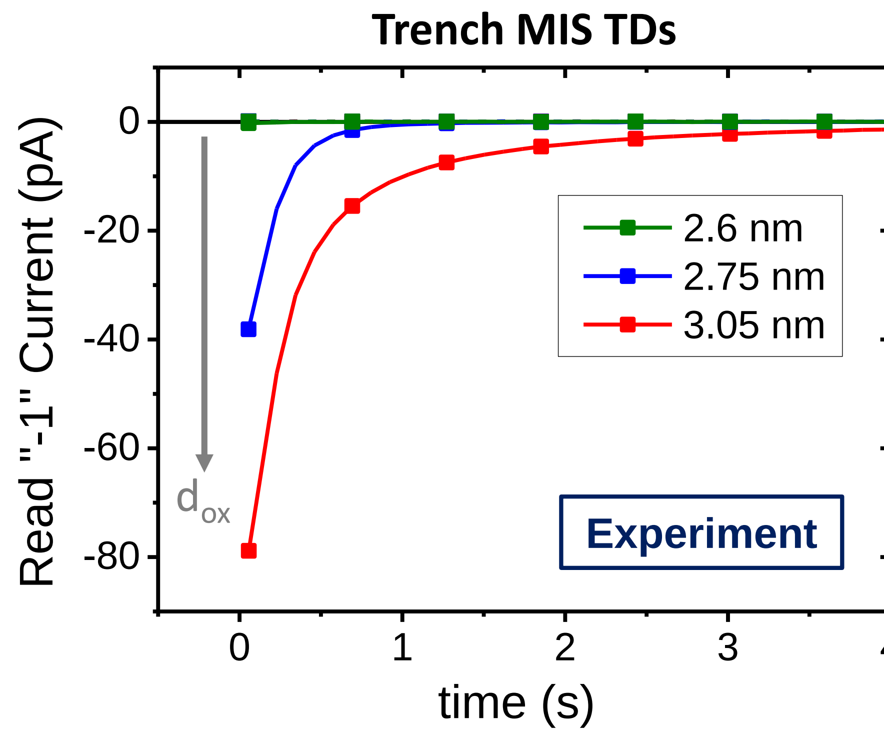
Two trends of d_{ox} — transient current

1) d_{ox} = 2.5 ~ 3 nm
   - ➢ **d_{ox} ↑, |read "-1" current| ↑.**

2) d_{ox} > 3 nm (simulation)
   - ➢ **d_{ox} ↑, |read "-1" current| ↓.**

Simulated Retention: Part 1



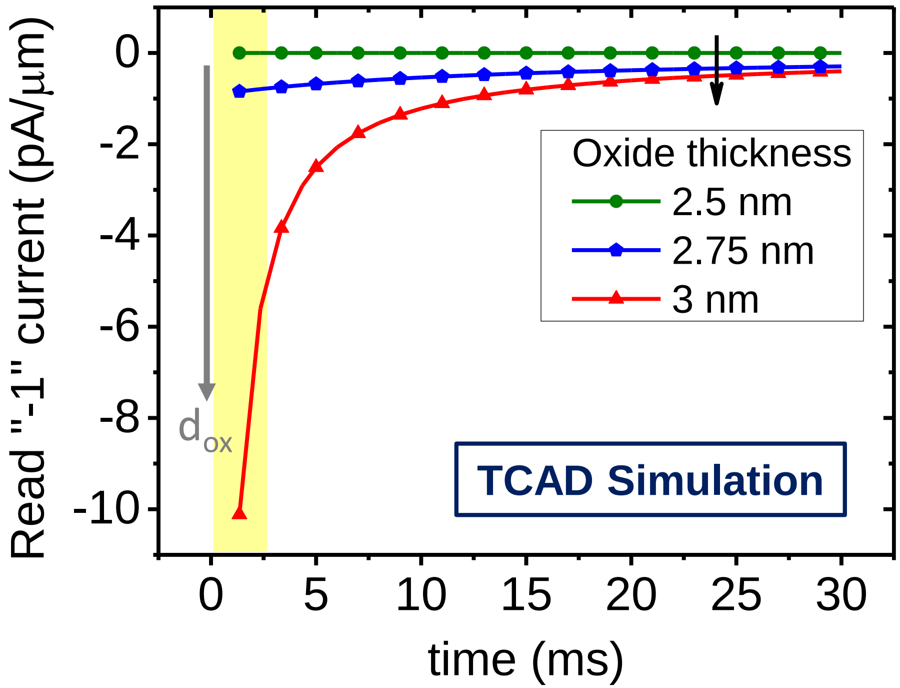


1) d_{ox} = 2.5 ~ 3 nm

➢ **d_{ox} ↑, |read "-1" current| ↑.**

d_{ox} ↑ » n_{excess} ↑
» |read "-1" current| ↑

Simulated Retention: Part 1

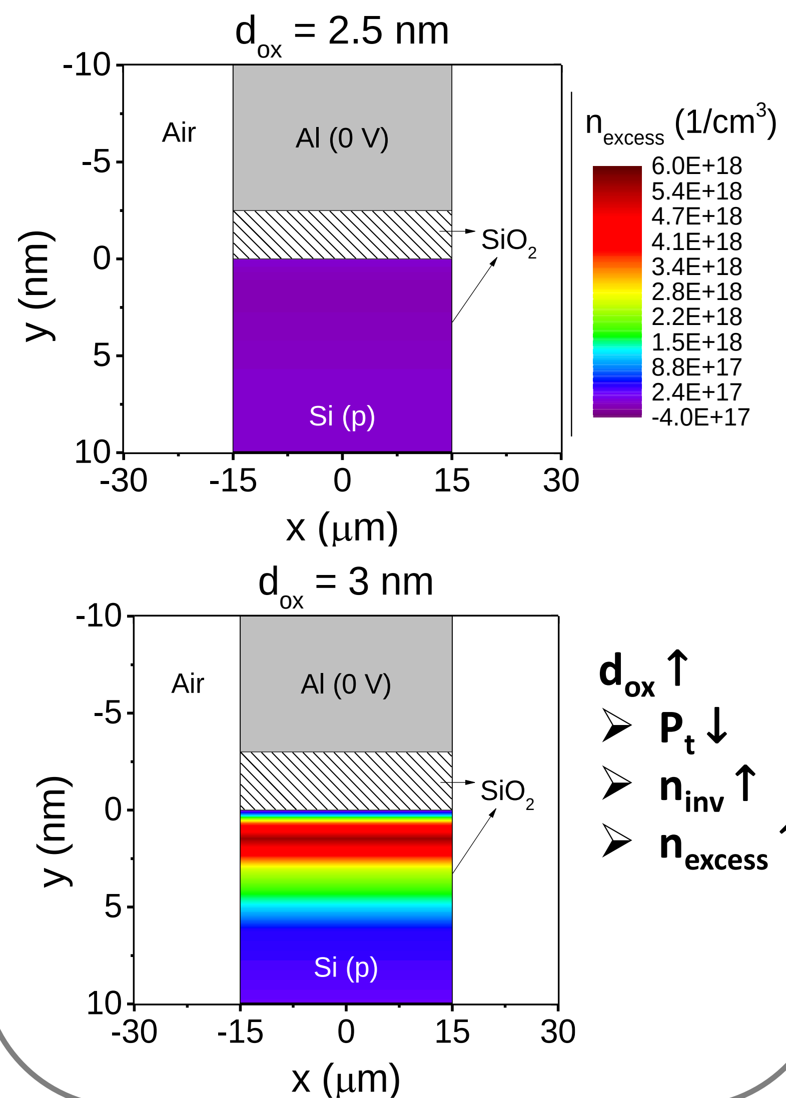


1) d_{ox} = 2.5 ~ 3 nm

- **d_{ox} ↑, |read "-1" current| ↑.**

***d_{ox} ↑ » n_{excess} ↑ » |read "-1" current| ↑**

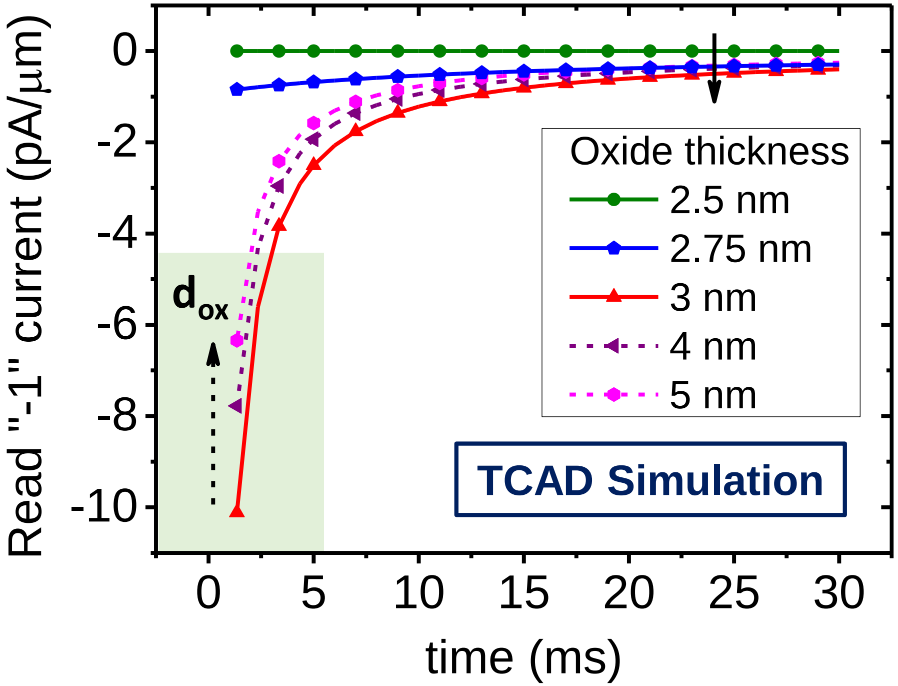
n_{excess} at t= 1.35 ms (simulation)



d_{ox} ↑

- **P_t ↓**
- **n_{inv} ↑**
- **n_{excess} ↑**

Simulated Retention: Part 2



1) d_{ox} = 2.5 ~ 3 nm

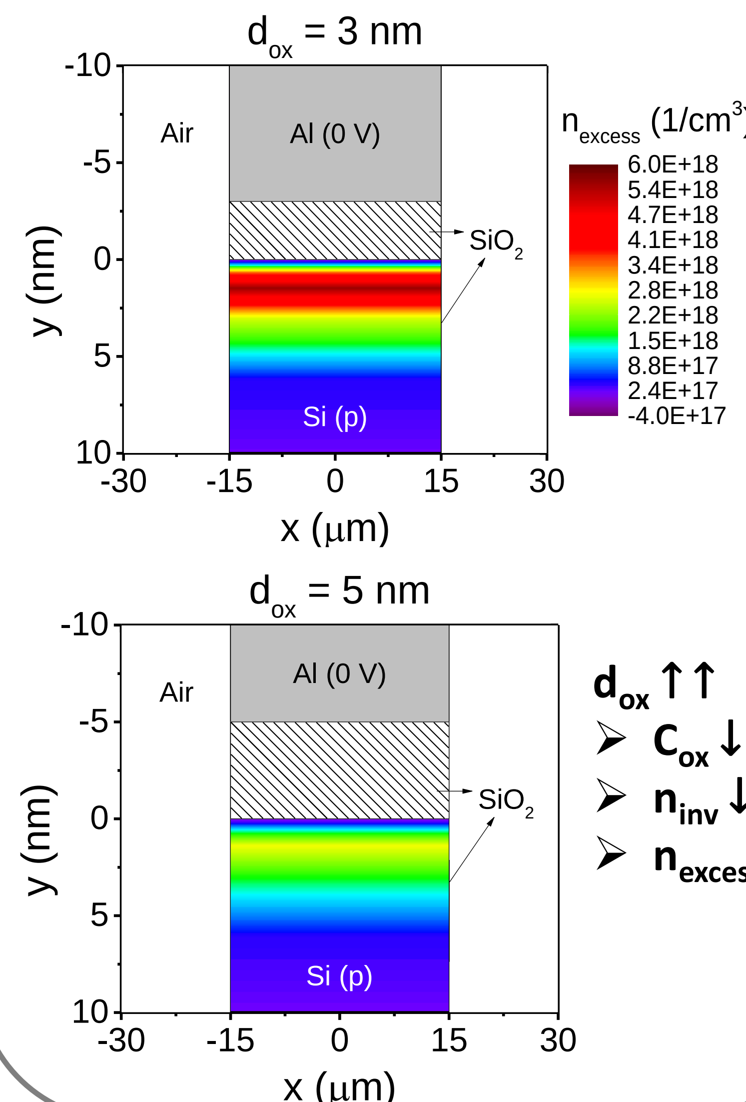
➢ **d_{ox} ↑, |read "-1" current| ↑.**

2) d_{ox} > 3 nm (simulation)

➢ **d_{ox} ↑, |read "-1" current| ↓.**

|read "-1" current| ∝ n_{excess}

n_{excess} at t= 1.35 ms (simulation)



d_{ox} ↑↑

➢ **C_{ox} ↓**

➢ **n_{inv} ↓**

➢ **n_{excess} ↓**

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Conclusion

- Investigated "transient current – d_{ox}" relation of Trench MIS TDs by (1) experiments and (2) TCAD simulation.

- d_{ox} = 2.5 ~ 3 nm: $d_{ox}\uparrow$, $P_t\downarrow$, $n_{excess}\uparrow$, |Transient current| $\uparrow$.
- d_{ox} = 3 ~ 5 nm: $d_{ox}\uparrow$, $C_{ox}\downarrow$, $n_{excess}\downarrow$, |Transient current| $\downarrow$.

- |Transient current| $\propto$ excess electrons (n_{excess}).

Thank you for listening!

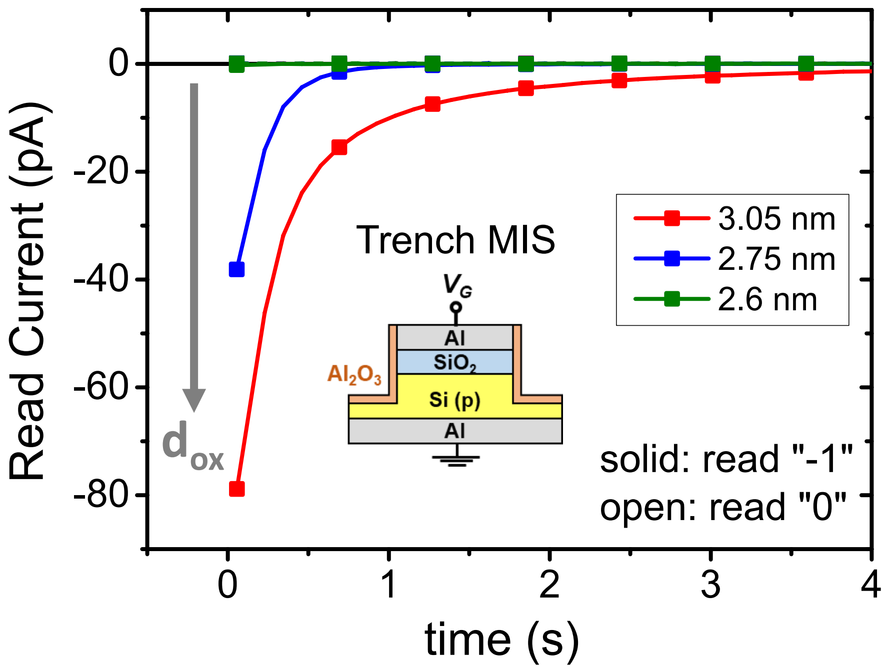
Presenter: Jian-Yu Lin

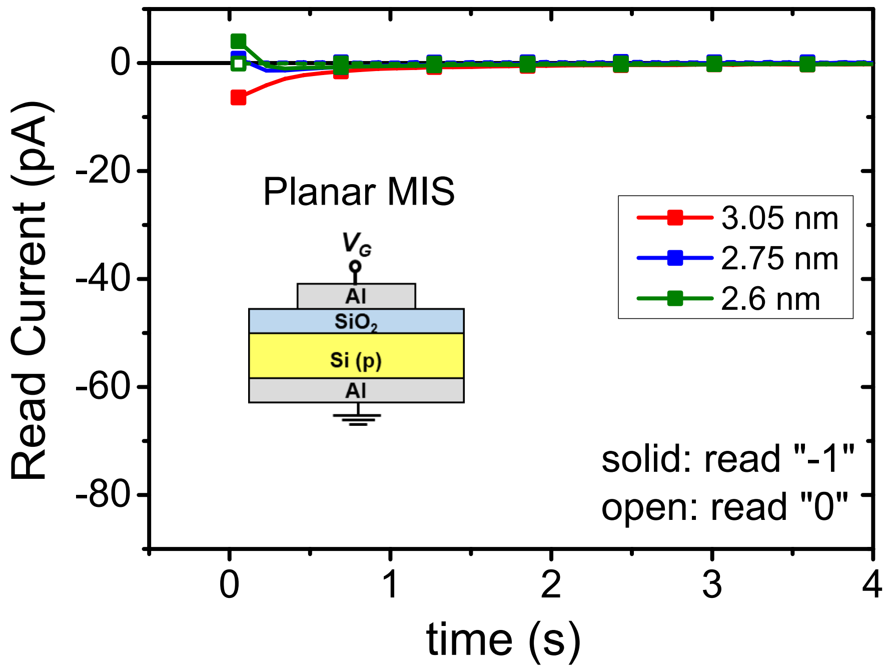
Acknowledgement

- This work was supported by the Ministry of Science and Technology of Taiwan under Contracts MOST 110-2221-E-002-140 and 110-2622-8-002-014.

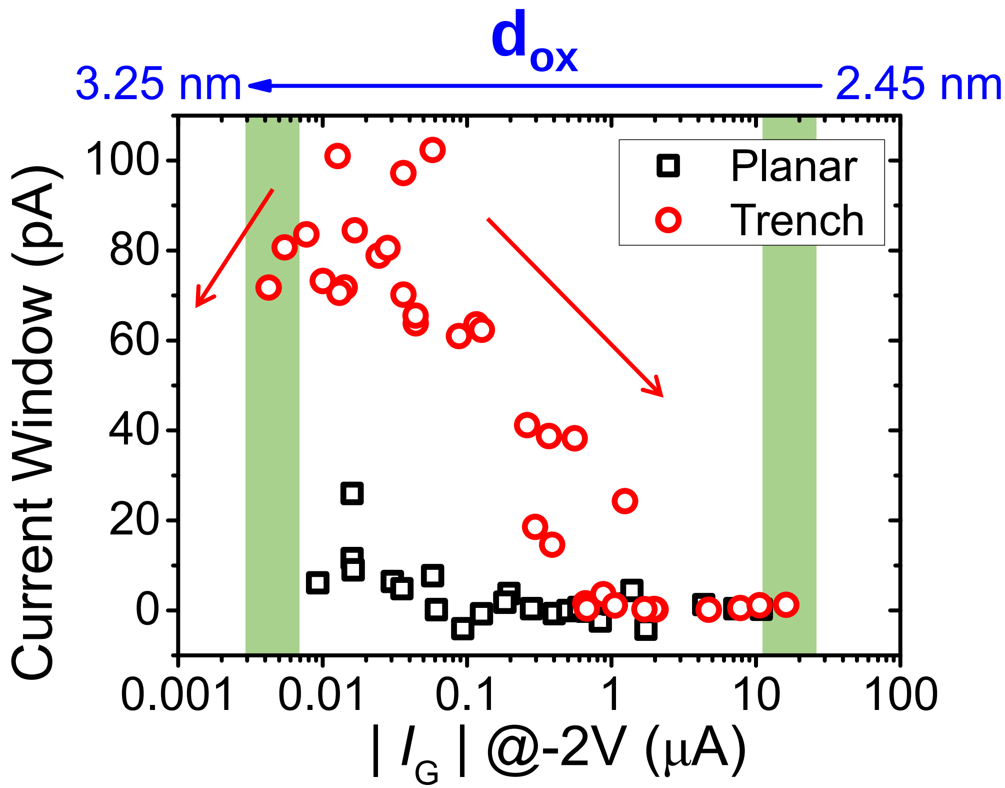
Q&A

Memory Retention





Turn Around in Experiment

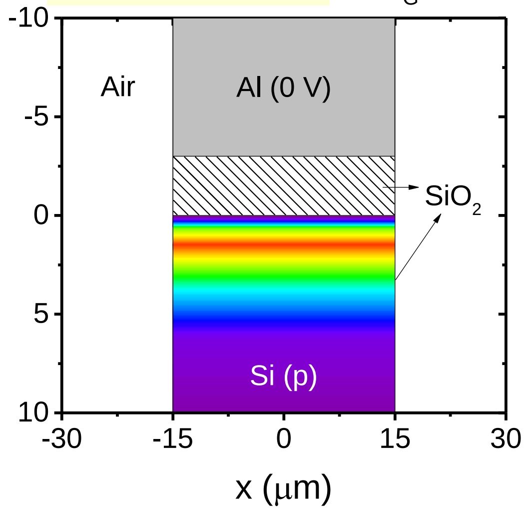


- **Y-axis:** Current Window ≈ |read "-1" current|.
- **X-axis:** d_{ox} from 3.25 ~ 2.45 nm.

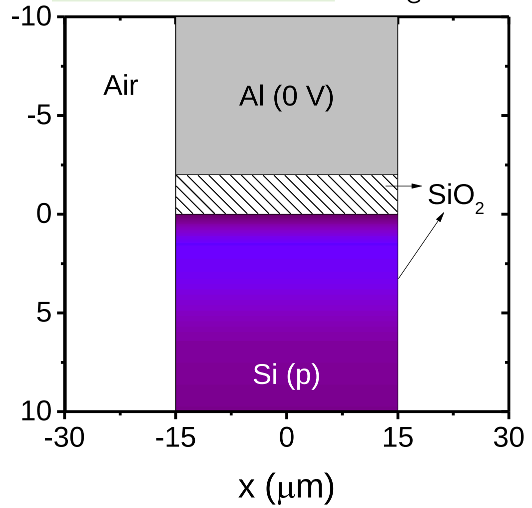
Transient TCAD with Different EOTs

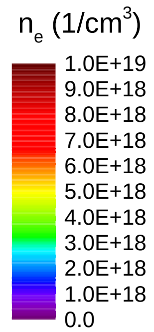
- **<u>Electron concentration under linear scale (different d_{ox})</u>**

3 nm, t = 1.35 ms @ V_G = 0 V

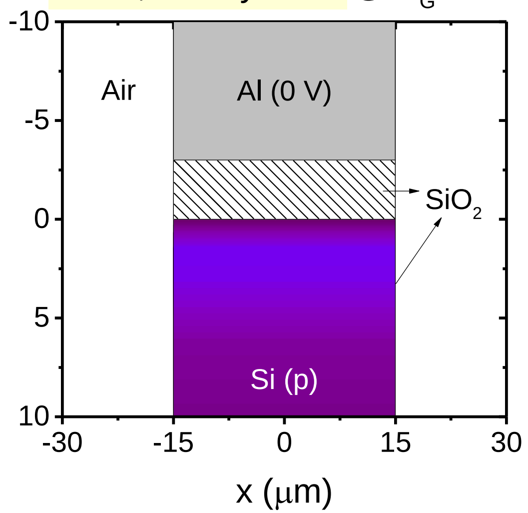


2 nm, t = 1.35 ms @ V_G = 0 V

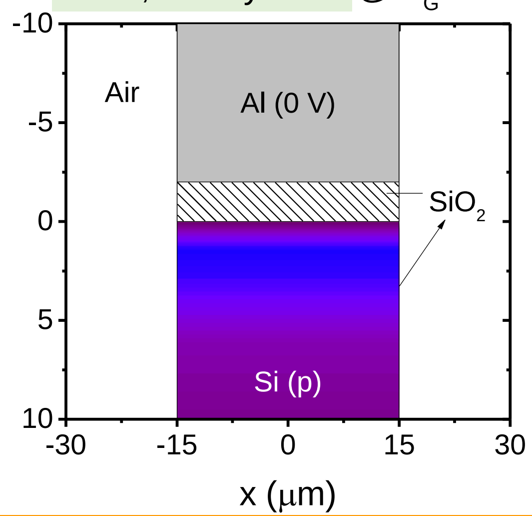


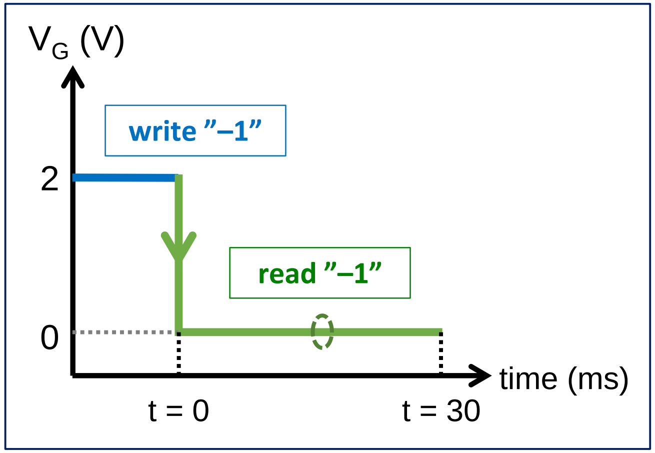


3 nm, steady-state @ V_G = 0 V



2 nm, steady-state @ V_G = 0 V





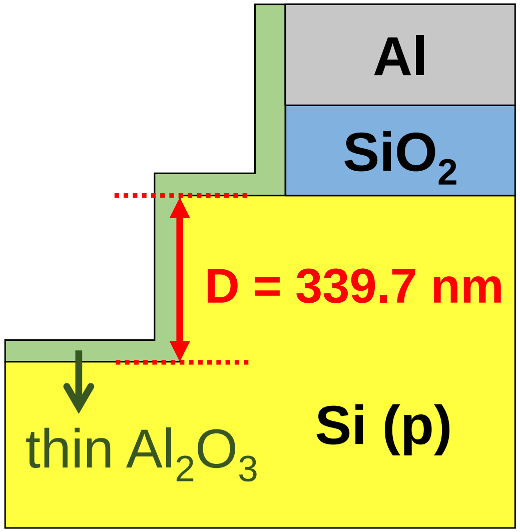
$$n_{excess} = n_e(@\,t = 1.35\ ms) - n_e(@\,t = \infty)$$

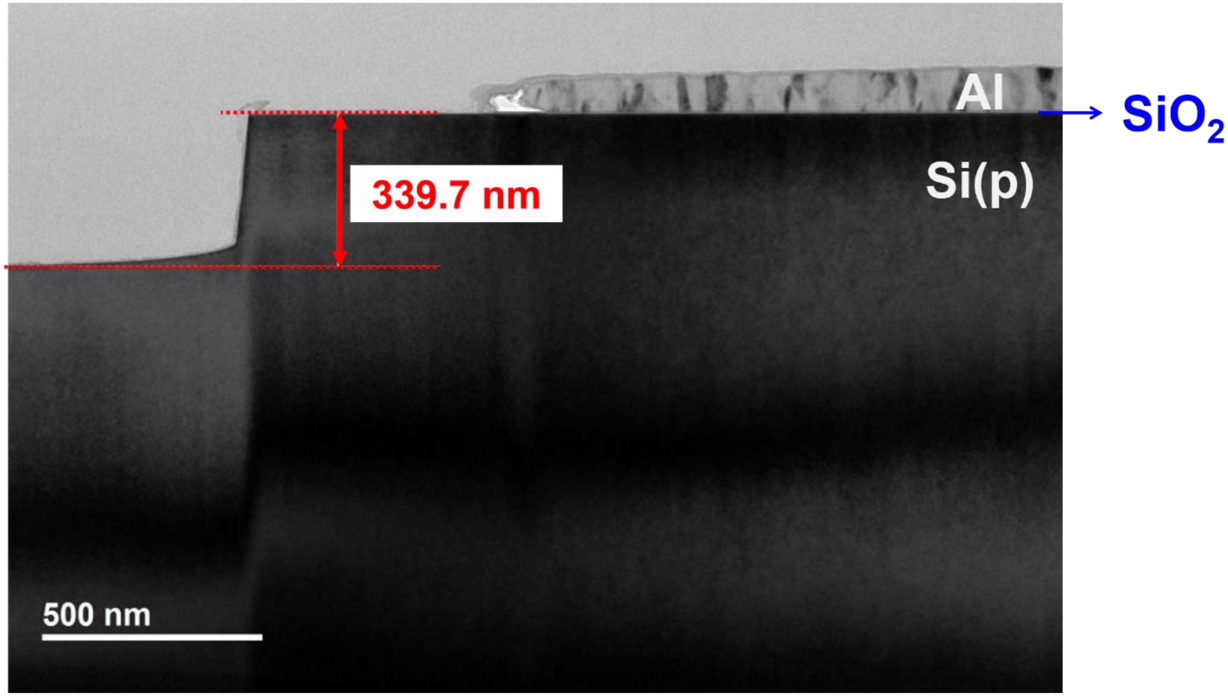
TCAD Simulation: Models

Physical Models
1. Concentration-dependent mobility (conmob)
2. SRH (srh)
3. Auger (auger)
4. Band gap narrowing (bgn)
5. Field-dependent mobility (fldmob)
6. Quantum/direct tunneling (qtunnsc)
7. Bohm quantum potential (bqp) models

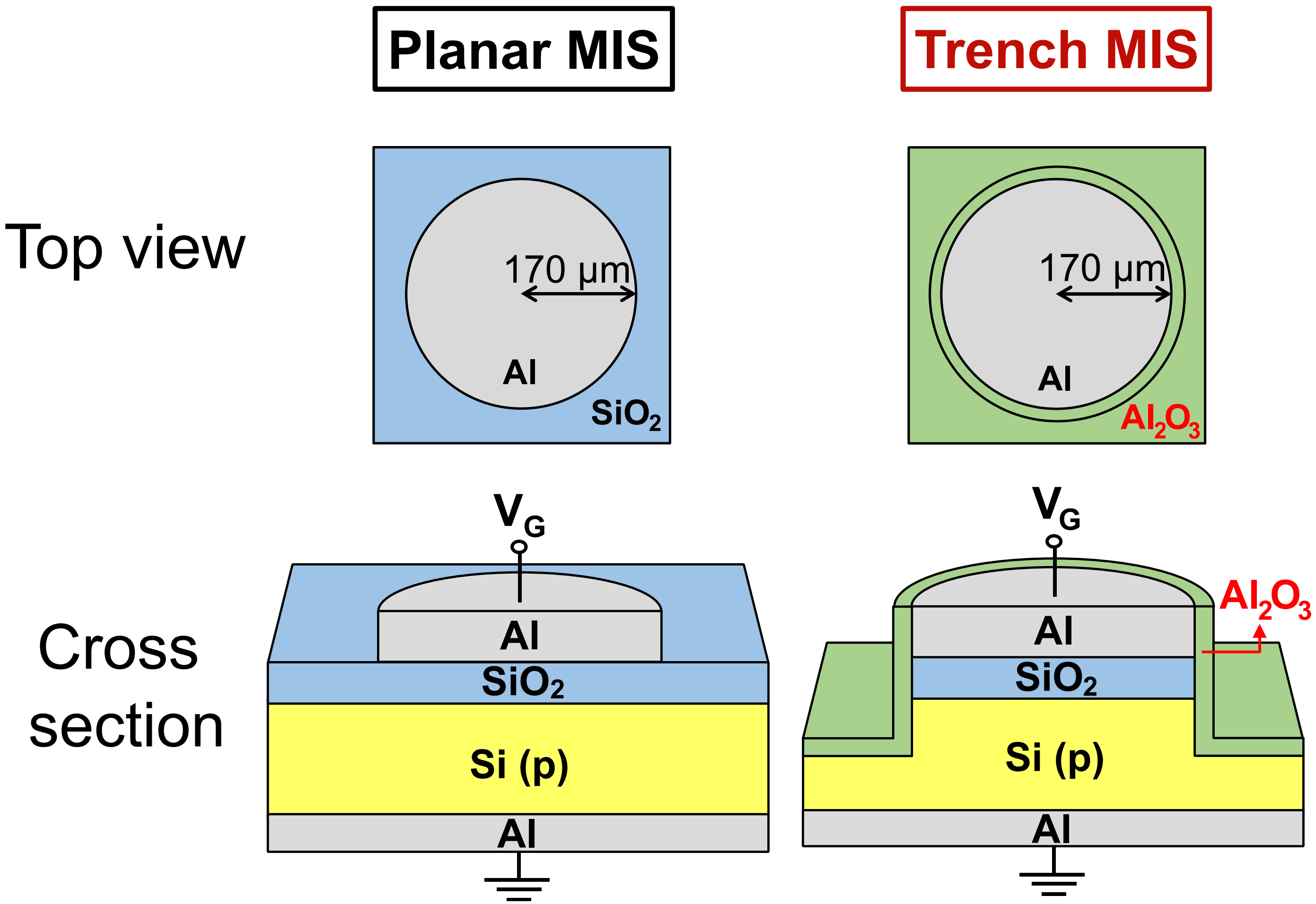
consider distribution of electrons in the inversion layer (quantum confinement)

Trench Structure

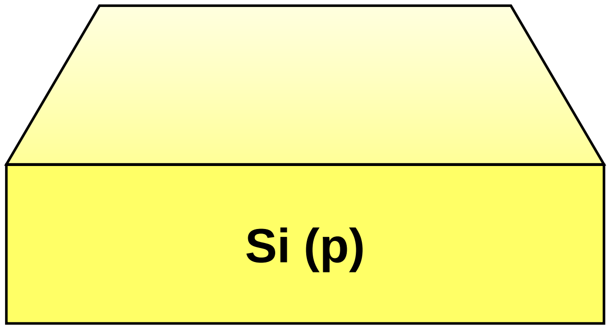




Device Structure

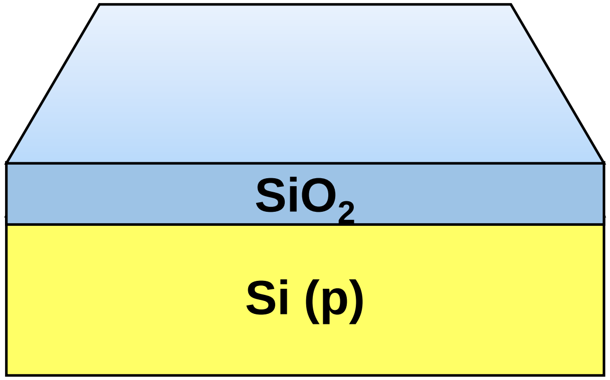


Device Fabrication (1/2)



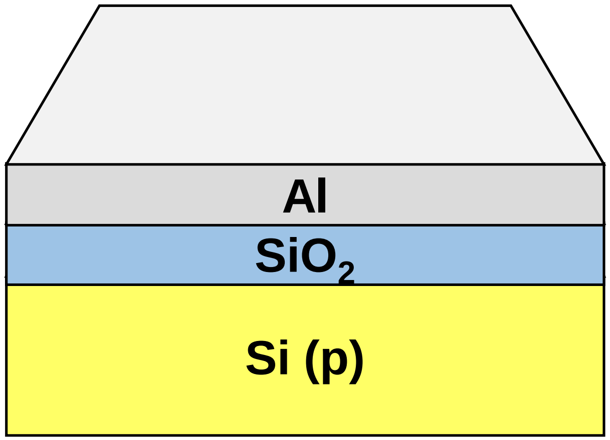
- Radio Corporation of America (RCA) clean
- Ultra-thin oxide grown by anodic oxidation
- RTA in N_2 at 950 ^{0}C for 15 s
- Thermal evaporate 250nm Al as top electrode
- Photolithography
- Al wet etching
- ✵ Si substrate etching by RIE

Device Fabrication (1/2)



- Radio Corporation of America (RCA) clean
- Ultra-thin oxide grown by anodic oxidation
- Rapid thermal annealing (RTA) in N_2 at 950 ^oC for 15 s
- Thermal evaporate 250nm Al as top electrode
- Photolithography
- Al wet etching
- ✵ Si substrate etching by RIE

Device Fabrication (1/2)



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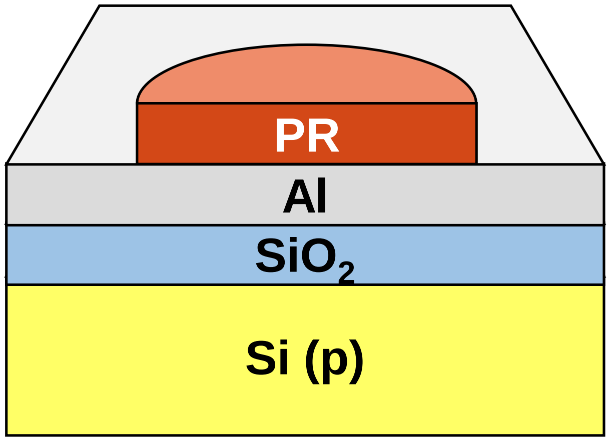

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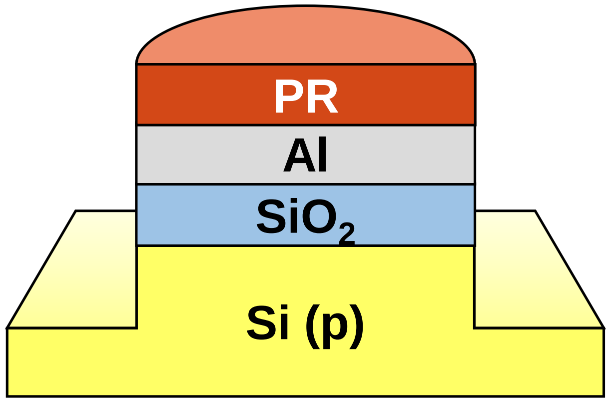
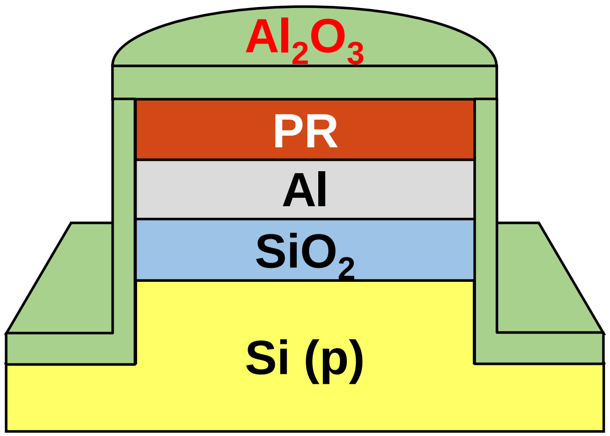


✵ Trench MIS only process

- Radio Corporation of America (RCA) clean
- Ultra-thin oxide grown by anodic oxidation
- RTA in N_2 at 950 ^{0}C for 15 s
- Thermal evaporate 250nm Al as top electrode
- Photolithography
- Al wet etching
- ✵ Si substrate etching by RIE

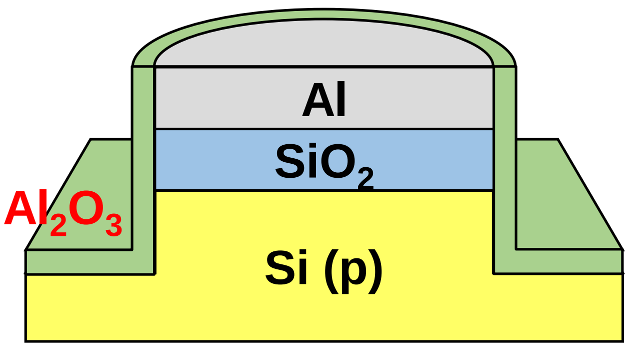
Device Fabrication (2/2)



Al_2O_3 layer (passivation layer):
protect Si substrate from being exposed to air.

- ✵ Remove native oxide by BOE
- ✵ Deposit Al_2O_3 by *in-situ* oxidation of dc sputtering Al target in Ar/O_2 ambient
- Lift-off photoresist (PR)
- ✵ Furnace annealing in N_2 at 200 ^oC for 10 minutes
- Backside native oxide removal
- 200 nm Al back electrode deposition

Device Fabrication (2/2)



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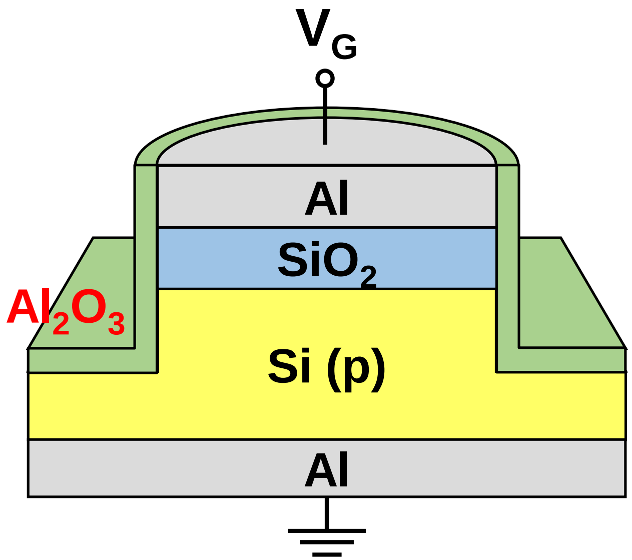

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