I aspire to pursue a PhD in Electrical Engineering and Computer Sciences at Massachusetts Institute of Technology. I would like to conduct research in Nanoscale Materials, Devices, and Systems since I am interested in semiconductor devices and have four years of relevant research experience (two years in university and two years as a master's student). I was inspired to pursue this topic in an undergraduate course, Electronics (I), where I enjoyed learning about the mechanisms behind semiconductor devices such as MOSFETs and diodes. My research includes a study of band structure, an analysis of interface state density (D_{it}) of FinFETs, and research on volatile memory devices using metal-insulator-semiconductor tunnel diodes (MIS TDs). I presented my results at two conferences and authored a paper published in a peer-reviewed journal all as first author. In terms of my academic performance, I have a BS in Electrical Engineering with an overall GPA of 4.15/4.3 (ranking top 7%) and an MS in Electronics Engineering with a GPA of 4.3/4.3 (ranking top 1%) from National Taiwan University. My career goal is to become a researcher in the semiconductor industry. I believe I can reach my goal with solid training in your program.

My first research on band structure solidified my understanding of solid-state physics. I joined Prof. Jiun-Yun Li's lab in my junior year in university and worked on investigating spin-orbit coupling in GeSn via band structure calculations using the empirical pseudopotential method (EPM). I started with the classical Kronig-Penney Model in solid-state physics and acquired a basic understanding of band structure. I then did a literature review of EPM simulation and realized modified virtual crystal approximation had to be adopted to set various Sn to Ge ratios in band structure calculations. I was eventually able to produce preliminary results of the GeSn band structure by utilizing a program called *Sentaurus Band Structure*. With this research project, I won a TSMC-NTU Research Center Scholarship, which was given by Taiwan Semiconductor Manufacturer Company (TSMC) to students at my university based on their academic and research performance.

During my two-month summer internship in the 5 nm Node (N5) Device Department at TSMC, I continued to enhance my knowledge of semiconductor physics and acquired project management capability. At that time, the Department did not have a way to evaluate the energy distribution of D_{it} using TSMC's wafer acceptance test (WAT) computer programs which are used by engineers to carry out electrical measurements. I was motivated to extract the D_{it} energy profiles of FinFETs using the charge pumping (CP) method. Besides learning about the theory of CP, I wrote several WAT programs to adjust the different gate pulse conditions in CP experiments and evaluate D_{it}. To ensure the project could meet the two-month deadline, I set up a schedule and a weekly task list and adhered to it. Eventually, I delivered results within the timeframe and presented them in a weekly department meeting. I was selected to be a finalist in the R&D group of the 2019 TSMC Summer Internship Competition (top 15% among all R&D interns) based on my project and presentation skills.

During my master's study in Prof. Jenn-Gwo Hwu's group, I gained a strong background in MOS and memory devices and the ability to support my explanations with data. The lab aimed to utilize MIS TDs as volatile memory devices by using the different transient currents of MIS TDs to store memory data. Yet, one of the key problems was how to further enlarge the transient current to have better memory performance. To solve this problem, I proposed a new structure for MIS TDs, called trench structure MIS TDs (denoted as trench MIS TDs). For devices with thin oxide (≈ 2.5 nm), I found that trench MIS TDs showed a stronger transient current with a current window (CW, the read current difference between two different memory states, can be viewed as a metric for memory performance) that was 5 times larger than traditional planar structure MIS TDs (denoted as planar MIS TDs) in long write time (>10 s) memory endurance measurements. The stronger transient current was attributed to the extra traps located in the trench structure, which could be verified by endurance experiments with different write voltage conditions. I presented the above results at *International Electronic Devices and Materials Symposium (IEDMS) 2020*.

Nevertheless, as mentioned above, trench MIS TDs with thin oxide (2.5 nm) required a write time (>10 s) that was too long to be used in actual memory chips to set different memory states. Therefore, I switched to investigating MIS TDs with thicker oxide (≥2.8 nm) to address this long write time issue. In the subsequent endurance measurements, I discovered that within the thick oxide range, trench MIS TDs not only demonstrated a larger transient current with a CW that was 25 times larger compared to planar MIS TDs but also demanded a much shorter write time (1 ms). Substantiated by capacitance-voltage measurements and technology computer-aided design simulation, I proposed that the weaker oxide electric field was the reason for the enhanced transient current in trench MIS TDs with thick oxide. The above results were published in *IEEE Transactions on Electron Devices* and presented at *IEDMS 2021* (Best Paper Award), and I am the first author.

Inspired by my internship in TSMC, I want to pursue a career as an R&D engineer developing next-generation semiconductor technologies. The program at Massachusetts Institute of Technology can help me achieve this goal since the Department is known for its strengths in this area. I would be excited to work with Professors Tomás Palacios, Jesús del Alamo, and Max Shulaker. I have been attracted to the idea of doing research on transistors ever since I worked on a topic related to FinFETs during my internship at TSMC. Professor Palacios's work on GaN high electron mobility transistors (HEMTs) aligns with my interest. I would like to study how to maximize the performance of CMOS circuits composed of GaN HEMTs. Prof. del Alamo has worked on InGaSb p-channel FinFETs, which is another research topic that interests me. I am keen to improve the performance of InGaSb pFETs using atomic layer etching and atomic layer deposition *in situ* processes, which might be able to achieve good interface quality in the InGaSb pFETs. Finally, I am intrigued by Prof. Shulaker's research on carbon nanotube (CNT) FETs, including device-level innovations, such as CNT doping by nonstoichiometric oxide, and circuit-level applications like microprocessors and imaging systems.

To sum up, with my strong background knowledge and research experience in semiconductor devices, I am confident that I can contribute to your program's research and reach my full potential with your faculty's guidance.

PS:

1. For further personal information, please refer to my website: **https://jerryjianlin.github.io/**
2. The following URL () is the pdf version of this "Statement of Objectives".