



國立臺灣大學電機資訊學院電子工程學研究所

碩士論文

Graduate Institute of Electronics Engineering

College of Electrical Engineering and Computer Science

National Taiwan University

Master Thesis

具閘極邊界溝槽結構之金氧半穿隧二極體之暫態電流

強化行為

Enhanced Transient Current Behavior in MIS(p) Tunnel

Diode with Gate Edge Trench Structure

林建宇

Jian-Yu Lin

指導教授：胡振國 博士

Advisor: Jenn-Gwo Hwu, Ph.D.

中華民國 110 年 6 月

June 2021



國立臺灣大學碩士學位論文
口試委員會審定書

具閘極邊界溝槽結構之金氧半穿隧二極體之暫態電流強化行為

Enhanced Transient Current Behavior in MIS(p) Tunnel Diode with Gate Edge Trench Structure

本論文係林建宇君（R08943076）在國立臺灣大學電子工程學研究所完成之碩士學位論文，於民國 110 年 6 月 25 日承下列考試委員審查通過及口試及格，特此證明

口試委員：

胡振國

（指導教授）

林致延

胡隱合

系主任、所長

林子豐

中
文
英

Enhanced Transient Current Behavior in MIS(p) Tunnel Diode with Gate Edge Trench Structure

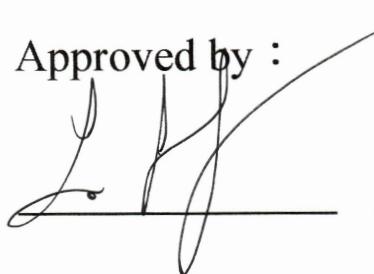
By
Jian-Yu Lin

THESIS

Submitted in partial fulfillment of the requirement
for the degree of Master of Science in Electronics Engineering
at National Taiwan University
Taipei, Taiwan, R.O.C.

June 2021

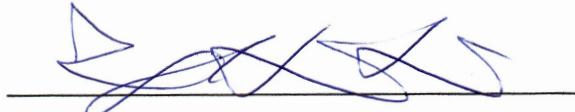
Approved by :

 Pi-kto Hu  Jenn-Gwo Hwu

Advised by :

Jenn-Gwo Hwu

Approved by Director :



誌謝



首次進到實驗室是在大四上的專題研究，從此之後就開始了在 CVLAB 的三年研究生生活：在一開始大四參與的 JDP 計畫，成為了提早進到實驗室與學長姐學習的契機；大四畢業的暑假經老師鼓勵到台積電暑期實習，這段經歷告訴我了還缺乏什麼以及未來該走的方向；此後的碩一、碩二，從一開始的不順利，到在每周的個人 meeting 中逐漸找到研究方向，最終順利寫出論文和發表 paper；非常感謝在這一段時間中，指導老師胡振國教授對我的栽培和耐心，以及在我每次遇到挫折時鼓勵我，給予我建議，成為我繼續支持下去的動力。另外感謝在疫情期間，還抽空幫我口試的兩位口試委員：林致廷教授與胡璧合教授，謝謝你們在口試時給予的寶貴意見，讓我能夠更完善我的碩士論文。

除此之外，能夠完成這份論文還要感謝研究室的各位學長學弟；江子豪學長，你精闢的見解常常給我不同的角度去思考我的研究，也感謝你在吃飯時不吝於分享你自己的想法，常給我不同的反思；許庭昊學長，感謝你之前畢業後還留在實驗室半年，carry 大學部的專題研究和實驗機台；陳柏均學長，謝謝你在 JDP 計畫時教我一些基礎知識，還有教我做實驗的基礎，也謝謝你和幾位學長樹立了良好的碩士論文典範，成為我想要超越的目標；楊詠竣學長，感謝你常帶動實驗室的氣氛，也常常跟大家一起去吃午餐和聊天；林冠文學長，很不好意思常常找你問問題和討論研究，雖然常問很多蠢蠢的問題，但是過程中你都很耐心的給我解答，與我討論，



使我在你身上學到非常多，祝你未來的博士班研究一帆風順；同屆的黃琛云，謝謝你常跟我聊天，之前還常一起修課和參加 JDP 計畫；陳人豪、陳冠竹，感謝你們積極的研究態度，讓我碩士兩年的研究也不斷地努力想要跟上你們的研究腳步，是我努力不懈的動力之一；晚我一年進實驗室的同屆黃崧璋，謝謝你在大三下時一起修量子電子學，還有幫忙 carry 最後的作業，最近一年你帶起了久違的實驗室研究風氣，相信未來實驗室一定會朝更好的方向發展，也祝你博士班研究順利；林津丞學弟，現在應該是實驗室出席率最高的人吧，常常周六來實驗室也可以看到你，以你做實驗的經驗和效率，未來應該研究會進行得很順利；林俊諭學弟，有非常多特別的研究 idea，常常給我一些不同的角度來看研究；林彥瑜學妹，比較少跟你聊到，也祝你和其他幾位學弟妹未來研究順利。

另外想特別感謝在暑期實習期間有給予各項幫助的 CVLAB 學長姊：林黃玄、廖建舜、周佳儒、林建智、李宗鴻等等，你們對我的熱情，讓當時初出茅廬來實習的我，不至於對工作環境感到緊張害怕，也謝謝你們每天都來找我吃午餐；非常謝謝當時帶領我的詹前泰主管，不論是在研究工作和生涯規劃方面都給了我不少意見，遇到您並且能夠在您手下工作，是一生之幸。

最後，感謝我親愛的家人，陪伴我在台大六年的生活，沒有你們的支持和鼓勵，我應該沒辦法從頭到尾走完這段路程。

林建宇

2021.7.2



摘要

本論文旨在研究一種新型結構的金氧半穿隧二極體，其全名為具閘極邊界溝槽結構之金氧半穿隧二極體(以下簡稱為溝槽元件)。與傳統的平面型金氧半穿隧二極體相比(以下簡稱為平面元件)，此新型結構元件在電流-電壓、記憶體留存、記憶體耐久特性中不只展現了較低的反偏壓電流，更擁有較大的暫態電流，比如說在 1000 個週期的記憶體耐久量測中，溝槽結構元件的記憶體電流窗口比傳統結構元件大了 25 倍。從高頻率的電容-電壓量測中可以推測，溝槽元件中的少數載子數量(即電子)較平面元件少，這也被認為是造成其反偏壓電流較小的原因。此外，根據以上的推論，我們提出了一個模型來解釋為何溝槽元件的暫態電流行為比平面元件要來的更強。最後，不同等效氧化層厚度對暫態電流的影響也在本論文中被詳細探討，並且我們發現溝槽元件在很大的等效氧化層厚度範圍內，都具有比平面元件更好的記憶體電流窗口。由於較強的暫態電流特性與其所致的較佳記憶體電流窗口，具閘極邊界溝槽結構之金氧半穿隧二極體擁有作為揮發性記憶體的潛力。

關鍵字：金氧半穿隧二極體、暫態電流行為、溝槽結構、記憶體特性。



Abstract

In this thesis, a new type of metal-insulator-semiconductor (MIS) tunnel diode (TD), trench MIS TD, was investigated. From current–voltage characteristics, memory retention, and memory endurance measurements, it is found the trench MIS TDs not only have lower reverse bias current but also show stronger transient current compared to traditional planar structure MIS TDs. For example, in the 1000 cycles memory endurance test, a 25 times larger memory current window (CW) in trench devices than the CW of planar devices was observed. The reason for the lower reverse bias current is attributed to the fewer minority carriers (electrons) in trench MIS TDs, which is supported by the high-frequency C–V measurement. As for the enhanced transient behavior of trench MIS TDs, a mechanism based on the understanding of fewer minority carriers in trench devices was proposed to explain the observation. Eventually, the effect of different equivalent oxide thicknesses (EOTs) on the CW was examined. It was found that the trench devices have better memory CW in a wide EOT range. Because of the enhanced transient behavior leading to better memory CW, trench MIS TDs have the potential to serve as volatile memory devices.

Key words: metal-insulator-semiconductor (MIS) tunnel diode (TD), transient current behavior, trench structure, memory property.

Contents



感謝	I
摘要	III
Abstract	IV
Contents.....	V
Figure Captions	VII
Chapter 1 Introduction	1
1-1. Motivation	2
1-2. Fundamentals of MIS(p) TD	4
1-2-1. Deep Depletion Phenomenon in C-V Curves	4
1-2-2. Thickness Dependency of Reverse Bias Current.....	6
1-2-3. Perimeter Dependency of Reverse Bias Current	7
1-3. Equivalent Oxide Thickness (EOT) Extraction	9
1-4. Summary	11
Chapter 2 I-V and C-V Characteristics of Trench MIS TDs.....	16
2-1. Introduction	17
2-2. Experimental	17
2-3. Results and Discussion.....	19
2-3-1. Lower Reverse Bias Current of Trench MIS TDs	20
2-3-2. Similar Forward Bias Capacitance and Current of MIS TDs	24
2-4. Summary	25
Chapter 3 Transient Current Behavior of Trench MIS TDs	32



3-1. Introduction	33
3-2. Results and Discussion.....	33
3-2-1. I-V Characteristics with Different Sweeping Rates	33
3-2-2. Memory Retention and Endurance Properties	35
3-2-3. Thermal Equilibrium Model of Transient Current	37
3-2-4. Verification of Thermal Equilibrium Model	41
3-2-4-1. Experimental Results	41
3-2-4-2. Transient TCAD Simulation.....	43
3-3. Summary	45
Chapter 4 Influence of EOT on Transient Current Behavior of MIS TDs.....	60
4-1. Introduction	61
4-2. Results and Discussion.....	61
4-2-1. I-V Curves with Different EOTs	61
4-2-2. Memory Retention Properties with Different EOTs.....	62
4-2-3. Transient TCAD Simulation of MIS TDs with Different EOTs	64
4-3. Summary	66
Chapter 5 Conclusion and Future Work.....	75
5-1. Conclusion.....	76
5-2. Future Work	78
5-2-1. The Distance Between the Gate Edge and the Trench Edge	78
5-2-2. The Depth of the Trench	79
5-2-3. Effect of Different Sidewall Materials on the Transient Current Behavior.	79
References.....	87

Figure Captions



- Fig. 1-1.** The measured I–V characteristics of MIS (p) TDs with various oxide thicknesses. The inset shows the fabricated MIS (p) TD structure. [20] 12
- Fig. 1-2.** C–V curves of MIS TDs at 100kHz with different oxide thicknesses (d_{ox}). The voltage sweeping rate is about 167 mV/s. 12
- Fig. 1-3.** C–V curves that zoom in the reverse bias region of **Fig. 1-2**. Arrows are used to represent the place where deep depletion happens under different d_{ox} 13
- Fig. 1-4.** The schematic band diagrams of MIS (p) TDs with (a) thinner oxide and (b) thicker oxide at forward bias region ($V_{TD} < 0$ V). 13
- Fig. 1-5.** The schematic band diagrams of MIS (p) TDs with (a) thinner oxide and (b) thicker oxide at reverse bias region ($V_{TD} > 0$ V). 14
- Fig. 1-6.** The measured I–V characteristics of MIS TDs with various device areas. The dotted lines are the currents per unit device area, and the solid lines are the currents per unit device perimeter. The inset shows that the saturation current of MIS TD is mainly flowing through the edge of the device due to the fringing field effect. E_{edge} is the fringing electric field. [20]..... 14
- Fig. 1-7.** Schematic (a) device structure and (b) band diagram (along x—x' cutline) of MIS TD. The fringing electric field (red arrows) is shown in (a) and denoted as E_{edge} 15
- Fig. 1-8.** Equivalent circuit models of MIS capacitor: (a) parallel circuit model for C–V measurement and (b) three-element model that considers corrected (or true) capacitance (C_c), effective device resistance (R_p), and series resistance (R_s). 15

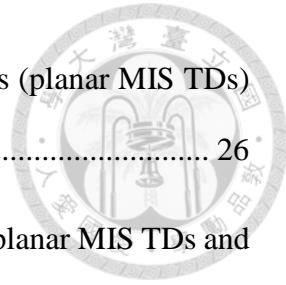


Fig. 2-1. The experimental process flow of planar structure MIS TDs (planar MIS TDs) and trench structure MIS TDs (trench MIS TDs)..... 26

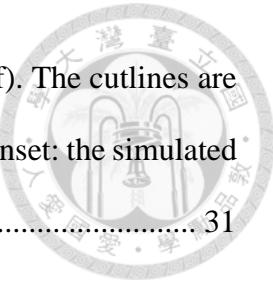
Fig. 2-2. Top views and schematic cross-section views of traditional planar MIS TDs and the proposed trench structure MIS TDs. The top Al metal gates were all patterned as the circle shape with a radius of $170\ \mu\text{m}$ 27

Fig. 2-3. Current–voltage characteristics of the planar and the trench MIS TDs with two voltage sweeping directions. At $V_G > 0\ \text{V}$, MIS TDs are in reverse bias region. At $V_G < 0\ \text{V}$, MIS TDs are in forward bias region. Solid: voltage sweeps forward. Dash: voltage sweeps backward. 27

Fig. 2-4. High-frequency capacitance–voltage (C–V) characteristics of planar and trench MIS TDs with two voltage sweeping directions. Inset: zooming in part of the C–V curves, which shows trench MIS TD is in deep depletion state while planar MIS TD is in inversion state. The voltage sweeping rate is about $167\ \text{mV/s}$. Solid: voltage sweeps forward from $-2\ \text{V}$ to $+2\ \text{V}$. Dash: voltage sweeps backward from $+2\text{V}$ to -2V 28

Fig. 2-5. Schematic cross-sections of (a) planar and (b) trench MIS TDs with fringing field distribution. Red arrows indicate the fringing field. The purple region represents the range of the depletion region. For planar MIS TDs, minority carriers (electrons) from the neighbor substrate can supply to the gate edge of the devices. Schematic band diagrams of the (c) planar and (d) trench devices at $V_G = +2\ \text{V}$ along the cutlines X–X' in (a) and (b). 29

Fig. 2-6. (a) The structure parameters of planar MIS TD and (b) trench MIS TD used in Silvaco TCAD simulation. The simulated depletion region of (c) the planar and (d) trench MIS TD. The simulated total electric field in (e) planar MIS TD and (f) trench MIS TD, confirming the smaller fringing oxide field in trench devices.



(g) The total electric field in SiO_2 along the cutlines in (e), (f). The cutlines are located at 0.2 nm downward from the bottom of the Al gate. Inset: the simulated V_{ox} values.	31
---	----

Fig. 3-1. Current–voltage characteristics of the planar and the trench MIS TDs with two voltage sweeping directions and different voltage sweeping rates (dV/dt). At $V_G > 0$ V, MIS TDs are in reverse bias region. At $V_G < 0$ V, MIS TDs are in forward bias region. Solid: voltage sweeps forward. Dash: voltage sweeps backward.

.....	46
-------	----

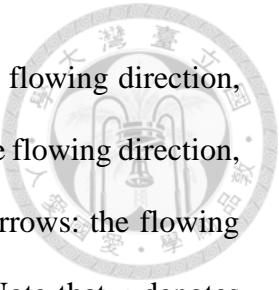
Fig. 3-2. Write and read voltage operation settings used in the memory measurement.

.....	46
-------	----

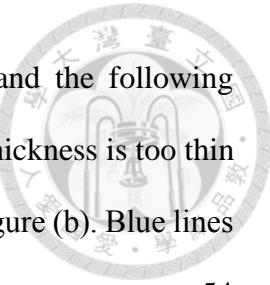
Fig. 3-3. (a) Retention characteristics of planar and trench MIS TDs. The measurement steps and settings are shown in **Fig. 3-2**. (b) The extracted current window from (a). Current window (CW) is defined as the read current difference between “0” and “−1” states. Retention time (R.T.) is defined as the amount of time it takes for CW to drop to half of its original value at time = 0^+ s..... 47

Fig. 3-4. (a) Endurance characteristics of planar and trench MIS TDs. The endurance read current data is read at time = 0^+ s in each read operation. (b) Extracted CW from the endurance measurement in (a). The write and read voltage settings are the same as **Fig. 3-2**. 48

Fig. 3-5. Schematic MIS TDs structures that are used to explain “Thermal Equilibrium Model”. At write “−1” condition, both (a) planar and (b) trench devices accumulate inversion charges (Q_{inv}), namely electrons (represented by −), near the SiO_2 / Si interface. At the beginning ($t = 0^+$ s) of read “−1” condition, because the switching from write to read operation is so quick, the Q_{inv} of (c) planar and (d) trench MIS TDs have no time to be recombined or disappear and



become excess inversion carriers (Q_{excess}). Blue arrows: the flowing direction, which results in / $I_{h(T)}$ / current flow, of holes. Red arrows: the flowing direction, which results in / $I_{e(T)}$ / current flow, of electrons. Purple arrows: the flowing direction, which results in / $I_{h(D)}$ / current flow, of holes. Note that e denotes electron current, h denotes hole current, T denotes tunneling current, and D denotes displacement current.	49
Fig. 3-6. Schematic band diagrams that demonstrate the concept of “Thermal Equilibrium Model” along the cutline x—x’ in Fig. 3-5 . At $t = 0^+$ s of read “–1” condition, because the switching from write to read operation is so quick, the Q_{inv} of (c) planar and (d) trench MIS TDs have no time to be recombined or disappear and become excess inversion carriers (Q_{excess}).....	50
Fig. 3-7. Write and read voltage operation settings used to verify “Thermal Equilibrium Model”.....	51
Fig. 3-8. Endurance measurement of (a) planar MIS TD and (b) trench MIS TD using the write and read voltage conditions in Fig. 3-7 . The endurance read current data is read at time = 0^+ s in each read operation. Solid: read “0” state. Open: read “–1” state.....	52
Fig. 3-9. Retention characteristics of a planar MIS TD with positive read “–1” current. The measurement steps are the same as in Fig. 3-2	53
Fig. 3-10. Schematic band diagrams used to explain the positive transient current of planar MIS TDs. (a) The band diagram of planar MIS TD at region 1 of Fig. 3-9 . (b) The band diagram of planar MIS TD at region 2 of Fig. 3-9	53
Fig. 3-11. (a) Schematic structure of trench MIS TDs used in the transient TCAD simulation. d_{ox} ranges from 2 nm to 6 nm. (b) The trench MIS TD structure	



of TCAD simulation. This will help readers to understand the following contour figures more easily. Note that because the oxide thickness is too thin under μm scale, the oxide layer can barely be seen in subfigure (b). Blue lines are used to mark the position of the oxide layer. 54

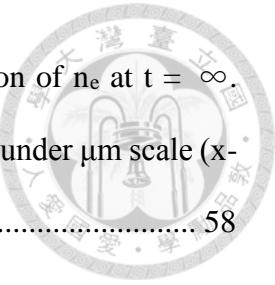
Fig. 3-12. Simulation steps of transient TCAD. At first, steady-state solutions of trench MIS TDs at $V_G = 0\text{V}$ and $+2\text{ V}$ are performed. Secondly, transient solution switching from $V_G = +2\text{ V}$ to 0 V , i.e. write “ -1 ” and read “ -1 ” operations, is conducted. Please note that write “ 0 ” and read “ 0 ” operations are not simulated for the expected zero transient current. 54

Fig. 3-13. Simulated retention result of trench MIS TD with $d_{\text{ox}} = 3.2\text{ nm}$ under read “ -1 ” operation. Negative read “ -1 ” current that is similar to the experimental result in **Fig. 3-3(a)** can be observed. 55

Fig. 3-14. Contour plots of total y-component current density ($J_{\text{total}, y}$) of trench MIS TD at (a) time = 1.35 ms , (b) time = 2.35 ms , (c) time = 3.35 ms , (d) time = 4.35 ms , and (e) time = 30 ms under read “ -1 ” operation. As the time goes from 1.35 to 30 ms , the magnitude of $J_{\text{total}, y}$ reduces, which is consistent with the simulation in **Fig. 3-13**. 56

Fig. 3-15. Contour plots of electron concentration (n_e) under log scale. (a) Steady-state n_e at $V_G = +2\text{ V}$. (b–e) Transient n_e under read “ -1 ” operation from $t = 1.35\text{--}30\text{ ms}$ after V_G switches to 0 V . (f) Steady-state n_e at $V_G = 0\text{ V}$, which can be viewed as the transient solution of n_e at $t = \infty$ 57

Fig. 3-16. Contour plots of electron concentration (n_e) under linear scale. Notice that compared to **Fig. 3-15**, this figure zooms in the region close to $\text{SiO}_2 / \text{Si(p)}$ interface. (a) Steady-state n_e at $V_G = +2\text{ V}$. (b–e) Transient n_e under read “ -1 ” operation from $t = 1.35\text{--}30\text{ ms}$ after V_G switches to 0 V . (f) Steady-state n_e



at $V_G = 0$ V, which can be viewed as the transient solution of n_e at $t = \infty$.
Since the oxide layer (3.2 nm) at trench sidewall is too thin under μm scale (x-axis), it cannot be seen in the figures..... 58

Fig. 3-17. Contour plots of recombination rate (Recom.) near the $\text{SiO}_2 / \text{Si(p)}$ interface of trench MIS TD under read “-1” operation at (a) time = 1.35 ms, (b) time = 2.35 ms, (c) time = 4.35 ms, and (d) time = 30 ms under read “-1” operation. As the time goes, the recombination rate will reduce because of the fewer excess electrons. 59

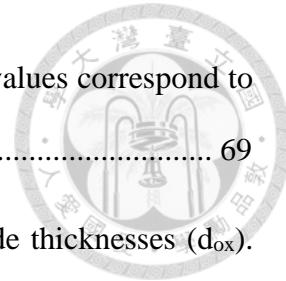
Fig. 4-1. I–V characteristics of planar MIS TDs with various EOTs. Solid: voltage sweeps forward. Dash: voltage sweeps backward. Voltage sweeping rate is about 75 mV/s. 67

Fig. 4-2. I–V characteristics of trench MIS TDs with various EOTs. The zero current voltage (ZCV) of device with $EOT = 3.25$ nm at backward direction is 0.46 V. Solid: voltage sweeps forward. Dash: voltage sweeps backward. Voltage sweeping rate is about 75 mV/s. 67

Fig. 4-3. Retention properties of planar MIS TDs with various EOTs (3.2–2.5 nm). Since read “0” current of all MIS TDs are close to 0, they are not shown in the figure for simplicity. 68

Fig. 4-4. Retention properties of trench MIS TDs with various EOTs (3.25–2.5 nm). Since read “0” current of all MIS TDs are close to 0, they are not shown in the figure for simplicity. 68

Fig. 4-5. The current window (CW) of MIS TDs with different EOTs. The gate current at forward bias (-2 V) is used to represent the EOT. The thicker the EOT is, the



smaller the $|I_G| @ -2 \text{ V}$ becomes. Different $|I_G| @ -2 \text{ V}$ values correspond to different EOT values of the devices..... 69

Fig. 4-6. Schematic band diagrams of MIS TDs with different oxide thicknesses (d_{ox})

Q_{inv} : total inversion charges. P_t : oxide tunneling probability. 69

Fig. 4-7. Simulated retention result of trench MIS TDs with various d_{ox} under read “-1” operation. Although the time scale is different from the measured results in **Fig. 4-4**, the trend (thicker oxide have better transient current) of the negative current is almost the same as in **Fig. 4-4**. In the transient TCAD simulation, write “0” and read “0” operations are not simulated for the expected zero read “0” current.

..... 70

Fig. 4-8. Measured and simulated CW of trench MIS TDs at different d_{ox} (or EOTs).

Since write “0” and read “0” operations were not simulated in the study, the simulated CW values are extracted by the modified definition, $|read @ t = 1.35 \text{ ms}|$, based on (3-9). Red symbols: simulated data. Blue symbols: measured data of trench devices that were shown before in **Fig. 4-5**.

..... 71

Fig. 4-9. Simulated CW of trench MIS TDs at different $d_{ox} = 2. More simulated CW data compared to **Fig. 4-8** are added to enable the discussion of optimal CW..... 71$

Fig. 4-10. Contour plots of electron concentration (n_e) of trench MIS TDs with (a–b) $d_{ox} = 4 \text{ nm}$, (c–d) $d_{ox} = 3 \text{ nm}$, and (e–f) $d_{ox} = 2 \text{ nm}$ under log scale. (a), (c), and (e) show the transient n_e under read “-1” operation at $t = 1.35 \text{ ms}$. (b), (d), and (f) show the steady-state n_e at $V_G = 0 \text{ V}$, which can be viewed as the transient solution of n_e at $t = \infty$ 72

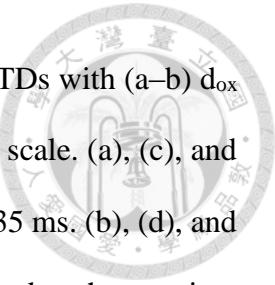


Fig. 4-11. Contour plots of electron concentration (n_e) of trench MIS TDs with (a–b) $d_{ox} = 4$ nm, (c–d) $d_{ox} = 3$ nm, and (e–f) $d_{ox} = 2$ nm under linear scale. (a), (c), and (e) show the transient n_e under read “–1” operation at $t = 1.35$ ms. (b), (d), and (f) show the steady-state n_e at $V_G = 0$ V, which can be viewed as the transient solution of n_e at $t = \infty$ 73

Fig. 4-12. Extracted excess carrier concentration (n_{excess}) of trench MIS TDs with (a) $d_{ox} = 4$ nm, (b) $d_{ox} = 3$ nm, and (c) $d_{ox} = 2$ nm under linear scale..... 74

Fig. 5-1. (a) Schematic structure of trench MIS TDs. (b) TEM image of the trench MIS TDs. The distance L between the trench edge and the metal gate is about 500.2 nm..... 81

Fig. 5-2. Fabrication process flow of trench MIS TDs. Because of the Al wet etching process (step 4), the generated undercut creates distance between Al and trench edge..... 82

Fig. 5-3. (a) Trench MIS TD with undercut distance L will have equivalently larger V_{ox} because of more minority carriers supply. (b) Trench MIS TD without undercut will have equivalently smaller V_{ox} considering fewer minority carriers supply from neighbor substrate..... 83

Fig. 5-4. (a) Schematic structure of trench MIS TDs. (b) TEM image of the trench MIS TDs. The depth of the trench structure D is about 339.7 nm. 83

Fig. 5-5. Fabrication process flow of trench MIS TDs with SiO_2 sidewall. 84

Fig. 5-6. I–V curves of planar and trench MIS TDs with voltage sweeping rate ≈ 75 mV/s. Trench: Al_2O_3 represents the trench MIS TDs with sputtered Al_2O_3 sidewall. Trench: SiO_2 represents the trench MIS TDs with ANO SiO_2 sidewall. Solid: voltage sweeps forward. Dash: voltage sweeps backward. 85

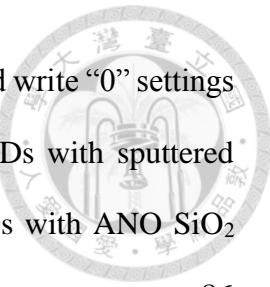


Fig. 5-7. Endurance characteristics using the same read, write “-1”, and write “0” settings as in **Fig. 3-2**. Trench: Al₂O₃ represents the trench MIS TDs with sputtered Al₂O₃ sidewall. Trench: SiO₂ represents the trench MIS TDs with ANO SiO₂ sidewall 86



Chapter 1

Introduction

1-1. Motivation

1-2. Fundamentals of MIS(p) TD

1-2-1. Deep Depletion Phenomenon in C–V Curves

1-2-2. Thickness Dependency of Reverse Bias Current

1-2-3. Perimeter Dependency of Reverse Bias Current

1-3. Equivalent Oxide Thickness (EOT) Extraction

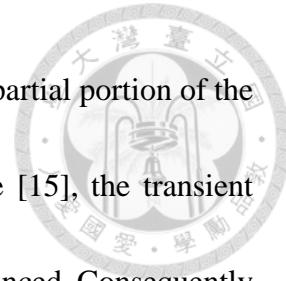
1-4. Summary



1-1. Motivation

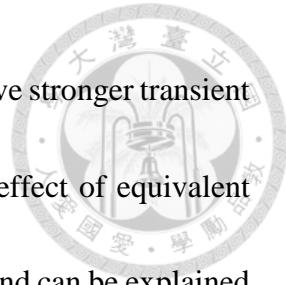
NOWADAYS, memory devices have become more and more important since the large demand for memory in applications such as 5G, Internet of things (IoT), Artificial intelligence (AI), and Big data. As a result, the study of transient behavior in semiconductor devices is getting critical as well because transient behavior represents the potential of electronic devices for memory applications. For example, traditional one transistor and one capacitor (1T-1C) dynamic random access memory (DRAM), which was invented by Dr. Robert Dennard from IBM in the late 1960s [1], uses the capacitor to store charges, and the memory states can be read by the voltage transient behavior caused by the charges stored in the capacitor. Besides 1T-1C DRAM, capacitor-less DRAM or 1T-DRAM, which has attracted great attention in recent years for its smaller cell size [2], [3], also exploits current transient behavior of the 1T-DRAM to store memory states [4]-[6].

Metal-insulator-semiconductor (MIS) tunnel diodes (TDs), which possess the advantages of low power consumption, CMOS compatible process, and low fabrication cost, have been studied for many years [7]-[10], and can be used as solar cell [11], photodetector [12], temperature sensor [13], etc. Furthermore, in recent research [14], [15], MIS TDs have been found to demonstrate strong transient behavior by changing their structure from traditional planar structure MIS TD (planar MIS TD) into



unconventional structures. To be more specific, by thinning down a partial portion of the gate metal thickness [14] or thickening the oxide at the gate edge [15], the transient current behavior of the altered structures MIS TDs can be largely enhanced. Consequently, by utilizing this transient current behavior, MIS TDs have the potential to be used as memory devices. However, the above-mentioned special structures all need two masks fabrication processes, which increases the fabrication cost and the process complexity.

In this thesis, a new type of MIS TDs, trench structure MIS TDs (trench MIS TDs), which also demonstrate enhanced transient current behavior compared with planar MIS TDs, is proposed. Most importantly, trench MIS TDs only need one mask process to fabricate, which is different from the previous work [14], [15]. The structure of this thesis is organized as follows. In **Chapter 1**, some background knowledge about MIS TDs is illustrated for better understanding of the discussion in the following thesis. Before the discussion of transient current behavior of trench MIS TDs, it is essential to first identify the difference of steady-state behavior between trench and planar MIS TDs. As a result, in **Chapter 2**, how trench structure affects the steady-state characteristics of MIS TDs will be investigated, using planar MIS TDs as comparisons. In **Chapter 3**, the transient current behavior of trench devices was then comprehensively examined by current-voltage (I-V) characteristics with different sweeping rates, memory retention, and memory endurance measurements. Based on the discussion in **Chapter 2**, “Thermal



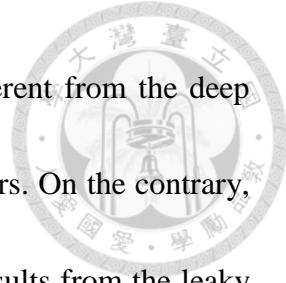
Equilibrium Model” was proposed to explain why trench MIS TDs have stronger transient current response compared to planar MIS TDs. In **Chapter 4**, the effect of equivalent oxide thickness (EOT) on the transient current behavior is identified and can be explained by the proposed model in **Chapter 3**. Eventually, the conclusion and the future work are stated in **Chapter 5**.

1-2. Fundamentals of MIS(p) TD

MIS TDs are devices that have similar structures to conventional MOS capacitors [see the inset of **Fig. 1-1**], except that they have insulator layers that are thin enough to allow electrons to tunnel through the oxide. Therefore, MIS TDs demonstrate a diode-like current–voltage (I–V) characteristic, as shown in **Fig. 1-1**. The I–V curves can be roughly split into two regions, the forward bias region ($V_{TD} < 0$ V) and the reverse bias region ($V_{TD} > 0$ V).

1-2-1. Deep Depletion Phenomenon in C–V Curves

If the insulator layer of MIS TDs is thin enough, a steady-state deep depletion phenomenon can be observed when a large gate voltage (V_G) is applied to the devices. To be more specific, in high-frequency capacitance–voltage (C–V) measurements [see **Fig. 1-2** and **Fig. 1-3**], the capacitance value will start to decrease as V_G keeps increasing, which implicates a wider and deeper depletion region, i.e. deep depletion phenomenon.



It is worth mentioning that this steady-state deep depletion is different from the deep depletion caused by the fast voltage sweeping rate in MOS capacitors. On the contrary, the steady-state deep depletion observed in **Fig. 1-2** and **Fig. 1-3** results from the leaky tunneling oxide. To explain this concept, one can start from the gate bias equation of MIS TDs, which can be written as

$$\begin{aligned} V_G &= V_{FB} + V_{ox} + \psi_s \\ &= V_{FB} - \frac{Q_d + Q_i}{C_{ox}} + \psi_s \end{aligned} \quad (1-1)$$

where V_{FB} is the flat band voltage, V_{ox} is the oxide voltage drop, ψ_s is the surface potential of Si, Q_d is the depletion charge density per unit area, Q_i is the inversion charge density per unit area, and C_{ox} is the oxide capacitance per unit area.

As the V_G increases, the $\text{SiO}_2 / \text{Si(p)}$ interface cannot accumulate more inversion carriers (electrons) not only because electrons can tunnel through the oxide easily at high V_G , but also because the generation rate of minority carriers is unable to keep up with the tunneling rate of the electrons. Hence, the almost pinned Q_i will lead to larger band bending in Si(p) substrate to balance the increasing positive voltage at metal gate [according to (1-1)] and result in the deep depletion phenomenon. **Fig. 1-3** exhibits a classical steady-state deep depletion phenomenon that the capacitance value of the three MIS TDs all start to decrease at a high gate voltage (marked with arrows).

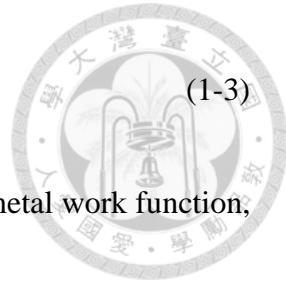
1-2-2. Thickness Dependency of Reverse Bias Current

Fig. 1-1 also demonstrates the I-V curves of MIS TDs with different oxide thicknesses (d_{ox}). At forward bias region ($V_{TD} < 0$ V), the current magnitude would decrease as d_{ox} increases since thicker oxide would lead to smaller tunneling probability for carriers [see **Fig. 1-4**]. Nonetheless, at reverse bias region, a totally different trend can be observed. To be more specific, the saturation current (e.g. $I_{TD} @ +2$ V) would increase when the d_{ox} becomes thicker, which seems to be counter-intuitive and incomprehensible. As a result, an effect called Schottky barrier height (SBH) modulation was proposed to explain this interesting phenomenon. To better illustrate the concept of SBH modulation, the schematic band diagrams of MIS TDs with thinner and thicker oxide at reverse bias ($V_{TD} > 0$ V) are shown in **Fig. 1-5**. Besides electron current component ($|I_e|$), hole current component ($|I_h|$) also contributes to the total saturation current and can be expressed as [9], [10], [16] :

$$I_h = A^* A_{eff} P_t T^2 \exp\left(-\frac{q\phi_{Bp}^*}{k_B T}\right) \left[1 - \exp\left(-\frac{qV_{TD}}{k_B T}\right)\right] \quad (1-2)$$

where A^* is the effective Richardson constant for holes, A_{eff} is the effective current flowing area, P_t is the tunneling probability, T is the temperature, q is the electron charge, ϕ_{Bp}^* is the hole-effective Schottky barrier height (SBH) [see **Fig. 1-5**], and k_B is Boltzmann's constant. The hole-effective SBH ϕ_{Bp}^* is related to the oxide voltage V_{ox} [10], which can be written as:

$$q\phi_{Bp}^* = q\chi_s - q\Phi_M + E_g - qV_{ox} \quad (1-3)$$



where χ_s is the electron affinity of the semiconductor, Φ_M is the metal work function, and E_g is the semiconductor bandgap.

When the same V_{TD} is applied to MIS TDs, larger V_{ox} will drop on thicker oxide and further lead to smaller ϕ_{Bp}^* in the MIS TD with thicker oxide by (1-3). According to (1-2), thicker oxide MIS (p) TDs will have larger hole current ($|I_h|$) than thinner oxide devices since their ϕ_{Bp}^* are smaller [see **Fig. 1-5(b)**]. It is noteworthy that although P_t decreases as d_{ox} becomes larger, the overall $|I_h|$ will still increase because $|I_h|$ is exponentially modulated by the reduced ϕ_{Bp}^* . The above description, also called SBH modulation, can be used to explain the larger saturation current in MIS (p) TD when the oxide becomes thicker.

1-2-3. Perimeter Dependency of Reverse Bias Current

Another intriguing property of MIS (p) TDs is the perimeter dependency of the reverse bias current. **Fig. 1-6** shows the I-V curves of MIS (p) TDs with various device areas. The dotted lines exhibit the current per unit area, yet the solid lines represent the current per unit perimeter of the electrode. Moreover, at forward bias region ($V_{TD} < 0$ V), one can notice that the I-V curves from different devices merge well [see the dotted lines in **Fig. 1-6**] after they are divided by their corresponding electrode gate area. This implies the forward bias current is dominated by the bulk-flowing current.



At reverse bias region ($V_{TD} > 0$ V), however, the current is proportional to the electrode perimeter rather than the area of MIS TDs, which can be confirmed by the nearly overlapped solid lines I-V curves in **Fig. 1-6**. The reason for the perimeter-dependent reverse bias current is the strong fringing electric field (E_{edge}) at the gate edge of MIS TDs, as shown in **Fig. 1-7(a)**. Remember that in the previous **Section 1-2-2**, in addition to electron current component ($|I_e|$), hole current component ($|I_h|$) also plays an important role in the total reverse bias current. Because of the strong fringing electric field, the corresponding large oxide voltage drop (V_{ox}) would result in the decrease of ϕ_{Bp}^* under the gate edge [by (1-3)]. According to (1-2) and (1-3), I_h that flows through device edge is much bigger than it flows through bulk region since I_h is exponentially modulated by the reduced ϕ_{Bp}^* [see **Fig. 1-7(b)**]. This explains why the reverse bias current of MIS TDs is dominated by the edge-flowing current (perimeter-dependent current).

People may notice that in **Fig. 1-6**, the forward bias current (at $V_{TD} < 0$ V) which is dependent on the device area does not seem to reflect the influence of fringing field. This is because of the lack of SBH when MIS TD is at forward bias, as shown in **Fig. 1-4**. As a result, the forward bias current is not exponentially modulated by the fringing field and V_{ox} . To be more specific, even if the fringing field still exists at $V_{TD} < 0$ V, the edge-



flowing current only account for minor portion of the total forward bias current, which is completely different from the case of reverse bias current.

1-3. Equivalent Oxide Thickness (EOT) Extraction

Usually, equivalent oxide thickness (EOT) of a MOS capacitor can be extracted by the capacitance measured at strong accumulation region by (1-4).

$$C_{acc} \approx C_{ox} = \frac{\epsilon_{ox}}{d_{ox}} A \quad (1-4)$$

where C_{acc} is the capacitance measured at accumulation region, C_{ox} is the oxide capacitance, ϵ_{ox} is the permittivity of the oxide, A is the device area, and d_{ox} is the equivalent oxide thickness (EOT). However, when EOT of the MOS capacitor becomes too small (namely, the case of MIS TDs), the gate direct tunneling current would increase rapidly, which makes quasi-static capacitance measurement difficult. Although high-frequency capacitance measurement can be utilized to overcome the gate leakage problem since the capacitive current is dominant at high-frequency, this results in another problem. That is, at high-frequency region, the series resistance would become critical because of the low impedance of the capacitor, which further gives rise to the frequency dispersion of C_{acc} . Consequently, (1-4) can not be used to determine the EOT of MIS TDs. Instead, the method proposed in [17], which will be described briefly in the following, is adopted to extract the EOT correctly.

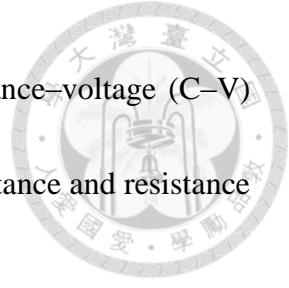


Fig. 1-8(a) shows the parallel circuit model used for capacitance–voltage (C–V) measurement of MIS TDs. C_m and R_m represent the measured capacitance and resistance value. Total impedance of the parallel circuit is given by

$$Z = \frac{D_m - j}{\omega C_m (1 + D_m^2)} \quad (1-5)$$

where $D_m = 1 / (\omega R_m C_m)$ is the dissipation factor and ω is the radian frequency. At high frequency, however, series resistance can not be neglected for the small impedance of C_m ($= -j / (\omega C_m)$). Thus, using the three-element circuit model [shown in **Fig. 1-8(b)**] to extract the true capacitance (C_c) of MIS TDs is more accurate. The total impedance of the three-element circuit is given by

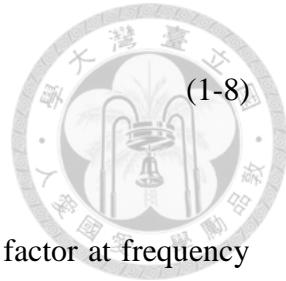
$$Z = R_s + \frac{R_p(1 - j\omega C_c R_p)}{1 + \omega^2 C_c^2 R_p^2} \quad (1-6)$$

where R_s is the series resistance of the substrate and the gate, R_p represents the effective device resistance due to tunneling (leakage) through the gate oxide, and C_c is the corrected (true) capacitance of the MIS TDs. By equating the imaginary parts of (1-5) and (1-6), one can obtain

$$\frac{1 + \omega^2 C_c^2 R_p^2}{C_c R_p^2} = \omega^2 C_m (1 + D_m^2) \quad (1-7)$$

By measuring the capacitance and the dissipation factors at two different frequencies, substituting them into (1-7) for each frequency, and solving the unknown C_c , the following equation can be deduced:

$$C_c = \frac{f_1^2 C_{m1} (1 + D_{m1}^2) - f_2^2 C_{m2} (1 + D_{m2}^2)}{f_1^2 - f_2^2}$$



where C_{m1} and D_{m1} are the measured capacitance and dissipation factor at frequency f_1 , and C_{m2} and D_{m2} are the measured capacitance and dissipation factor at frequency f_2 . Eventually, the EOT of MIS TDs can be determined by fitting the two-frequency corrected capacitance–voltage ($C_c - V_G$) curves to the simulated C–V curves using the quantum simulator developed by Berkeley Device Group [18], [19].

1-4. Summary

In this chapter, the motivation of the thesis and some background knowledge about MIS TDs were illustrated. Among these sections, the basic current–voltage (I–V) property and the deep depletion phenomenon of C–V curves are of importance because they would enable people to understand the properties of trench structure MIS TDs (Trench MIS TDs) discussed in the following chapters. Particularly, the fact that the reverse bias current of MIS TDs is edge-flowing current dominated is the key reason for how forming trench structure under the gate edge of MIS TDs has such a great impact on the transient current behavior of MIS TDs.

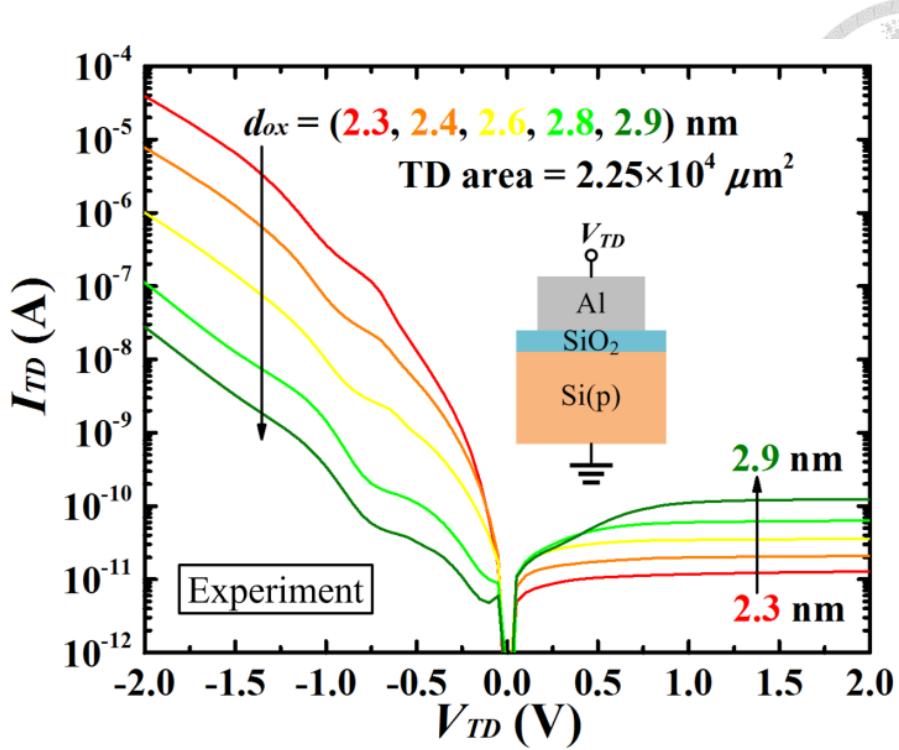


Fig. 1-1. The measured I–V characteristics of MIS (p) TDs with various oxide thicknesses. The inset shows the fabricated MIS (p) TD structure. [20]

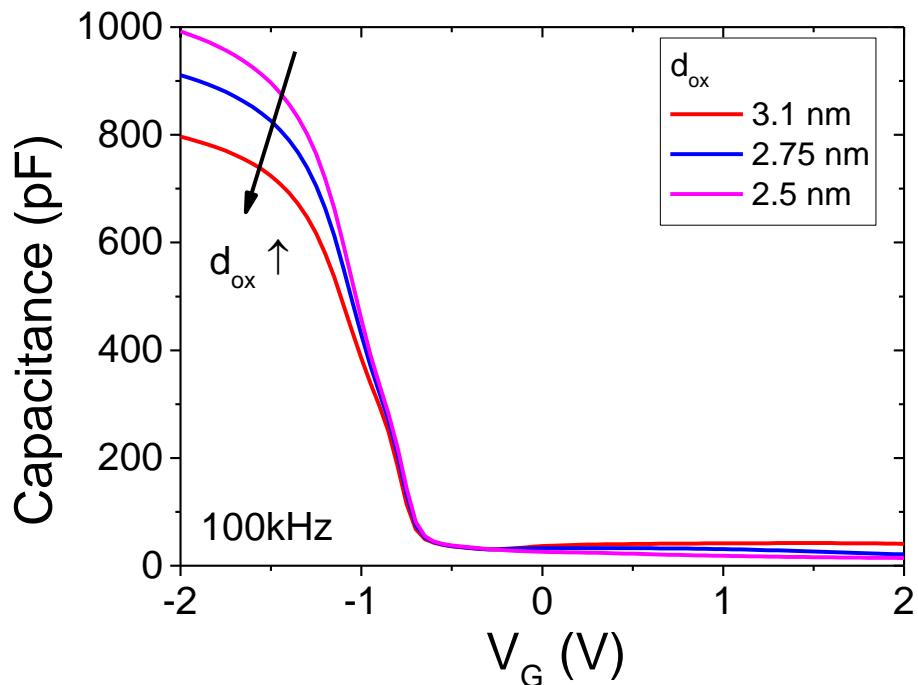


Fig. 1-2. C–V curves of MIS TDs at 100kHz with different oxide thicknesses (d_{ox}). The voltage sweeping rate is about 167 mV/s.

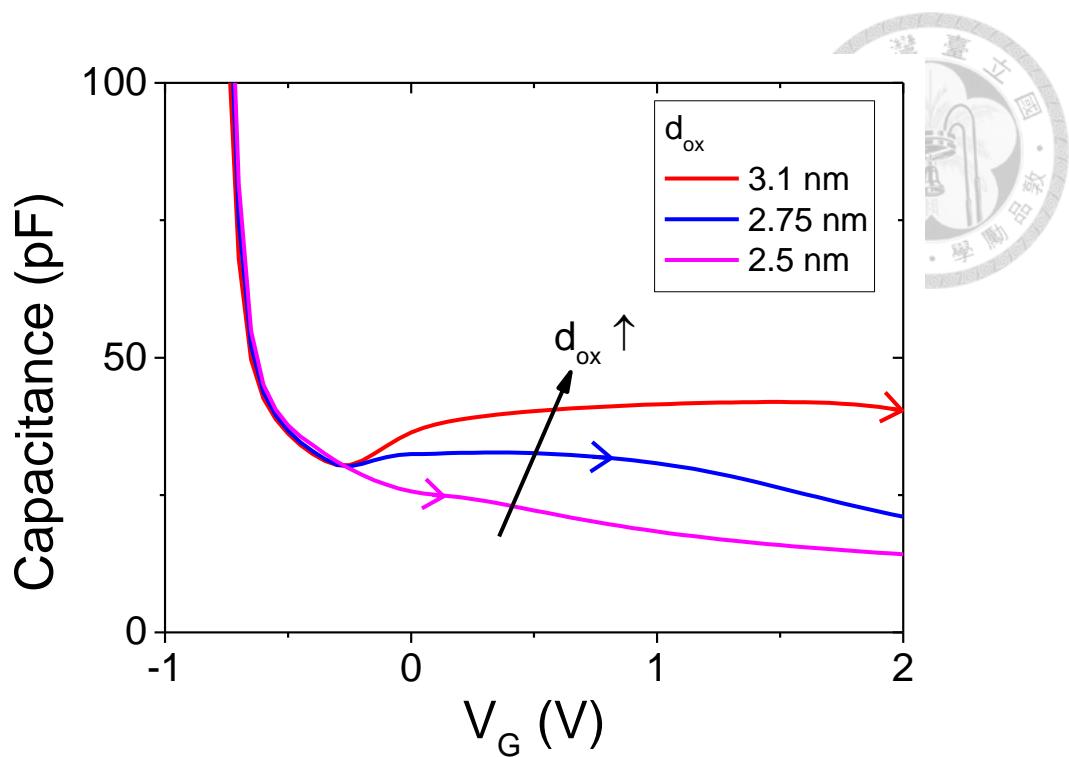


Fig. 1-3. C–V curves that zoom in the reverse bias region of **Fig. 1-2**. Arrows are used to represent the place where deep depletion happens under different d_{ox} .

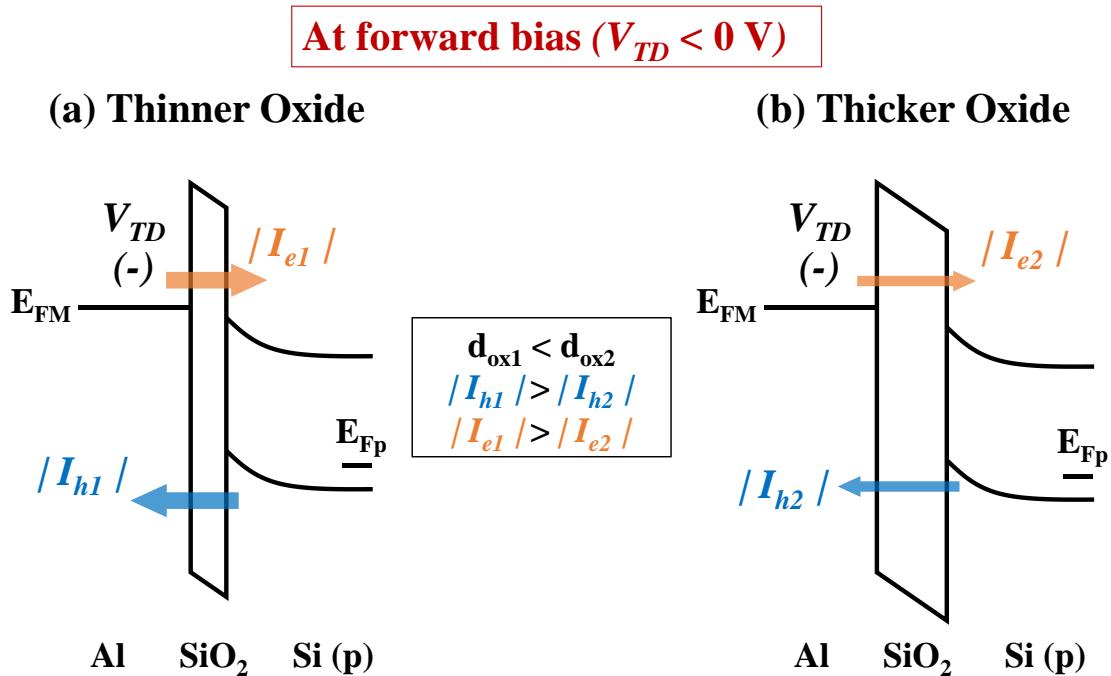


Fig. 1-4. The schematic band diagrams of MIS (p) TDs with (a) thinner oxide and (b) thicker oxide at forward bias region ($V_{TD} < 0$ V).

At reverse bias ($V_{TD} > 0$ V)

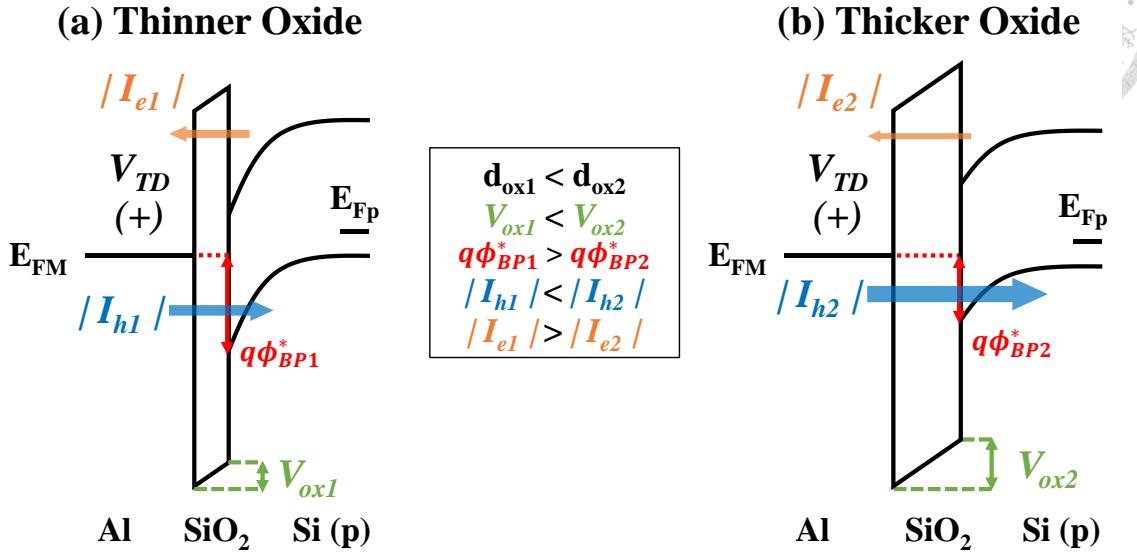


Fig. 1-5. The schematic band diagrams of MIS (p) TDs with (a) thinner oxide and (b) thicker oxide at reverse bias region ($V_{TD} > 0$ V).

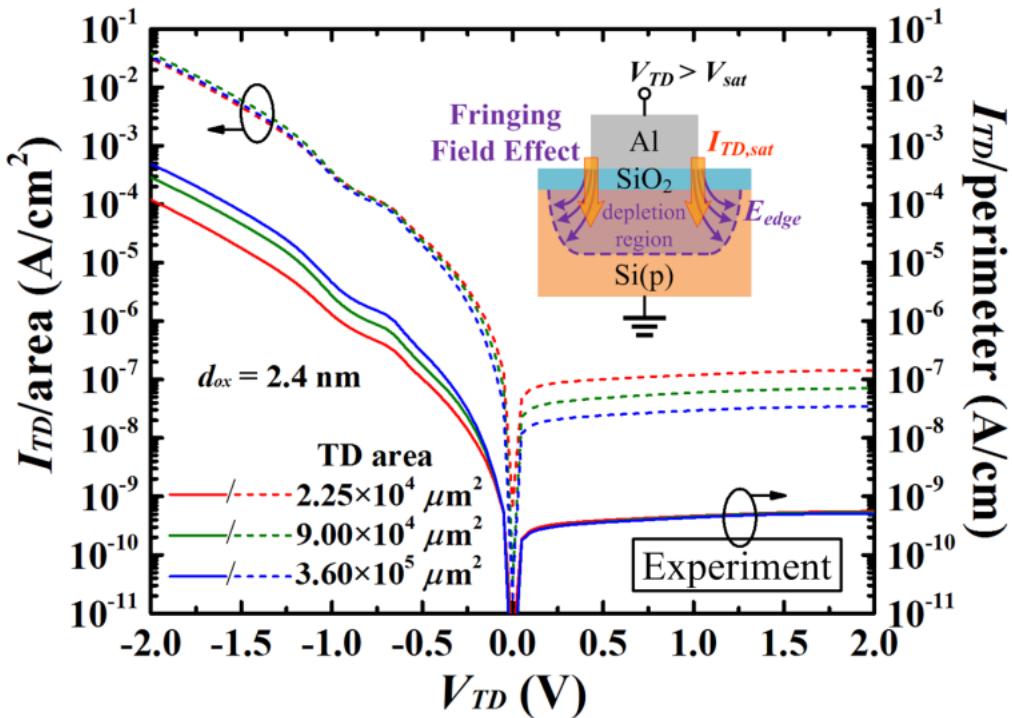


Fig. 1-6. The measured I–V characteristics of MIS TDs with various device areas. The dotted lines are the currents per unit device area, and the solid lines are the currents per unit device perimeter. The inset shows that the saturation current of MIS TD is mainly flowing through the edge of the device due to the fringing field effect. E_{edge} is the fringing electric field. [20]

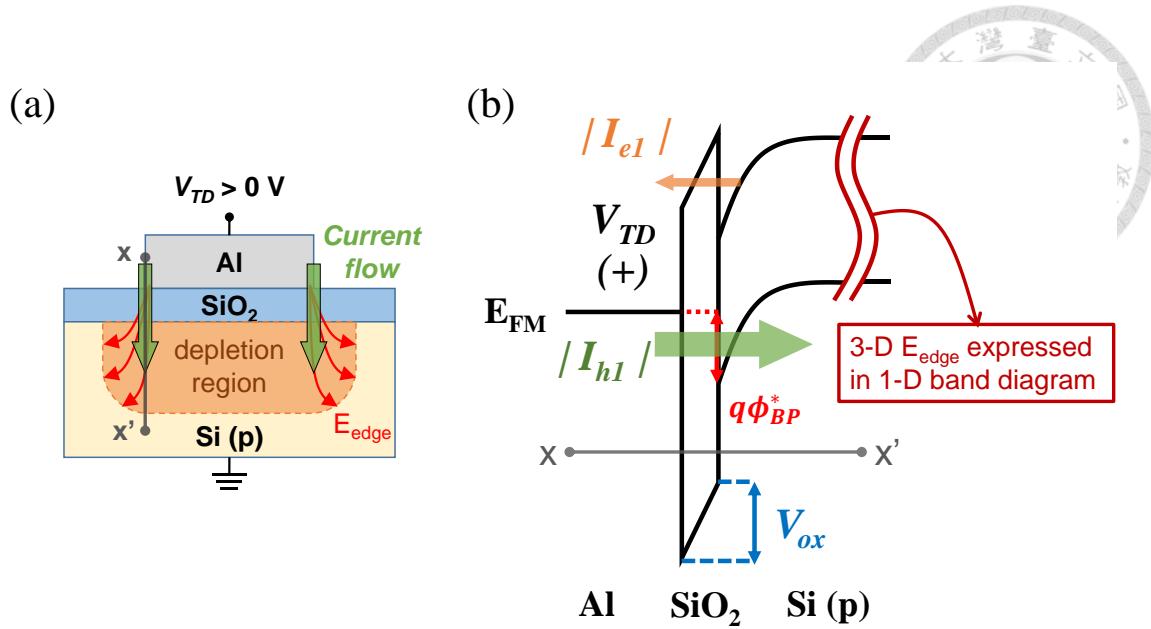


Fig. 1-7. Schematic (a) device structure and (b) band diagram (along $x-x'$ cutline) of MIS TD. The fringing electric field (red arrows) is shown in (a) and denoted as E_{edge} .

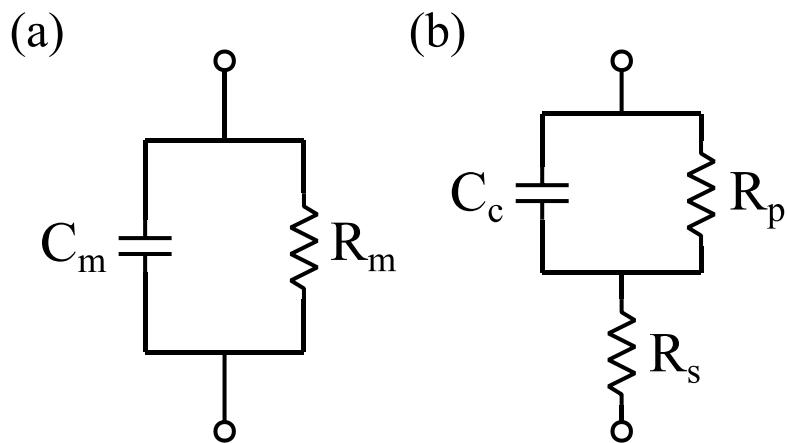


Fig. 1-8. Equivalent circuit models of MIS capacitor: (a) parallel circuit model for C-V measurement and (b) three-element model that considers corrected (or true) capacitance (C_c), effective device resistance (R_p), and series resistance (R_s).

Chapter 2

I–V and C–V Characteristics of Trench MIS TDs



2-1. Introduction

2-2. Experimental

2-3. Results and Discussion

2-3-1. Lower Reverse Bias Current of Trench MIS TDs

2-3-2. Similar Forward Bias Capacitance and Current of MIS TDs

2-4. Summary



2-1. Introduction

In the previous chapter, some background knowledge of MIS(p) TDs was illustrated.

However, this understanding of MIS(p) TDs is based on conventional planar structure MIS TDs (denoted as planar MIS TDs). As for the MIS TDs with gate edge trench structure (denoted as trench MIS TDs) proposed in this thesis, we still need to investigate their basic electrical characteristics (such as current-voltage (I-V) and capacitance-voltage (C-V) properties) and the difference of these characteristics between planar and trench MIS TDs. As a result, in this chapter, the discussion of C-V and I-V properties of trench devices was first focused on. Specifically, the steady-state I-V behavior will be thoroughly examined. This part of discussion is beneficial to understanding the enhanced transient current behavior of trench devices in **Chapter 3**.

2-2. Experimental

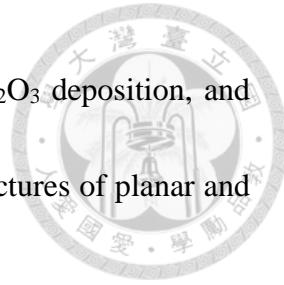
The process flow of fabricated devices is shown in **Fig. 2-1** and will be described in the following. Boron-doped p-type (100)-oriented silicon wafers with a resistivity of 1– $10 \Omega \cdot \text{cm}$ (doping concentration is around $1 \times 10^{16} \text{ cm}^{-3}$) were used as the substrate. After standard Radio Cooperation of America (RCA) cleaning process, anodic oxidation (ANO) was adopted to grow a layer of SiO_2 in deionized water under room temperature. Rapid thermal annealing (RTA) was then performed under a 20-torr N_2 ambient at 950°C for 15



s. Next, a layer of 250 nm thick aluminum metal was thermally evaporated and patterned by photolithography and wet etching, which forms the metal gates of MIS TDs. It should be noted that after the wet etching process, the photoresist (PR) on the aluminum layer was kept for the following process.

By using this PR layer as a soft mask, reactive ion etching (RIE) was employed to etch the Si substrate outside the metal gate and a trench structure was formed at the gate edge. Since the etched Si substrate was exposed to the air after the RIE process, after dipping buffered oxide etchant (BOE) to remove the native oxide, a layer of Al_2O_3 was deposited by *in situ* oxidation of dc sputtering to prevent the device from degradation caused by moisture in the air. In the dc sputtering process, Al targets were sputtered in a mixed Ar/O₂ ambient with a ratio of 1:3 at 2.5×10^{-2} torrs. The details of the *in situ* oxidation sputtering and the reliability analysis of the sputtered films were illustrated and discussed elsewhere [21], [22]. After depositing the Al_2O_3 , PR was removed by the lift-off process. Furnace annealing at 200°C for 10 minutes in N₂ ambient was then used to improve the quality of the Al_2O_3 . Finally, 200 nm thick aluminum layer was deposited by thermal evaporation as the back electrode after removing the backside native oxide by BOE. The abovementioned process finished the fabrication of trench MIS TDs.

Another group of devices, traditional planar structure MIS TDs (planar MIS TDs), were also fabricated as control groups. The difference between the process of trench MIS



TDs and planar MIS TDs is that there were no RIE Si etching, Al_2O_3 deposition, and furnace annealing in the process of planar MIS TDs. Schematic structures of planar and trench MIS TDs are shown in **Fig. 2-2**.

Electrical characteristics of the devices were measured by Agilent B1500A semiconductor device analyzer at room temperature. The equivalent oxide thickness (EOT) of the studied devices was extracted by fitting the two-frequency corrected C–V curves [18] of 100kHz and 10kHz under consideration of quantum mechanical effect [17], as was introduced in **Chapter 1**. The EOT of the studied devices ranges from 2.45 to 3.25 nm.

2-3. Results and Discussion

Fig. 2-3 shows the current–voltage (I–V) characteristics of planar and trench devices with voltage sweeping forward and backward. Compared to planar MIS TDs, there are two major differences in the I–V curves of trench MIS TDs:

- (1) The lower reverse bias steady-state current at large gate voltage (e.g. at $V_G = +2$ V).
- (2) The enhanced transient displacement current, which can be observed from the larger hysteresis in **Fig. 2-3** at the low voltage region.

In the following paragraph of **Section 2-3-1**, the first difference, (1) the lower reverse bias steady-state current of trench devices, will be first discussed since it gives us an

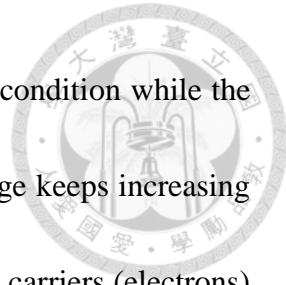


insight into the basic steady-state current difference between the planar and trench MIS TDs. On the other hand, the second difference, (2) the enhanced transient displacement current, will be thoroughly discussed and explained in **Chapter 3**.

2-3-1. Lower Reverse Bias Current of Trench MIS TDs

Compared to the planar device, the trench device shows a smaller reverse bias current at +2 V [see **Fig. 2-3**]. In this work, $I_G @ +2$ V was chosen for comparison because the contribution of the transient displacement current is smaller than the conduction current at high V_G , which can be seen from the relatively smaller deviation of the current from two directions at high voltage than at low voltage region. This indicates that the current of $I_G @ +2$ V is dominated by steady-state conduction current rather than transient displacement current. Remember that the goal of this section is to examine the effect of trench structure on the steady-state current of MIS TDs. Hence, using $I_G @ +2$ V as benchmark can rule out most of the effect of transient current on the total gate current of MIS TDs.

In order to find the cause of the reduced reverse bias current, high-frequency C–V curves were measured, as shown in **Fig. 2-4**. The effective oxide charge number densities (N_{eff}), which are around $2.81 \times 10^{11} \text{ cm}^{-2}$ for planar MIS TD and $3.77 \times 10^{11} \text{ cm}^{-2}$ for trench MIS TD, can be extracted from the flat band voltage shift of the C–V curves. Notice that C–V curves also exhibit big difference between planar and trench devices when $V_G > 0$



V. To be more specific, the planar MIS TD is in stronger inversion condition while the trench MIS TD shows deep depletion phenomenon as the gate voltage keeps increasing to $V_G = +2$ V. This means in planar devices, there are more minority carriers (electrons) supplied from the neighbor Si (p) substrate outside the gate edge to the surface region (at SiO_2 / Si (p) interface) [illustrated in **Fig. 2-5(a)**], which causes the device under stronger inversion. On the contrary, for the case of trench MIS TDs, since a part of Si (p) substrate outside the gate edge is removed, the supply number of minority carriers from the Si (p) reduce accordingly [see **Fig. 2-5(b)**]. As a result, without enough minority carriers supplement, the number of inversion charges in trench device will not increase as V_G becomes larger. The gate bias equation of MIS TDs can be written as [the same as (1-1)]

$$\begin{aligned} V_G &= V_{FB} + V_{ox} + \psi_s \\ &= V_{FB} - \frac{Q_d + Q_i}{C_{ox}} + \psi_s \end{aligned} \quad (2-1)$$

where V_{FB} is the flat band voltage, V_{ox} is the oxide voltage drop, ψ_s is the surface potential of Si, Q_d is the depletion charge density per unit area, Q_i is the inversion charge density per unit area, and C_{ox} is the oxide capacitance per unit area. For trench MIS TDs, according to (2-1), when V_G increases, Q_d and ψ_s will rise because of the almost fixed amount of Q_i , resulting in the enlarging band bending and the deep depletion phenomenon. On the other hand, for planar MIS TDs, because of more supply of Q_i , Q_i can keep



increasing as V_G becomes bigger (under stronger inversion), leading to the less changed Q_d , ψ_s , and the shallower depletion region compared with it of trench devices.

Based on the above discussion, the equivalent V_{ox} of trench MIS TDs is smaller than it of planar MIS TDs at the same positive V_G since more V_G of trench device drops on ψ_s and causes deep depletion. From (2-1) and the same V_{FB} , the larger ψ_s means smaller V_{ox} in trench MIS TDs. **Fig. 2-5(c)** and **Fig. 2-5(d)**, which show the schematic band diagrams of the two kinds of device at $V_G = +2$ V, illustrate the concept of equivalently smaller V_{ox} of trench devices. It is believed that this reduced V_{ox} accounts for the smaller reverse bias current in trench MIS TDs. The relation between V_{ox} and the reverse bias current will be explained in the following.

The steady-state reverse bias current of a planar MIS TD can be written as:

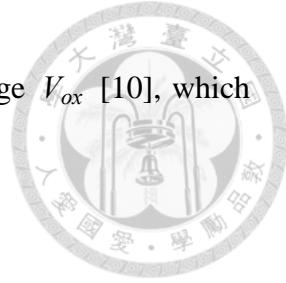
$$I_{steady} = I_{e(T)} + I_{h(T)} \quad (2-2)$$

where $I_{e(T)}$ is the electron tunneling current and $I_{h(T)}$ is the hole tunneling current.

Among (2-2), $I_{h(T)}$ can be expressed as [9], [10], [16]: [same as (1-2)]

$$I_{h(T)} = A^* A_{eff} P_t T^2 \exp\left(-\frac{q\phi_{Bp}^*}{k_B T}\right) \left[1 - \exp\left(-\frac{qV}{k_B T}\right)\right] \quad (2-3)$$

where A^* is the effective Richardson constant for holes, A_{eff} is the effective current flowing area, P_t is the tunneling probability, T is the temperature, q is the electron charge, ϕ_{Bp}^* is the hole-effective Schottky barrier height (SBH), and k_B is Boltzmann's



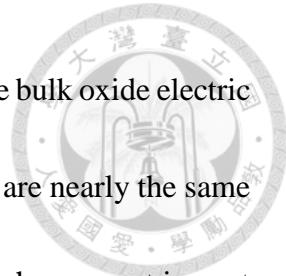
constant. The hole-effective SBH ϕ_{Bp}^* is related to the oxide voltage V_{ox} [10], which can be written as: [same as (1-3)]

$$q\phi_{Bp}^* = q\chi_S - q\Phi_M + E_g - qV_{ox} \quad (2-4)$$

where χ_S is the electron affinity of the semiconductor, Φ_M is the metal work function, E_g is the semiconductor bandgap.

From (2-3) and (2-4), the equivalently larger V_{ox} in planar MIS TDs would result in the decrease of hole-effective SBH ϕ_{Bp}^* , which further leads to larger $I_{h(T)}$ [see **Fig. 2-5(c)** and **Fig. 2-5(d)**]. Since $I_{e(T)}$ is also larger for bigger V_{ox} , it is explicable that planar MIS TDs have larger reverse bias current than trench MIS TDs [by (2-2)].

In **Fig. 2-6**, Silvaco TCAD simulation was used to verify the lower V_{ox} in trench devices. **Fig. 2-6(a)** and **(b)** show the simulated device structures of planar and trench MIS TDs, respectively. The difference between the depletion region of planar and trench devices is demonstrated by the simulation results in **Fig. 2-6(c)** and **(d)**. For trench device, the depletion region under the gate edge is indeed deeper than it of planar MIS TD because of the insufficient minority carriers and smaller V_{ox} . In **Fig. 2-6(e)**, **(f)**, and **(g)**, one can see the difference of V_{ox} between planar and trench devices by the electric field in the oxide layers. The expected larger V_{ox} can be verified by the stronger oxide electric field [see **Fig. 2-6(e)**] and the larger simulated V_{ox} values [see the inset of **Fig. 2-6(g)**] at the gate edge of planar MIS TD compared with trench MIS TD. However, it should be noted

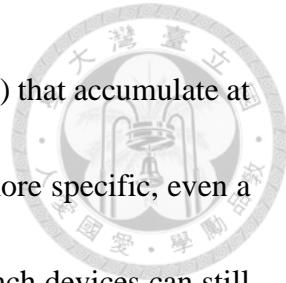


that despite the smaller edge V_{ox} in trench devices, the bulk V_{ox} and the bulk oxide electric field (V_{ox} and total oxide electric field @ $x = +6$ nm) in both devices are nearly the same [see **Fig. 2-6(g)**]. This is reasonable since the removed substrate only has a great impact on the supply of minority carriers to the edge part of MIS TDs. As to the bulk region of the trench device, it is too far away from the trench structure so it remains almost unaffected.

However, based on the simulation results, one may doubt that trench structure can reduce the total reverse bias current that much, e.g. the I_G @ +2 V of the trench device is over one order smaller than it of the planar device [see **Fig. 2-3**], considering only the V_{ox} close to trench edge is lowered [see **Fig. 2-6(g)**]. To address this question, one should remember that for planar MIS TDs, the reverse bias current is dominated by the edge-flowing current, as was introduced in **Section 1-2-3**. Therefore, when part of the substrate outside the gate edge of planar devices is removed, i.e. becoming the case of trench devices, the reduced edge V_{ox} will largely lower the edge-flowing current and, moreover, the total reverse bias current.

2-3-2. Similar Forward Bias Capacitance and Current of MIS TDs

Readers may notice that planar and trench devices have similar capacitance value and forward bias current level at $V_G = -2$ V, which does not reflect the influence of the removed substrate, as shown in **Fig. 2-3** and **Fig. 2-4**. This is because at $V_G = -2$ V, when



MIS TDs are under accumulation region, it is majority carriers (holes) that accumulate at the $\text{SiO}_2 / \text{Si(p)}$ interface of MIS TDs, not minority carriers. To be more specific, even a part of substrate is removed, the rest of the p-type Si substrate in trench devices can still offer enough holes for MIS TDs to maintain in accumulation condition. Therefore, the V_{ox} @ $V_G = -2$ V of planar and trench devices is expected to be the same, which explains the similarity of capacitance and current properties of both kinds of devices at large negative bias (e.g. $V_G = -2$ V).

2-4. Summary

The C–V and I–V characteristics of trench MIS TDs are investigated in this chapter. Fewer minority carriers supplied from the neighbor Si(p) substrate in trench devices might be the key reason for the lack of inversion capacitance signal in C–V and the lower steady-state reverse bias current in I–V of trench MIS TDs compared to planar MIS TDs. To validate the assumption, TCAD simulation was adopted, confirming that the oxide electric field and the V_{ox} at the gate edge of trench MIS TDs is smaller than that of planar MIS TDs as assumed.

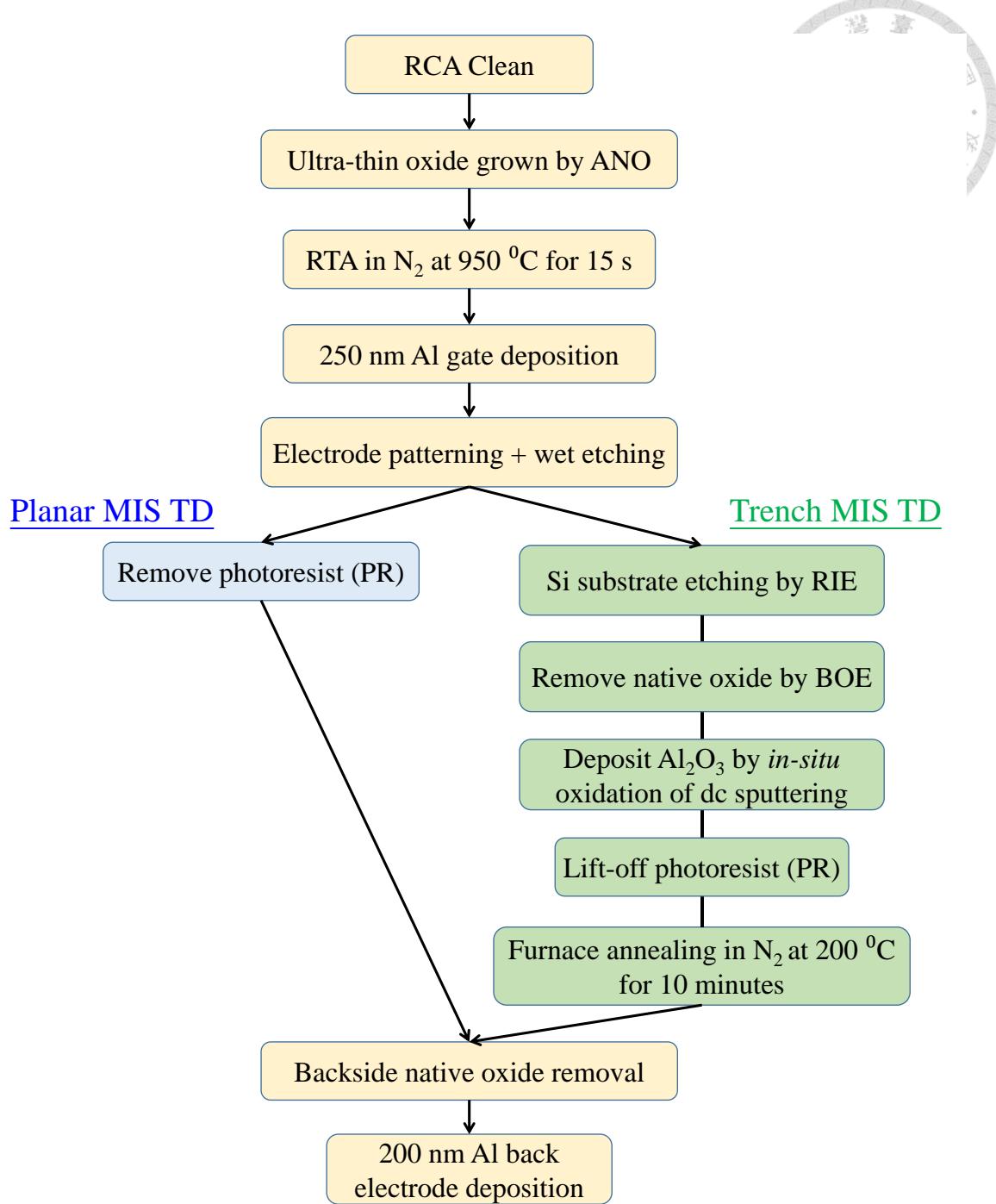


Fig. 2-1. The experimental process flow of planar structure MIS TDs (planar MIS TDs) and trench structure MIS TDs (trench MIS TDs).

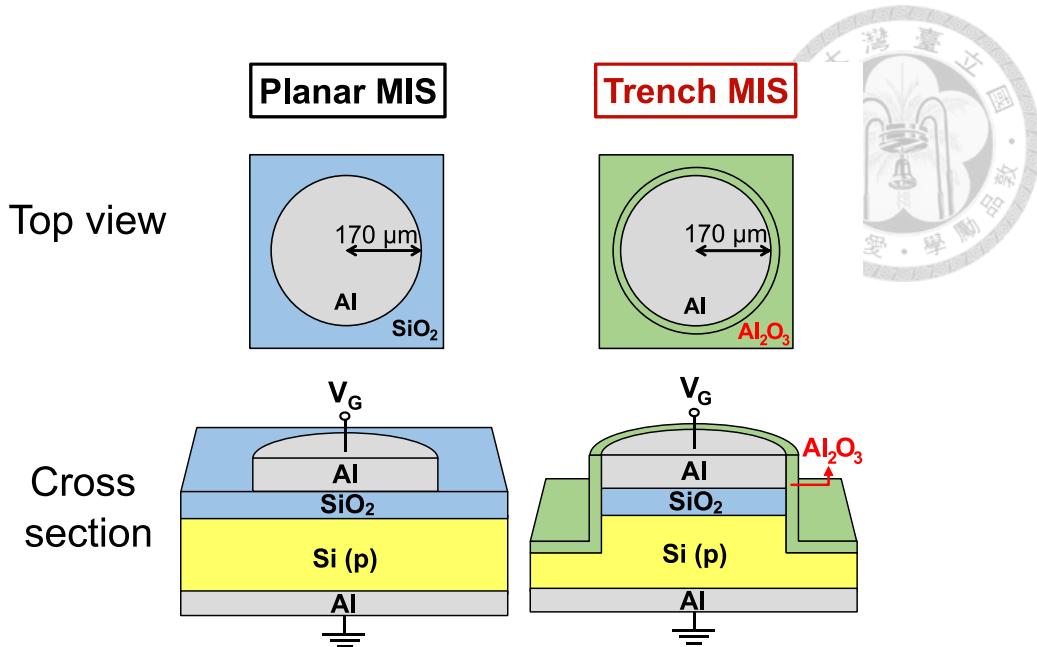


Fig. 2-2. Top views and schematic cross-section views of traditional planar MIS TDs and the proposed trench structure MIS TDs. The top Al metal gates were all patterned as the circle shape with a radius of $170 \mu\text{m}$.

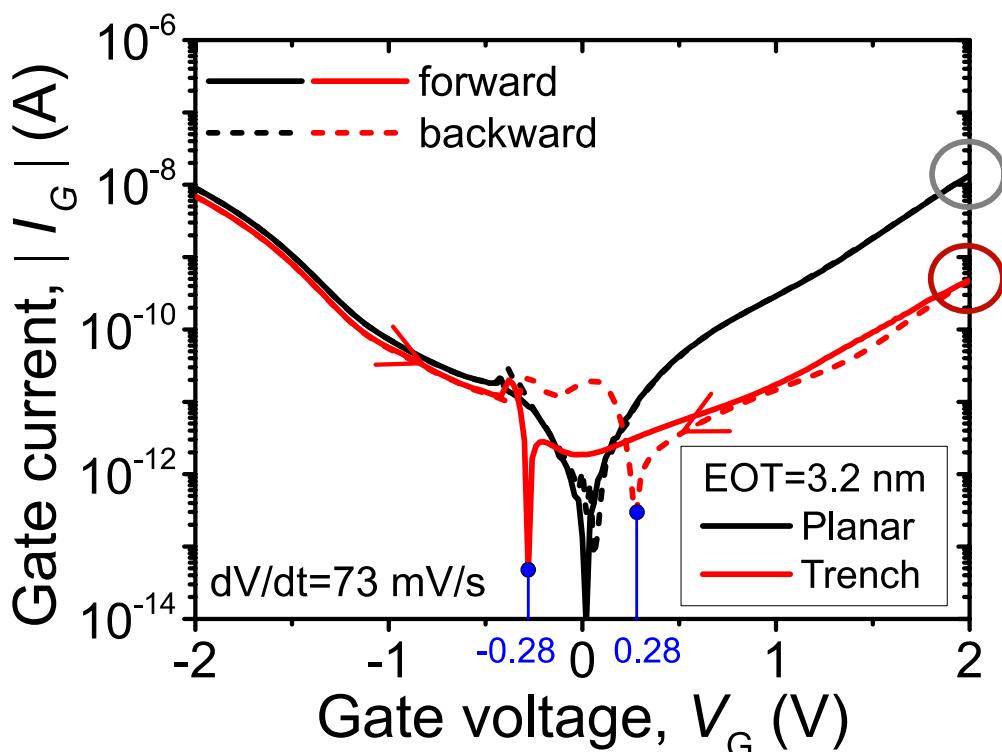


Fig. 2-3. Current–voltage characteristics of the planar and the trench MIS TDs with two voltage sweeping directions. At $V_G > 0 \text{ V}$, MIS TDs are in reverse bias region. At $V_G < 0 \text{ V}$, MIS TDs are in forward bias region. Solid: voltage sweeps forward. Dash: voltage sweeps backward.

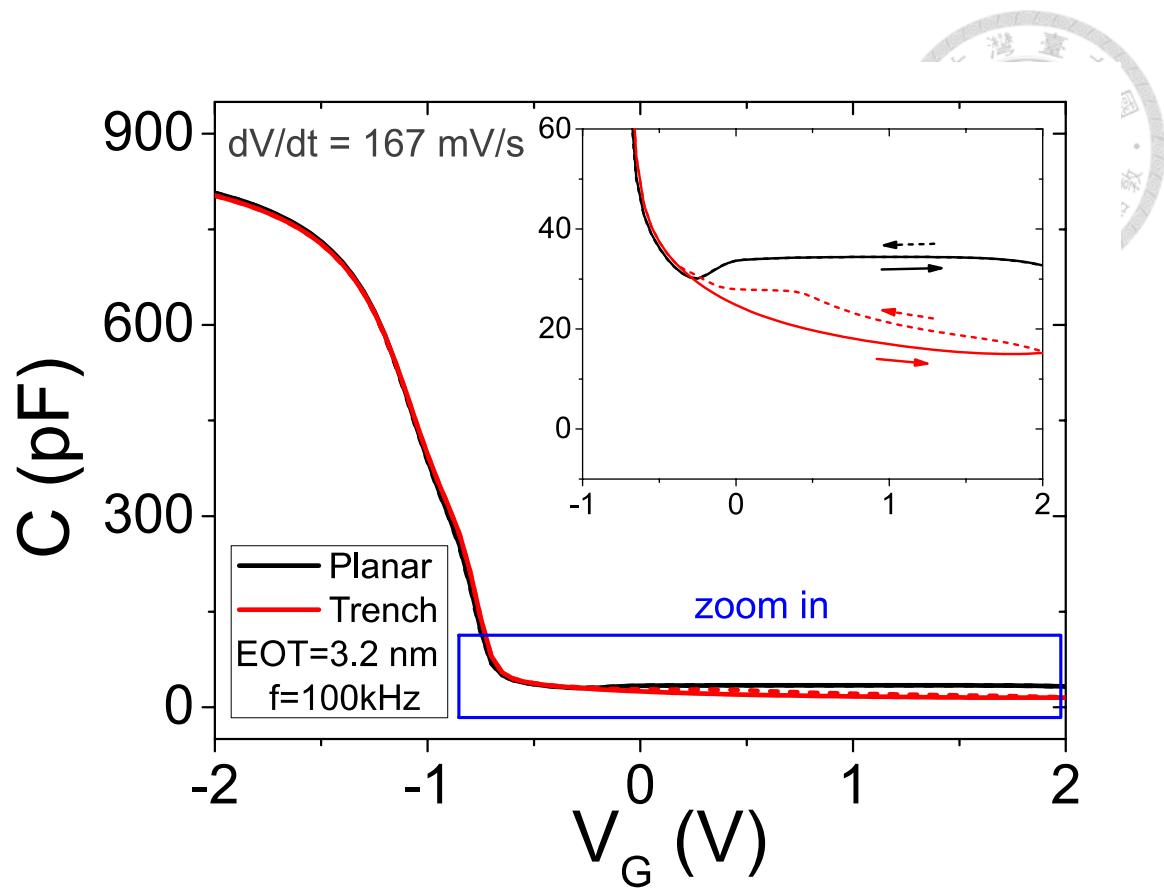


Fig. 2-4. High-frequency capacitance–voltage (C–V) characteristics of planar and trench MIS TDs with two voltage sweeping directions. Inset: zooming in part of the C–V curves, which shows trench MIS TD is in deep depletion state while planar MIS TD is in inversion state. The voltage sweeping rate is about 167 mV/s. Solid: voltage sweeps forward from -2 V to $+2$ V. Dash: voltage sweeps backward from $+2$ V to -2 V.

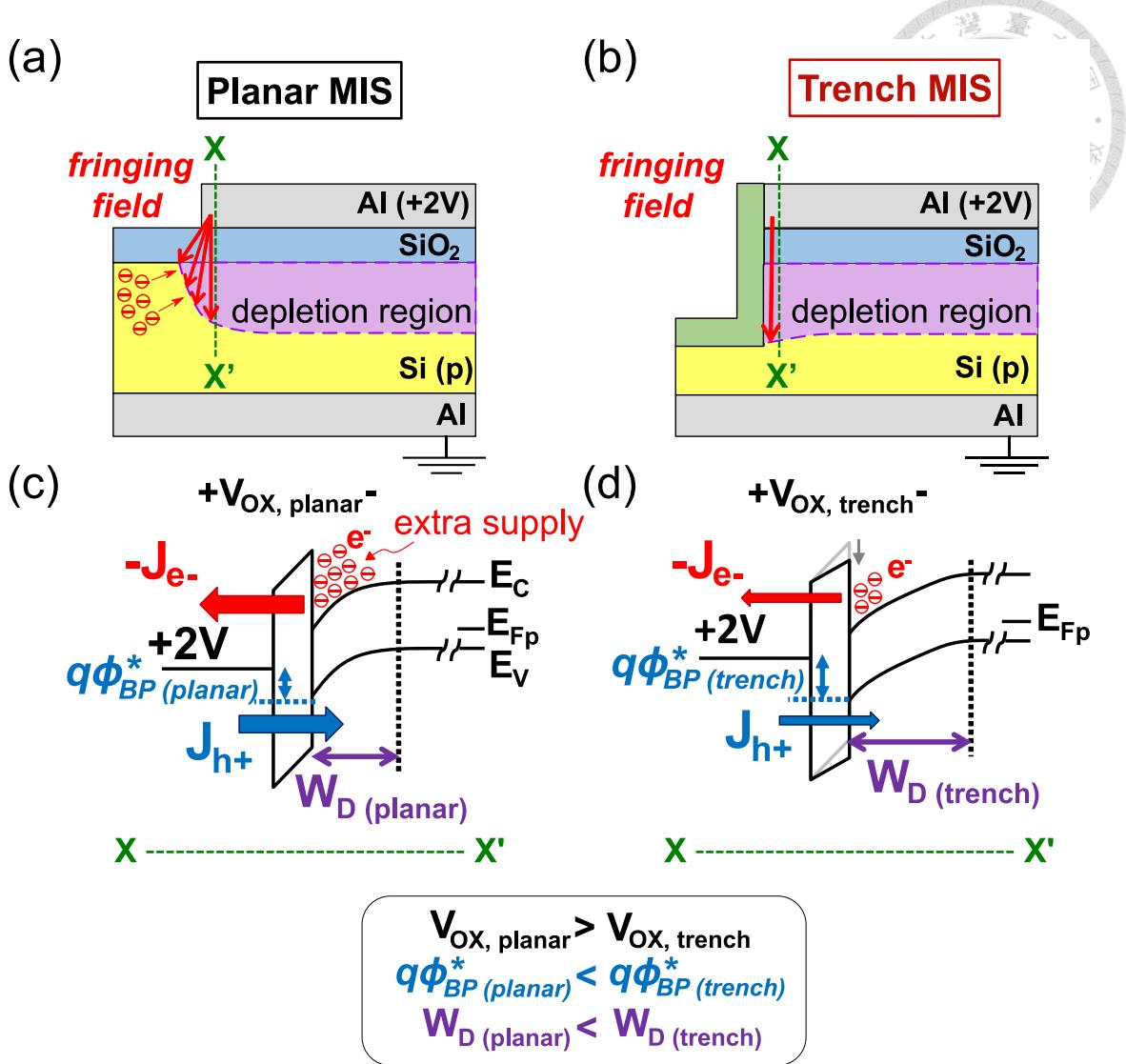
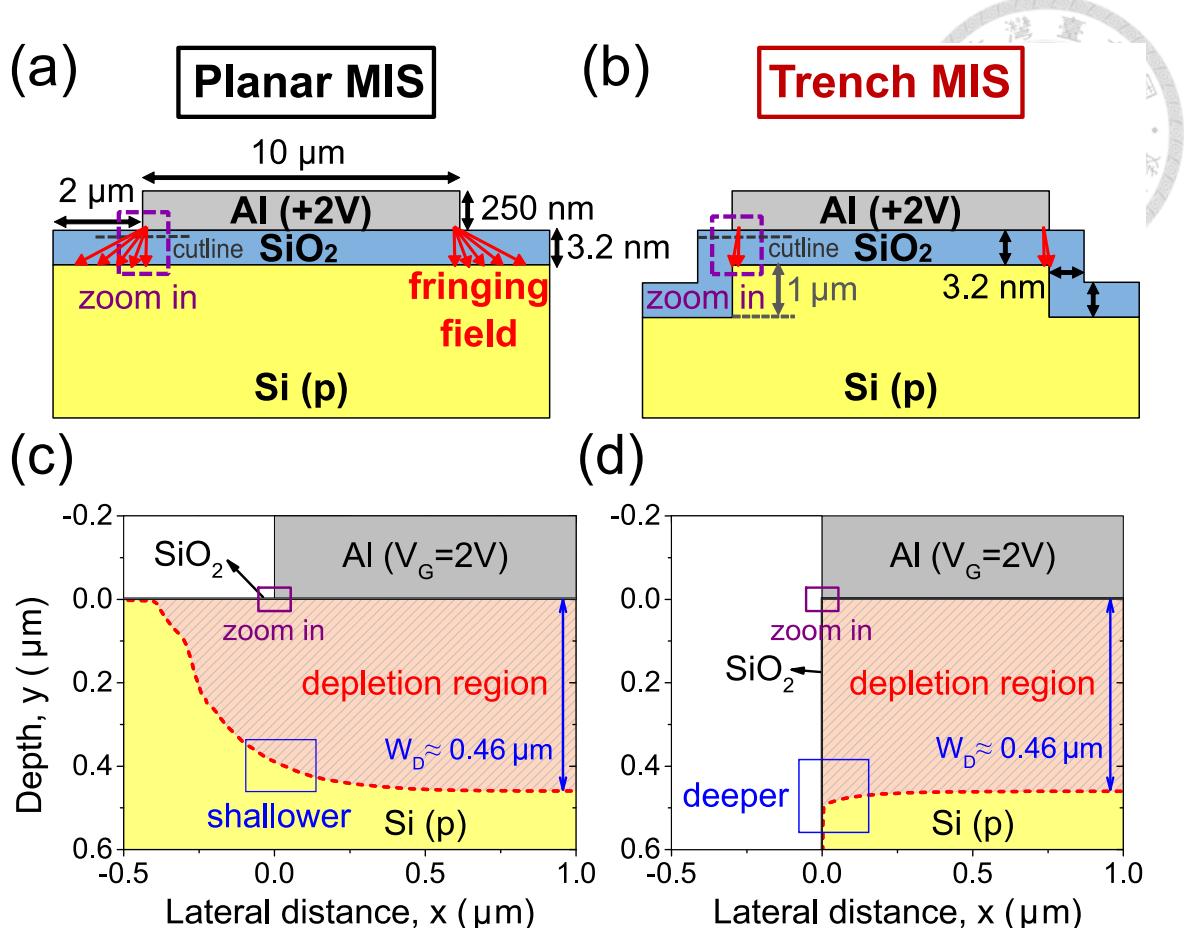


Fig. 2-5. Schematic cross-sections of (a) planar and (b) trench MIS TDs with fringing field distribution. Red arrows indicate the fringing field. The purple region represents the range of the depletion region. For planar MIS TDs, minority carriers (electrons) from the neighbor substrate can supply to the gate edge of the devices. Schematic band diagrams of the (c) planar and (d) trench devices at $V_G = +2$ V along the cutlines X–X' in (a) and (b).



(to be continued)

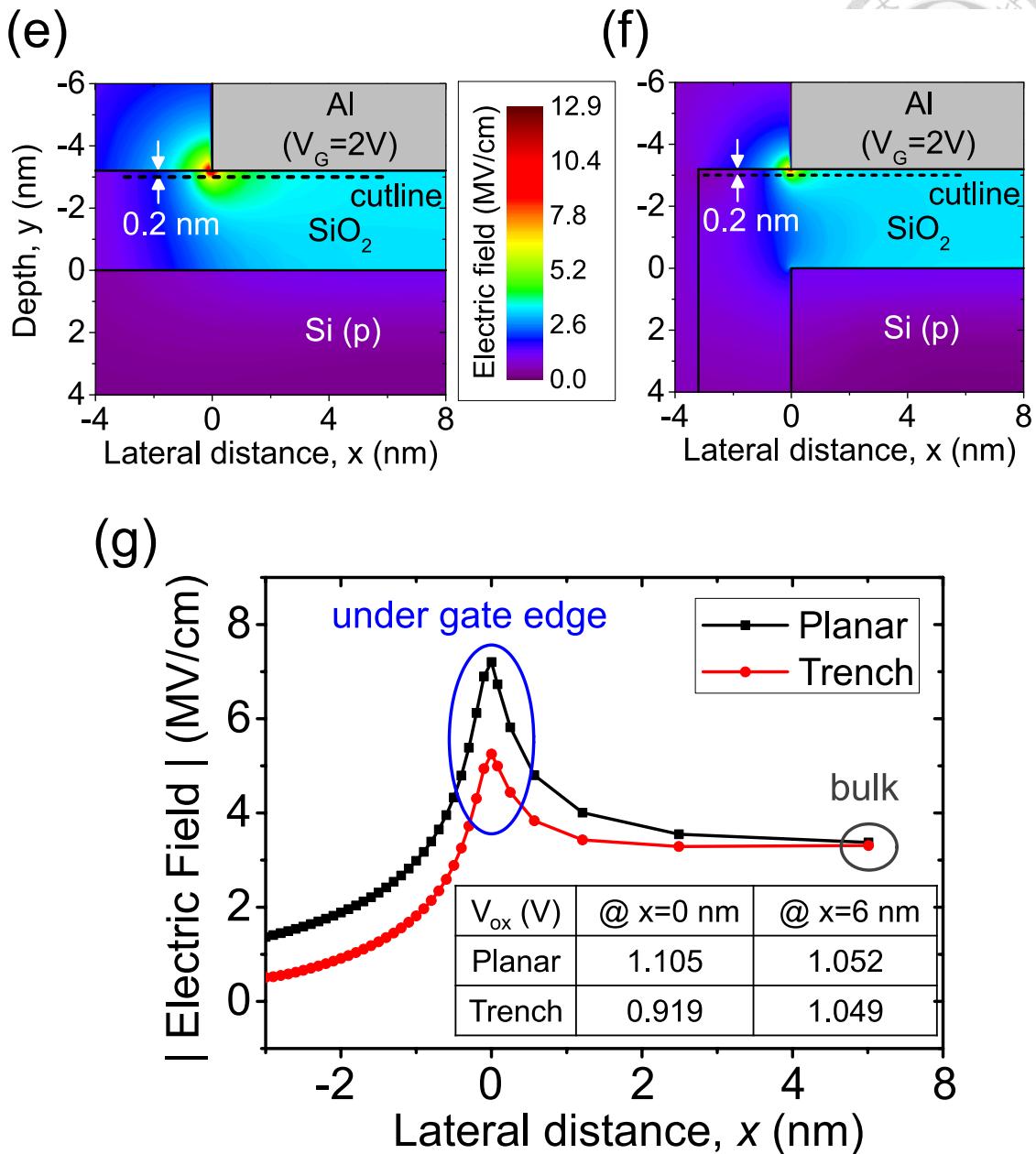
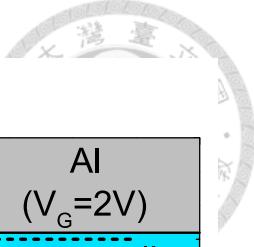


Fig. 2-6. (a) The structure parameters of planar MIS TD and (b) trench MIS TD used in Silvaco TCAD simulation. The doping concentration of Si(p) is $1 \times 10^{16} \text{ cm}^{-3}$. The simulated depletion region of (c) the planar and (d) trench MIS TD. The simulated total electric field in (e) planar MIS TD and (f) trench MIS TD, confirming the smaller fringing oxide field in trench devices. (g) The total electric field in SiO_2 along the cutlines in (e), (f). The cutlines are located at 0.2 nm downward from the bottom of the Al gate. Inset: the simulated V_{ox} values.

Chapter 3

Transient Current Behavior of Trench MIS TDs



3-1. Introduction

3-2. Results and Discussion

3-2-1. I-V Characteristics with Different Sweeping Rates

3-2-2. Memory Retention and Endurance Properties

3-2-3. Thermal Equilibrium Model of Transient Current

3-2-4. Verification of Thermal Equilibrium Model

3-2-4-1. Experimental Results

3-2-4-2. Transient TCAD Simulation

3-3. Summary



3-1. Introduction

In **Chapter 2**, the discussion is mainly focused on the steady-state current behavior (namely, the lower reverse bias current) of trench MIS TDs. However, besides the difference in steady-state current behavior compared with planar devices, trench devices also demonstrate special transient current characteristics, i.e. the enhanced transient displacement current. Since transient current behavior represents the potential use of a electronic device as memory, understanding the origin of the stronger transient current in trench MIS TDs is essential. Therefore, in **Chapter 3**, further investigation about the transient current behavior is conducted.

3-2. Results and Discussion

3-2-1. I–V Characteristics with Different Sweeping Rates

In **Fig. 2-3**, the enhanced transient current behavior at low gate voltage region can be observed. In order to examine this transient current characteristic, I–V curves with different voltage sweeping rates were measured, as shown in **Fig. 3-1**. If people take a closer look at the low voltage region of the I–V curves, the zero current voltages (ZCVs), where the current transition from negative to positive values or in reverse order happens, of planar devices under all sweeping rates and voltage sweeping directions conditions are all close to $V_G = 0$ V. However, the ZCVs of trench devices is -0.25 V in forward



sweeping direction and +0.21 V in backward direction when the sweeping rate (dV/dt) is 38 mV/s. The reason that contributes to these non-zero ZCVs is the enhanced displacement current in trench MIS TDs.

To illustrate this concept, the composition of total gate current in MIS TDs has to be introduced. The total gate current of MIS TDs consists of (1) conduction current (I_{cond}) and (2) displacement current (I_{disp}) components, which can be written into the following equations:

$$I_G = I_{cond} + I_{disp} \quad (3-1)$$

$$I_{disp} \propto \frac{dV_G}{dt} \quad (3-2)$$

When $V_G = 0$ V, conduction current (I_{cond}) is close to 0 A, yet the value of displacement current (I_{disp}) depends on the voltage sweeping rate (dV_G/dt). Consequently, if the displacement current of MIS TDs is small enough, the ZCV would still be close to 0 V, like the case of planar MIS TD in **Fig. 3-1**. Nonetheless, for trench MIS TD, the existence of larger displacement current results in the splitting of ZCVs from 0 V. To be more specific, at forward sweeping direction (**solid** curve in **Fig. 3-1**), because of the larger portion of positive displacement current with respect to conduction current, the gate current (I_G) would change from negative to positive value earlier before V_G reach 0 V, causing the ZCV of -0.25 V in trench MIS TDs. Similarly, at backward sweeping



direction (**dash** curve in **Fig. 3-1**), the larger portion of negative displacement current with respect to conduction current leads to the earlier change of the gate current from positive to negative value and results in the ZCV of +0.21 V. While the voltage sweeping rate increases, the even larger displacement current would give rise to the shifting of ZCVs to bigger magnitude, such as -0.25 V to -0.3 V and +0.21 V to +0.5 V [see **Fig. 3-1**].

The above observations in **Fig. 3-1** authenticates this transient current behavior comes from the displacement current component (I_{disp}) for the transient current (e.g. $I_G @ 0 \text{ V}$) is proportional to dV_G / dt .

3-2-2. Memory Retention and Endurance Properties

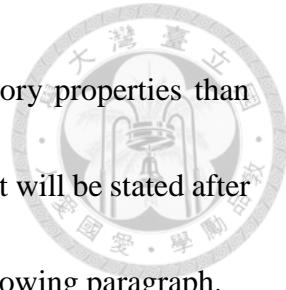
Until this part, the enhanced transient current behavior of trench devices results from the larger displacement current has been proved. Nevertheless, the origin of this stronger transient displacement current in trench MIS TDs is still unclear. Therefore, besides changing the sweeping rates of I-V curves, write-read memory measurements were also adopted to perform deeper investigation of the transient behavior. The steps and the setting of the memory measurements are shown in **Fig. 3-2**. The write “-1” and “0” voltage conditions are +2 V for 1 ms and 0 V for 1 ms, respectively. Note that 0 V was chosen to be the read voltage condition to minimize the steady-state conduction current and the power consumption in the read operation.



In **Fig. 3-3(a)**, after write “–1” ($V_G = +2$ V for 1 ms) pulse was applied to the gate of MIS TDs, both planar and trench devices read negative transient displacement currents (see read “–1” signal). However, the trench MIS TD exhibits apparently larger negative transient current (around –70 pA) than planar MIS TD (around –5 pA) at time = 0^+ s, which is consistent to the I_G-V_G curves in the backward voltage sweeping direction (dash lines) in **Fig. 3-1**. As the time increases, this negative transient current gradually disappears and the read current goes back to its steady-state value, i.e. 0 A, after time \approx 10 s (not shown in **Fig. 3-3(a)**). On the other hand, in write “0” ($V_G = 0$ V for 1 ms) and then read “0” operations, both devices read steady-state currents ≈ 0 A rather than time-dependent transient current. The memory current window (CW), which is defined as (3-3), of the devices can be extracted from **Fig. 3-3(a)**. As shown in **Fig. 3-3(b)**, at time = 0^+ s, the larger CW of the trench device also indicates the enhanced transient behavior compared to the planar one.

$$CW = I_{G, \text{read } "0"} - I_{G, \text{read } "-1"} \quad (3-3)$$

Fig. 3-4(a) shows the memory endurance characteristics of both devices. Correspondent with the memory retention measurement in **Fig. 3-3**, the magnitude of the negative transient current (read “–1” state) of trench device is also larger than it of planar device. Although a decay of CW in the trench device is observed in **Fig. 3-4(b)** before 600 cycles, it still maintains a 25 times larger CW than the planar device after the CW



becomes stable, which indicates trench MIS TDs have better memory properties than planar MIS TDs. As for the possible reason for the CW degradation, it will be stated after the origin of the negative transient current being explained in the following paragraph.

3-2-3. Thermal Equilibrium Model of Transient Current

In **Fig. 3-1**, **Fig. 3-3**, and **Fig. 3-4**, all trench devices have shown enhanced transient current behavior, e.g. the stronger negative transient current, which is related to the displacement current. The cause of this intriguing transient current behavior can be explained by the proposed “Thermal Equilibrium Model” in the following.

Fig. 3-5 and **Fig. 3-6** exhibit the concept of “Thermal Equilibrium Model” using the write “–1” ($V_G = +2$ V for 1 ms) and read “–1” ($V_G = 0$ V) operations as examples. To begin with, at write “–1”, when +2 V is applied to the gate, many minority carriers (Q_{inv}), i.e. electrons, pile up near the interface of $\text{SiO}_2 / \text{Si(p)}$ [see **Fig. 3-5(a-b)** and **Fig. 3-6(a-b)**]. Then, the gate voltage is quickly switched to 0 V to read the “–1” state transient current. Because the switching of V_G from +2 V to 0 V is too quick, there is no enough time for the electrons appealed by $V_G = +2$ V to be recombined or disappear. As a result, these electrons become excess carriers (Q_{excess}) at $V_G = 0$ V, causing the non-equilibrium state of the MIS TDs at the beginning of read “–1”. The total amount of Q_{excess} at “–1” state can be written as

$$Q_{excess} ("-1" \text{ state}) = Q_{inv}(@ + 2 \text{ V}) - Q_{inv}(@ 0 \text{ V}) \quad (3-4)$$

where Q_{inv} is the total inversion charges under steady-state (equilibrium) condition, yet

Q_{excess} is the total excess carrier charges under non-equilibrium condition. As a result, for

the MIS TDs to return to equilibrium state, Q_{excess} need to be recombined or repelled,

which brings about the negative transient current (read “-1”) as observed. The total

transient current is composed of three components [see the current flow arrows in **Fig. 3-5(c-d)** and **Fig. 3-6(c-d)**]:

- (1) Q_{excess} tunnel through gate oxide, which contributes to positive electron tunneling current, $I_{e(T)}$.
- (2) Holes from gate electrode tunnel through gate oxide and then recombine with Q_{excess} via traps, which contributes to positive hole tunneling current, $I_{h(T)}$.
- (3) Hole from back gate electrode inject into the Si(p) substrate and then recombine with Q_{excess} through traps, which contributes to negative hole displacement current, $I_{h(D)}$.

Since Q_{excess} would be reduced or recombined eventually for the devices to return to

thermal equilibrium, the Q_{excess} and the read “-1” transient current can be written as

$$|Q_{excess}| = \int |I_{e(T)}(t)| + |I_{h(T)}(t)| + |I_{h(D)}(t)| dt \quad (3-5)$$

and

$$\begin{aligned}
I_{G, \text{read} "-1"(t)} &= I_{e(T)}(t) + I_{h(T)}(t) + I_{h(D)}(t) \\
&= |I_{e(T)}(t)| + |I_{h(T)}(t)| - |I_{h(D)}(t)|
\end{aligned}$$



(3-6)

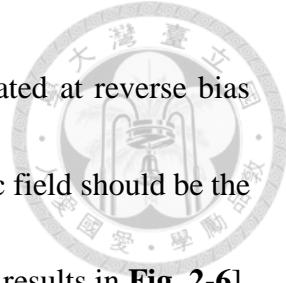
For planar MIS TDs, a small negative read “-1” current at $t = 0^+$ s can be observed

in **Fig. 3-3(a)**. By (3-6), one can infer that the $|I_{h(D)}|$ current in planar devices is a little bigger than the $|I_{h(T)}| + |I_{e(T)}|$ current at $t = 0^+$ s, as shown in **Fig. 3-5(c)** and **Fig. 3-6(c)**.

On the contrary, for trench MIS TDs, the enhanced negative read “-1” current indicates the $|I_{h(D)}|$ component is much bigger than the $|I_{h(T)}| + |I_{e(T)}|$ component at $t = 0^+$ s. This is because the trench devices have equivalently smaller V_{ox} .

According to the discussion in **Section 2-3-1**, the reduced average V_{ox} in trench MIS TDs would lead to smaller steady-state tunneling current. It is expected that the magnitude of the transient tunneling current components, i.e. $|I_{h(T)}|$ and $|I_{e(T)}|$, are also proportional to the V_{ox} . Thus, $|I_{h(T)}| + |I_{e(T)}|$ of the trench devices would become smaller considering the lower equivalent V_{ox} in trench MIS TDs. Based on the above statement, if both planar and trench devices have the same $|I_{h(D)}|$, by (3-6), larger negative transient current in read “-1” of trench MIS TDs at $t = 0^+$ s can be deduced [illustrated in **Fig. 3-5(d)** and **Fig. 3-6(d)**]. The above explanation is consistent with the experimental results in **Fig. 3-3(a)** and **Fig. 3-4(a)**.

It is worth mentioning that only the current under the gate edge is discussed to explain the difference of transient current behavior between planar and trench devices. It



is not only because the overall current of MIS TDs is edge-dominated at reverse bias region [see **Section 1-2-3**] but also because bulk V_{ox} and bulk electric field should be the same in two kinds of MIS TDs [see the bulk electric field simulation results in **Fig. 2-6**].

In other words, at the bulk region of MIS TDs, both planar and trench devices have the same transient current [also illustrated in **Fig. 3-5** by the carriers flow lines]. Starting from this point of view, the difference of edge transient current between planar and trench devices must account for the large differentiation of the overall transient current characteristics between planar and trench MIS TDs.

Now comes to the write “0” and read “0” operations in **Fig. 3-3** and **Fig. 3-4**. For read “0” state, there is no excess electron ($Q_{excess} = 0$, by (3-7)) because the voltage conditions of write “0” and read “0” are all 0 V. As a result, both planar and trench MIS TDs show zero transient currents in read “0” state [see **Fig. 3-3** and **Fig. 3-4**].

$$Q_{excess}("0" \text{ state}) = Q_{inv}(@ 0 \text{ V}) - Q_{inv}(@ 0 \text{ V}) = 0 \quad (3-7)$$

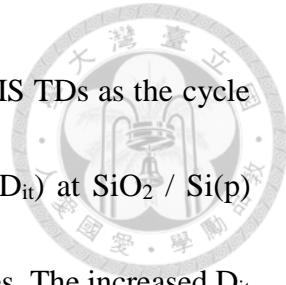
The read “0” current can be written as

$$I_{G, \text{read } "0"}(t) \approx 0 \quad (3-8)$$

Substituting (3-8) into (3-3), the following equation can be inferred.

$$CW = -I_{G, \text{read } "-1"} \quad (3-9)$$

which indicates the CW is proportional to the magnitude of the read “-1” current.



Back to **Fig. 3-4**, the decay of the transient current of trench MIS TDs as the cycle increases might result from the increase of interface trap density (D_{it}) at $\text{SiO}_2 / \text{Si(p)}$ interface and at trench sidewall as the number of operation cycles rises. The increased D_{it} would recombine some of the Q_{excess} , leading to the decrease of transient current and CW.

3-2-4. Verification of Thermal Equilibrium Model

3-2-4-1. Experimental Results

In the previous section, “Thermal Equilibrium Model” that can be used to explain the transient current behavior of MIS TDs and the enhanced transient current in trench MIS TDs was proposed. To sum up, the transient current is related to two factors according to the model: (1) the amount of Q_{excess} and (2) the relative magnitude between $|I_{h(T)}| + |I_{e(T)}|$ and $|I_{h(D)}|$ current components. In the following, whether the transient current of MIS TDs is indeed influenced by these two factors is verified by some experimental results.

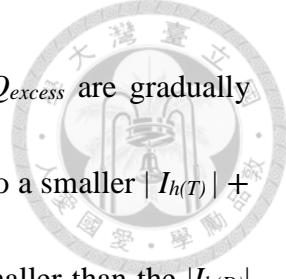
From **Fig. 3-6** and (3-5), it can be extrapolated that the quantity of the Q_{excess} is proportional to the magnitude of the transient current. Thus, by applying a smaller write “ -1 ” voltage, which reduces the number of Q_{inv} and Q_{excess} , the read “ -1 ” current of both devices should decrease accordingly. Based on this prediction, the impact of smaller write “ -1 ” voltage on the endurance property is investigated in **Fig. 3-8**. In the measurement, the write “ -1 ” voltage was adjusted from $+2$ V to $+1.5$ V and $+1$ V [see **Fig. 3-7**].



Moreover, when the write “–1” voltage reduces, the negative value of the transient current from both planar [**Fig. 3-8(a)**] and trench MIS TDs [**Fig. 3-8(b)**] decreases as expected. This observation substantiates that the transient current is related to the amount of Q_{excess} .

In “Thermal Equilibrium Model”, apart from Q_{excess} , the second factor that affects the negative transient current is the relative magnitude between $|I_{h(T)}| + |I_{e(T)}|$ (leading to positive transient current) and $|I_{h(D)}|$ (leading to negative transient current) current components. However, in **Fig. 3-3** and **Fig. 3-4**, only the existence of $|I_{h(D)}|$ components can be confirmed by the apparent negative read “–1” current. Hence, retention properties of more devices were measured to find whether there is MIS TD showing a positive read “–1” current so one can vindicate the transient current is determined by the competition between $|I_{h(T)}| + |I_{e(T)}|$ and $|I_{h(D)}|$ components.

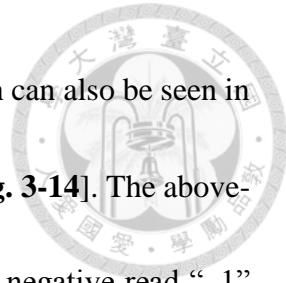
Eventually, totally 24 planar MIS TDs and 33 trench MIS TDs with various EOTs were measured. Although all read “–1” currents of trench devices are negative value, 9 out of 24 planar MIS TDs show positive read “–1” currents at the beginning of retention measurements, which can be used to corroborate the $|I_{h(T)}| + |I_{e(T)}|$ current. The retention characteristic of one of the nine planar devices is shown in **Fig. 3-9** to represent the observed positive read “–1” current. In **Fig. 3-9**, the retention curve can be split into two regions according to the sign of the read “–1” current. At region 1, where $I_G @ 0 \text{ V} > 0$, the positive transient current is caused by the larger $|I_{h(T)}| + |I_{e(T)}|$ than the $|I_{h(D)}|$ current



component [illustrated in **Fig. 3-10(a)**]. As the time goes, while Q_{excess} are gradually recombined, the V_{ox} also decreases ($\because V_{ox} \propto -Q_{inv} / C_{ox}$) and leads to a smaller $|I_{h(T)}| + |I_{e(T)}|$ current. Consequently, when the $|I_{h(T)}| + |I_{e(T)}|$ becomes smaller than the $|I_{h(D)}|$ current component, $I_G @ 0$ V would turn to negative value [illustrated in **Fig. 3-10(b)**], as observed in the region 2 of **Fig. 3-9**. Notice that the positive read “-1” current is suspected to appear in planar MIS TDs with more Q_{inv} , which further causes larger V_{ox} and bigger positive tunneling current. This explain why only some of the planar MIS TDs have positive read “-1” signal for different planar MIS TDs have slightly different number of Q_{inv} . In short, the observation of positive read “-1” current can support the existence of $|I_{h(T)}| + |I_{e(T)}|$ current and verify “Thermal Equilibrium Model”.

3-2-4-2. Transient TCAD Simulation

Besides experimental measurements, transient TCAD simulation is also adopted to substantiate the proposed model. In **Fig. 3-11**, structure parameters of trench MIS TDs used in the transient TCAD are shown. **Fig. 3-12** demonstrates the simulation steps of the transient TCAD solution. To begin with, steady-state TCAD of trench MIS TDs at $V_G = 0$ V and $+2$ V were solved first. After that, based on the steady-state solution at $V_G = +2$ V, transient simulation switching from $V_G = +2$ V to 0 V can be conducted. In the simulated retention current of **Fig. 3-13**, negative read “-1” current, which is qualitatively similar to the experimental data (like **Fig. 3-3**), of trench devices can be observed.



Moreover, this negative current would reduce as the time goes, which can also be seen in the contour plot of total y-component current density ($J_{total, y}$) [see **Fig. 3-14**]. The above-mentioned simulation results have corroborated the existence of the negative read “-1” current observed in the memory properties measurement before.

Another essential thing that needs to be verified is the cause of the transient current, According to the proposed “Thermal Equilibrium Model”, negative transient current results from the recombination and repelling of excess carriers (electrons). In the simulation of **Fig. 3-15(a-b)** and **Fig. 3-16(a-b)**, one can observe when V_G switches from +2 V to 0 V, inversion carriers become excess electrons that stay in the Si substrate [see **Fig. 3-15(b)**] and near the SiO_2 / Si (p) interface [see **Fig. 3-16(b)**]. As the time increases, these excess electrons are gradually repelled or recombined, which results in the decrease of electron concentration (n_e), as shown in **Fig. 3-15(b-f)** and **Fig. 3-16(b-f)**. In addition, the recombination rate, which is the highest at time = 1.35 ms [see **Fig. 3-17**], also declines with n_e as the time goes. Based on these transient simulation results, one can infer that recombination and decreasing of excess electrons do contribute to the negative transient current. Accompanied with the experimental supports in **Section 3-2-4-1**, the authentication of “Thermal Equilibrium Model” has been strengthened.



3-3. Summary

In this chapter, the transient current behaviors of MIS TDs are comprehensively studied by I-V curves with different voltage sweeping rates, retention, and endurance memory measurements. The above experimental results confirm that trench MIS TDs have stronger transient current properties than planar MIS TDs. Furthermore, the proposed “Thermal Equilibrium Model” can explain the root cause of this enhanced transient behavior of trench devices. In the end of this chapter, more experimental results and transient TCAD simulation were presented to support “Thermal Equilibrium Model”.

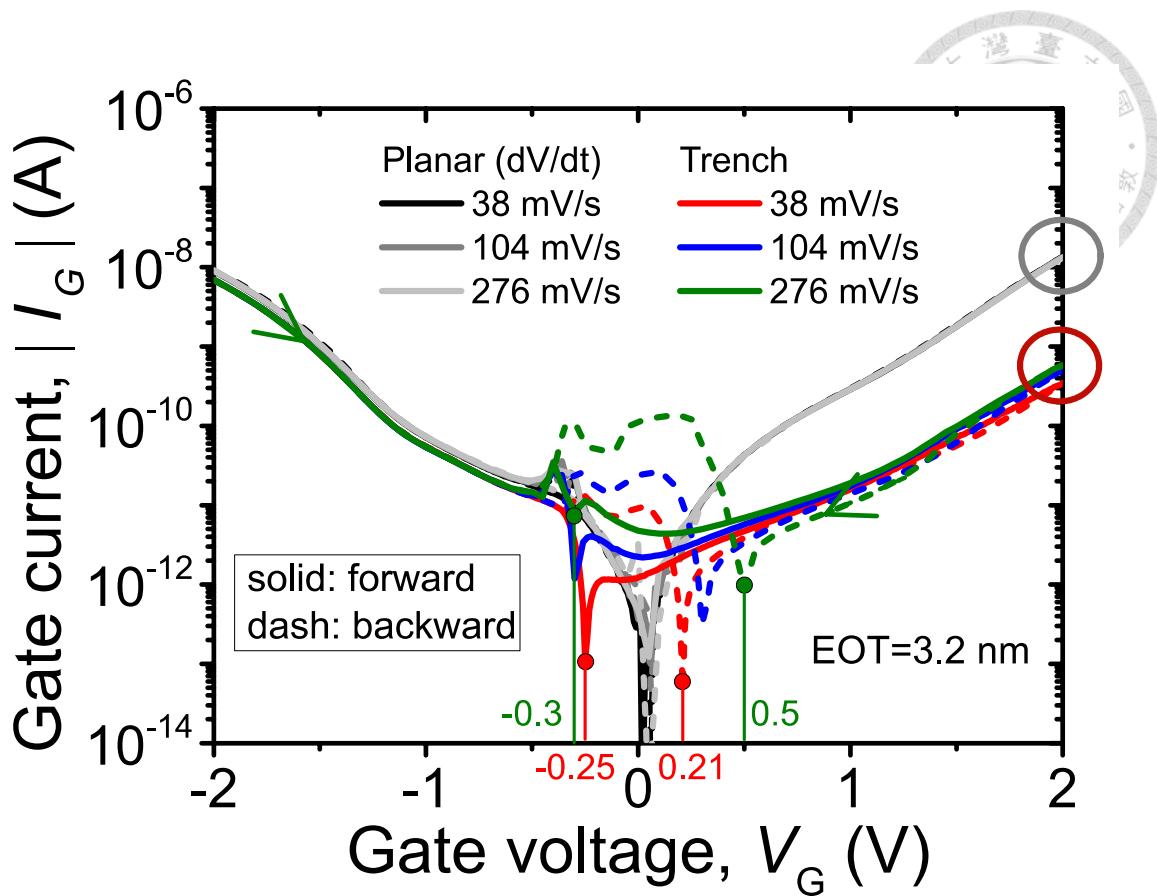


Fig. 3-1. Current–voltage characteristics of the planar and the trench MIS TDs with two voltage sweeping directions and different voltage sweeping rates (dV/dt). At $V_G > 0$ V, MIS TDs are in reverse bias region. At $V_G < 0$ V, MIS TDs are in forward bias region. Solid: voltage sweeps forward. Dash: voltage sweeps backward.

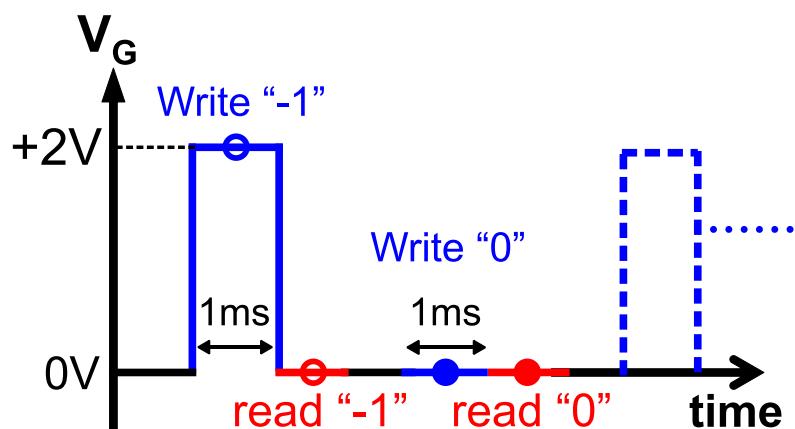
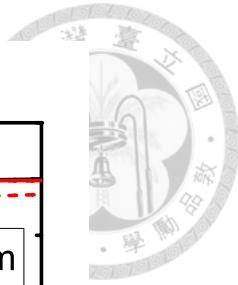
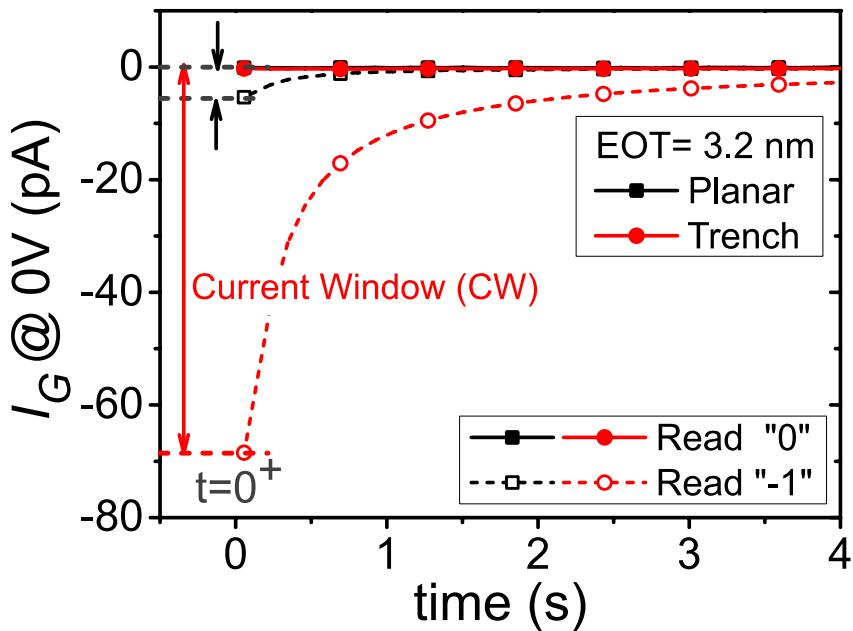


Fig. 3-2. Write and read voltage operation settings used in the memory measurement.



(a)



(b)

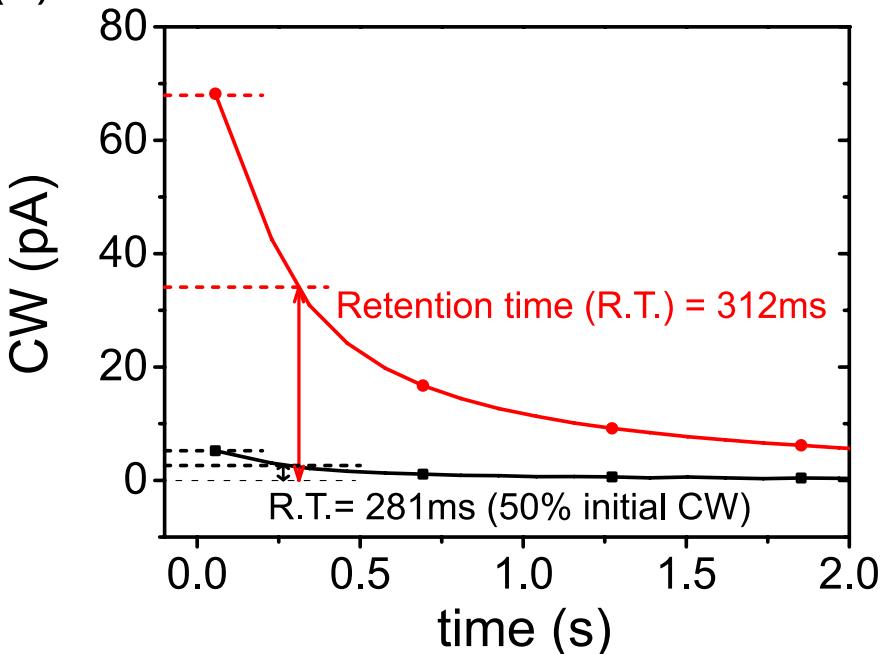


Fig. 3-3. (a) Retention characteristics of planar and trench MIS TDs. The measurement steps and settings are shown in **Fig. 3-2**. (b) The extracted current window from (a). Current window (CW) is defined as the read current difference between “0” and “-1” states. Retention time (R.T.) is defined as the amount of time it takes for CW to drop to half of its original value at time = 0^+ s.

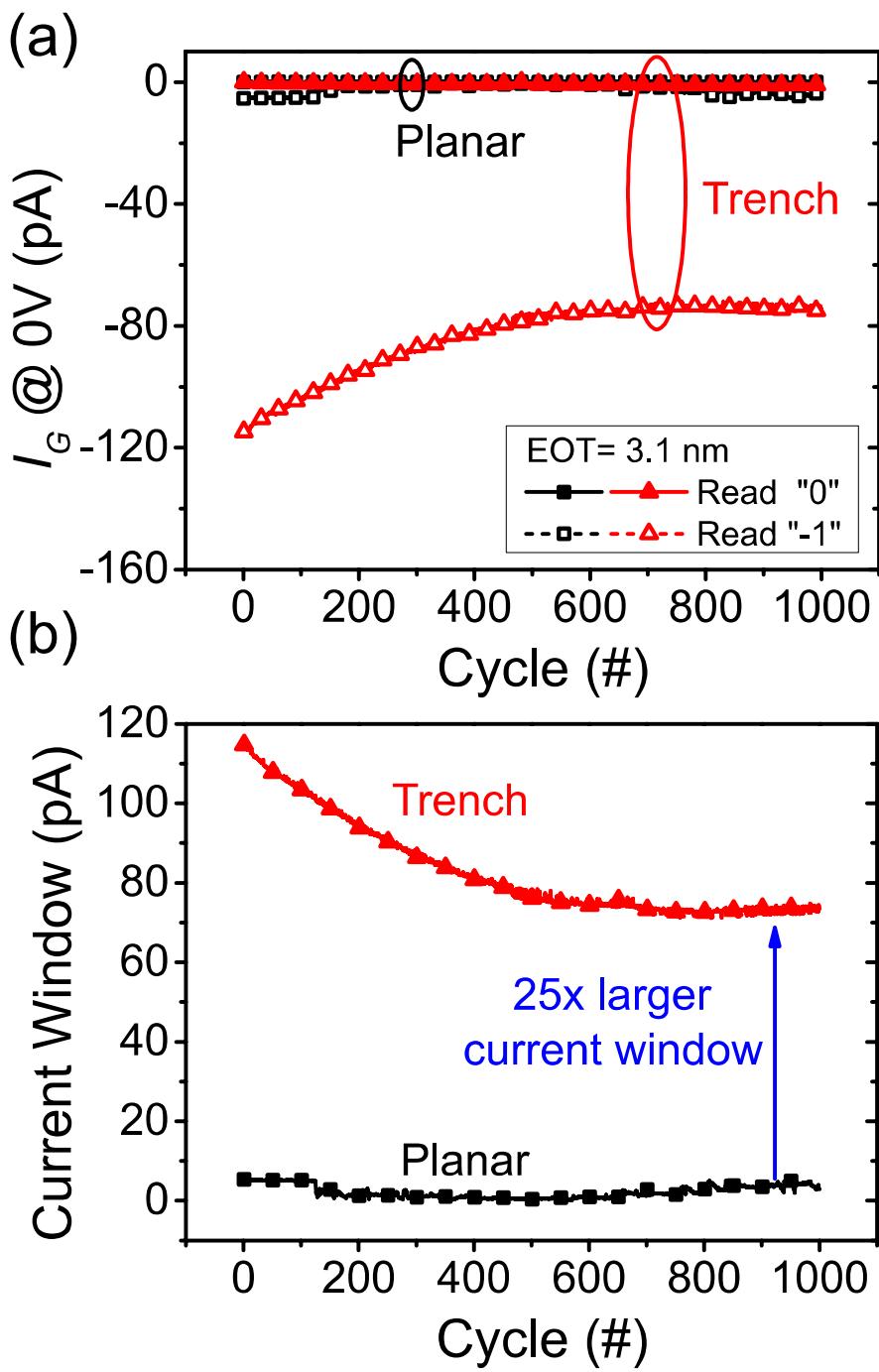
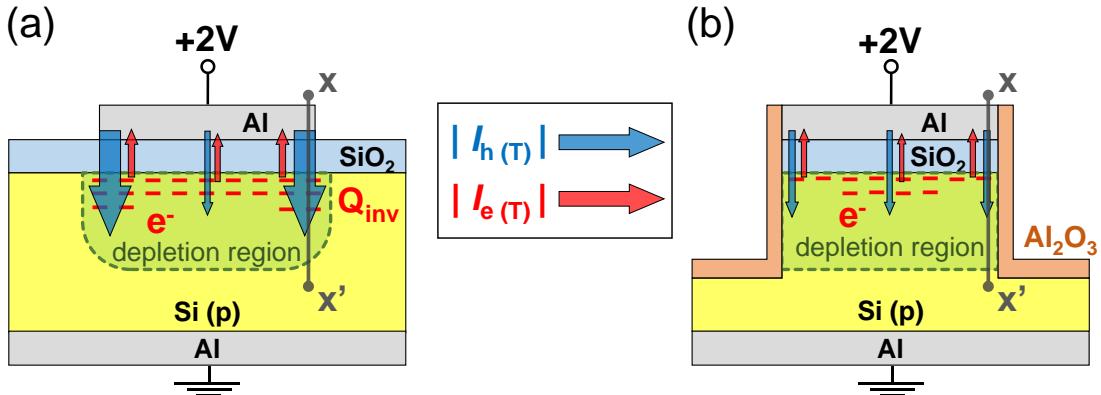
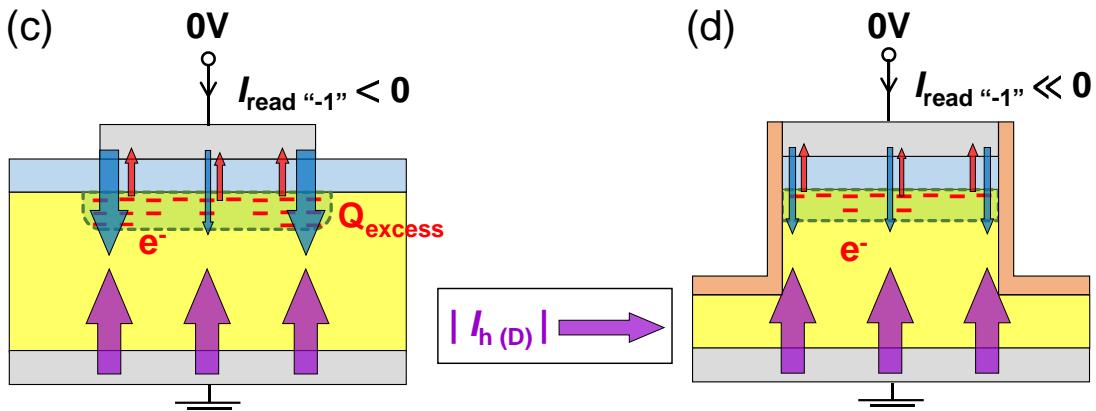


Fig. 3-4. (a) Endurance characteristics of planar and trench MIS TDs. The endurance read current data is read at time = 0^+ s in each read operation. (b) Extracted CW from the endurance measurement in (a). The write and read voltage settings are the same as **Fig. 3-2**.

1. Write “-1” (+2V, steady-state)



2. Read “-1” @ $t=0^+s$ (non-equilibrium)



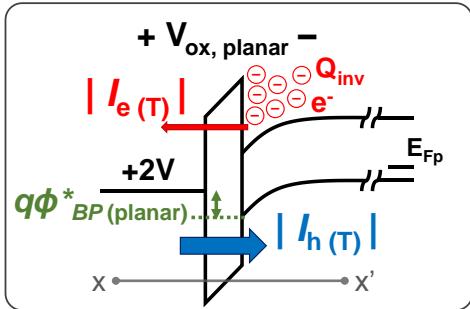
$$\begin{aligned} |I_{e(T)}| + |I_{h(T)}|_{(\text{planar})} &\gg |I_{e(T)}| + |I_{h(T)}|_{(\text{trench})} \\ |I_{h(D)}|_{(\text{planar})} &\approx |I_{h(D)}|_{(\text{trench})} \\ |I_{\text{read } -1}|_{(\text{planar})} &\ll |I_{\text{read } -1}|_{(\text{trench})} \end{aligned}$$

Fig. 3-5. Schematic MIS TDs structures that are used to explain “Thermal Equilibrium Model”. At write “-1” condition, both (a) planar and (b) trench devices accumulate inversion charges (Q_{inv}), namely electrons (represented by $-$), near the SiO_2 / Si interface. At the beginning ($t = 0^+ s$) of read “-1” condition, because the switching from write to read operation is so quick, the Q_{inv} of (c) planar and (d) trench MIS TDs have no time to be recombined or disappear and become excess inversion carriers (Q_{excess}). **Blue arrows:** the flowing direction, which results in $|I_{h(T)}|$ / current flow, of holes. **Red arrows:** the flowing direction, which results in $|I_{e(T)}|$ / current flow, of electrons. **Purple arrows:** the flowing direction, which results in $|I_{h(D)}|$ / current flow, of holes. Note that e denotes electron current, h denotes hole current, T denotes tunneling current, and D denotes displacement current.

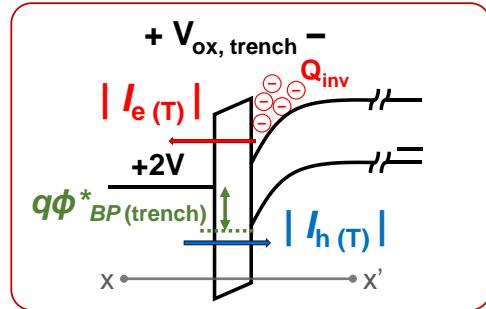


1. Write “-1” (+2V, steady-state)

(a) Planar MIS

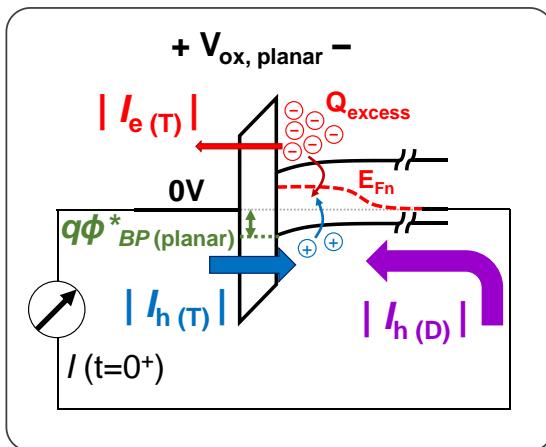


(b) Trench MIS

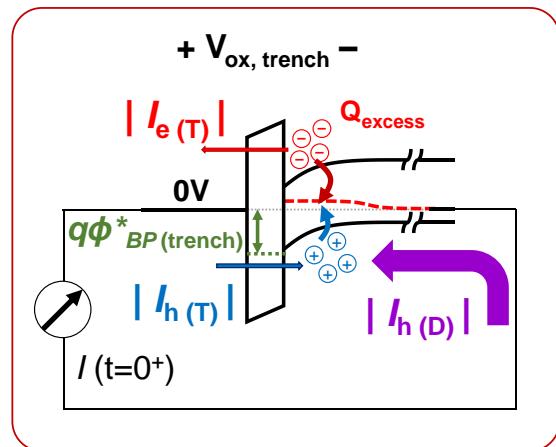


2. Read “-1” @ t=0⁺s (non-equilibrium)

(c) Planar MIS



(d) Trench MIS



$$\begin{aligned}
 & V_{ox, \text{planar}} > V_{ox, \text{trench}} \\
 & q\Phi^*_{BP(\text{planar})} < q\Phi^*_{BP(\text{trench})} \\
 & |I_{e(T)}| + |I_{h(T)}|_{(\text{planar})} \gg |I_{e(T)}| + |I_{h(T)}|_{(\text{trench})} \\
 & |I_{h(D)}|_{(\text{planar})} \approx |I_{h(D)}|_{(\text{trench})}
 \end{aligned}$$

Fig. 3-6. Schematic band diagrams that demonstrate the concept of “Thermal Equilibrium Model” along the cutline x—x’ in **Fig. 3-5**. At t = 0⁺ s of read “-1” condition, because the switching from write to read operation is so quick, the Q_{inv} of (c) planar and (d) trench MIS TDs have no time to be recombined or disappear and become excess inversion carriers (Q_{excess}).

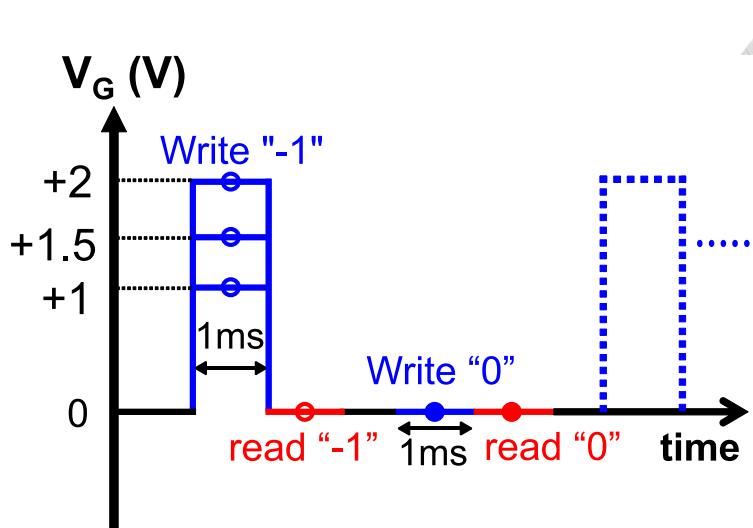


Fig. 3-7. Write and read voltage operation settings used to verify “Thermal Equilibrium Model”.

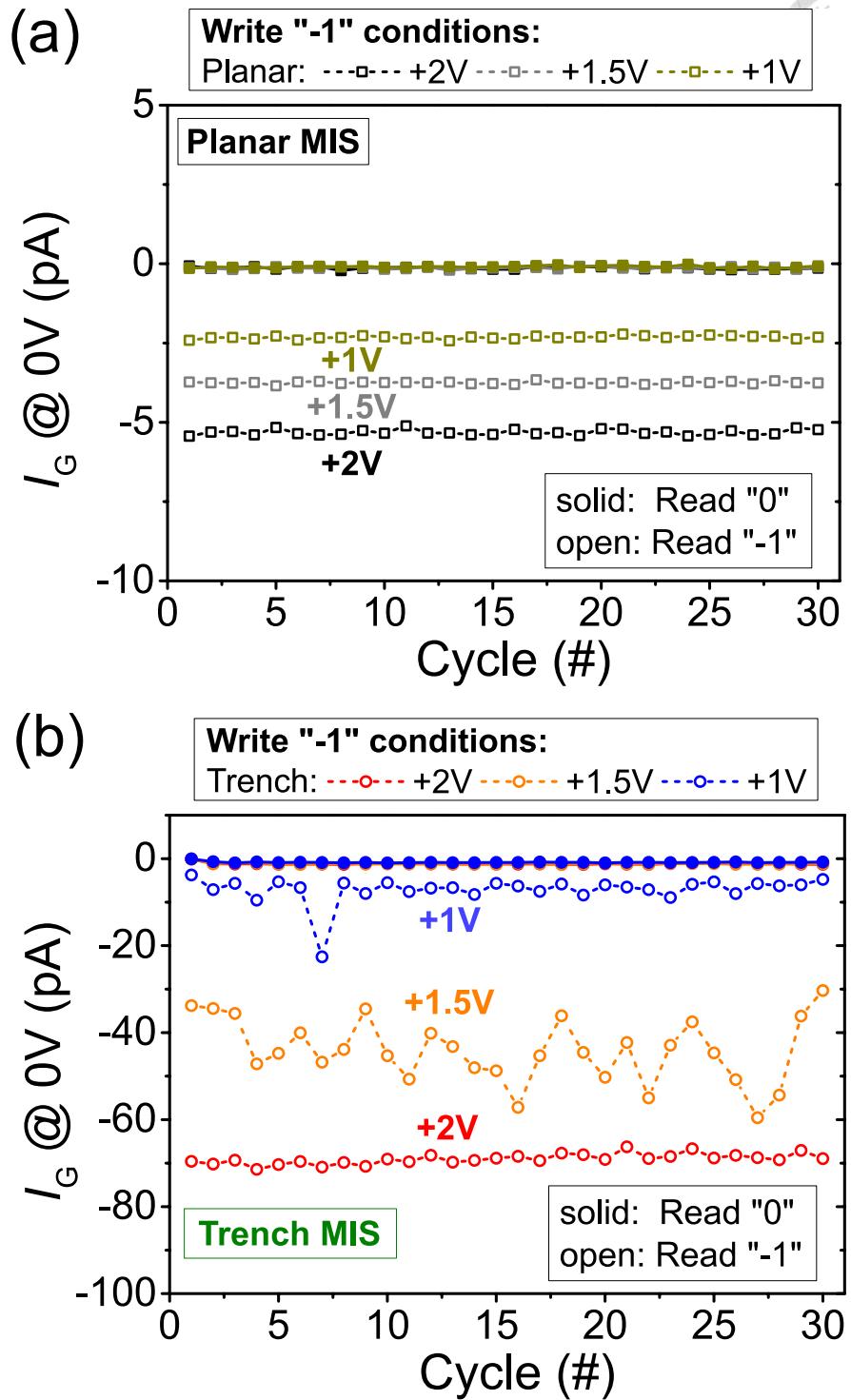


Fig. 3-8. Endurance measurement of (a) planar MIS TD and (b) trench MIS TD using the write and read voltage conditions in **Fig. 3-7**. The endurance read current data is read at time = 0^+ s in each read operation. Solid: read “0” state. Open: read “-1” state.

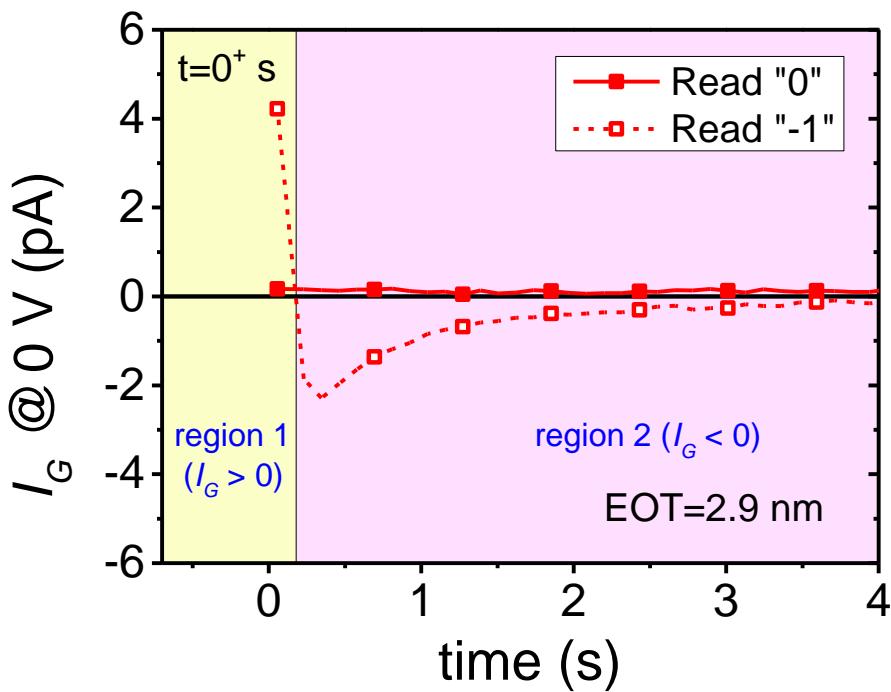
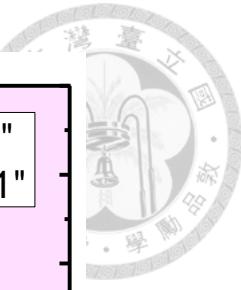


Fig. 3-9. Retention characteristics of a planar MIS TD with positive read “-1” current. The measurement steps are the same as in **Fig. 3-2**.

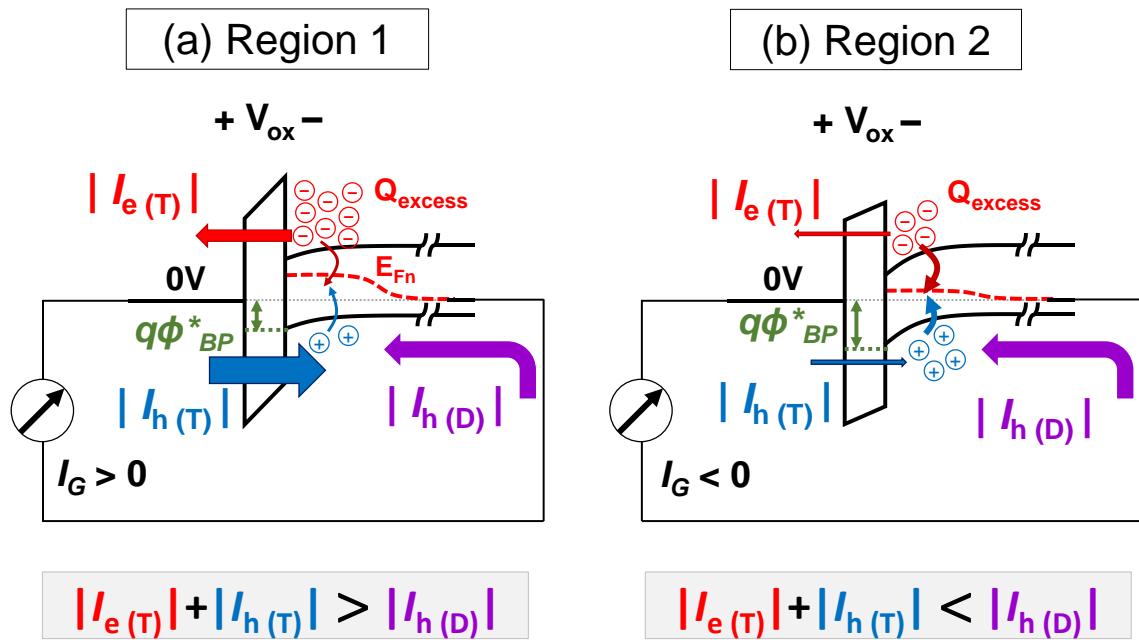


Fig. 3-10. Schematic band diagrams used to explain the positive transient current of planar MIS TDs. (a) The band diagram of planar MIS TD at region 1 of **Fig. 3-9**. (b) The band diagram of planar MIS TD at region 2 of **Fig. 3-9**.

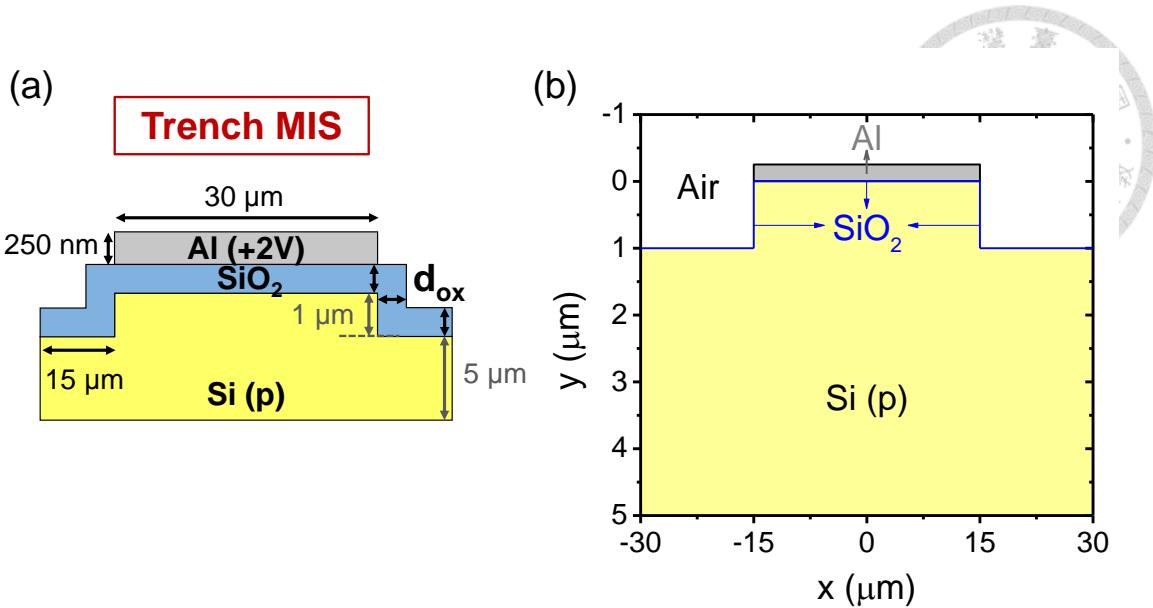


Fig. 3-11. (a) Schematic structure of trench MIS TDs used in the transient TCAD simulation. d_{ox} ranges from 2 nm to 6 nm. (b) The trench MIS TD structure of TCAD simulation. This will help readers to understand the following contour figures more easily. Note that because the oxide thickness is too thin under μm scale, the oxide layer can barely be seen in subfigure (b). **Blue lines** are used to mark the position of the oxide layer.

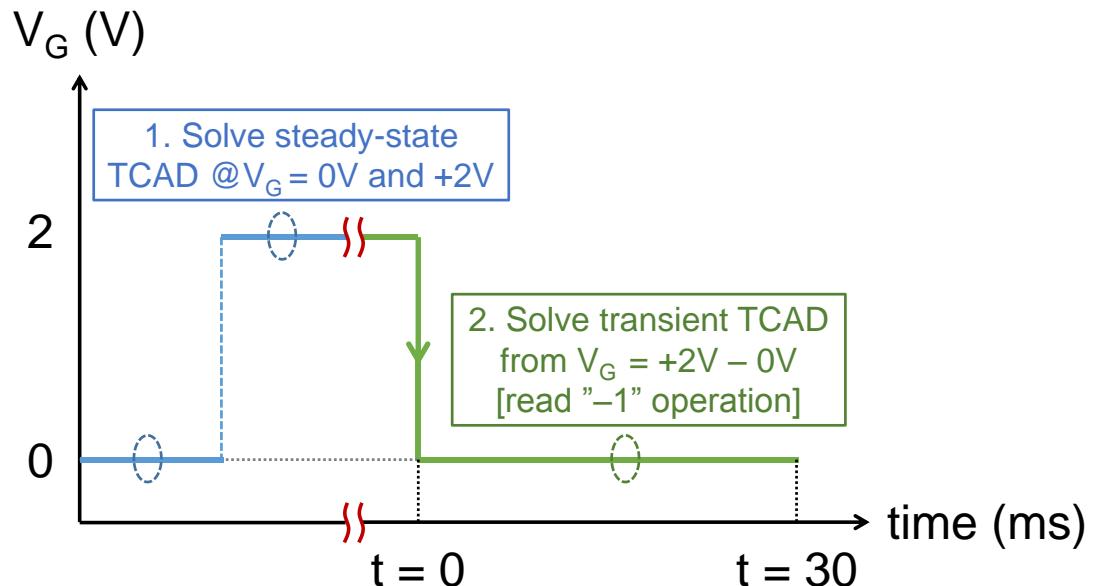


Fig. 3-12. Simulation steps of transient TCAD. At first, steady-state solutions of trench MIS TDs at $V_G = 0\text{V}$ and $+2\text{V}$ are performed. Secondly, transient solution switching from $V_G = +2\text{V}$ to 0V , i.e. write “-1” and read “-1” operations, is conducted. Please note that write “0” and read “0” operations are not simulated for the expected zero transient current.

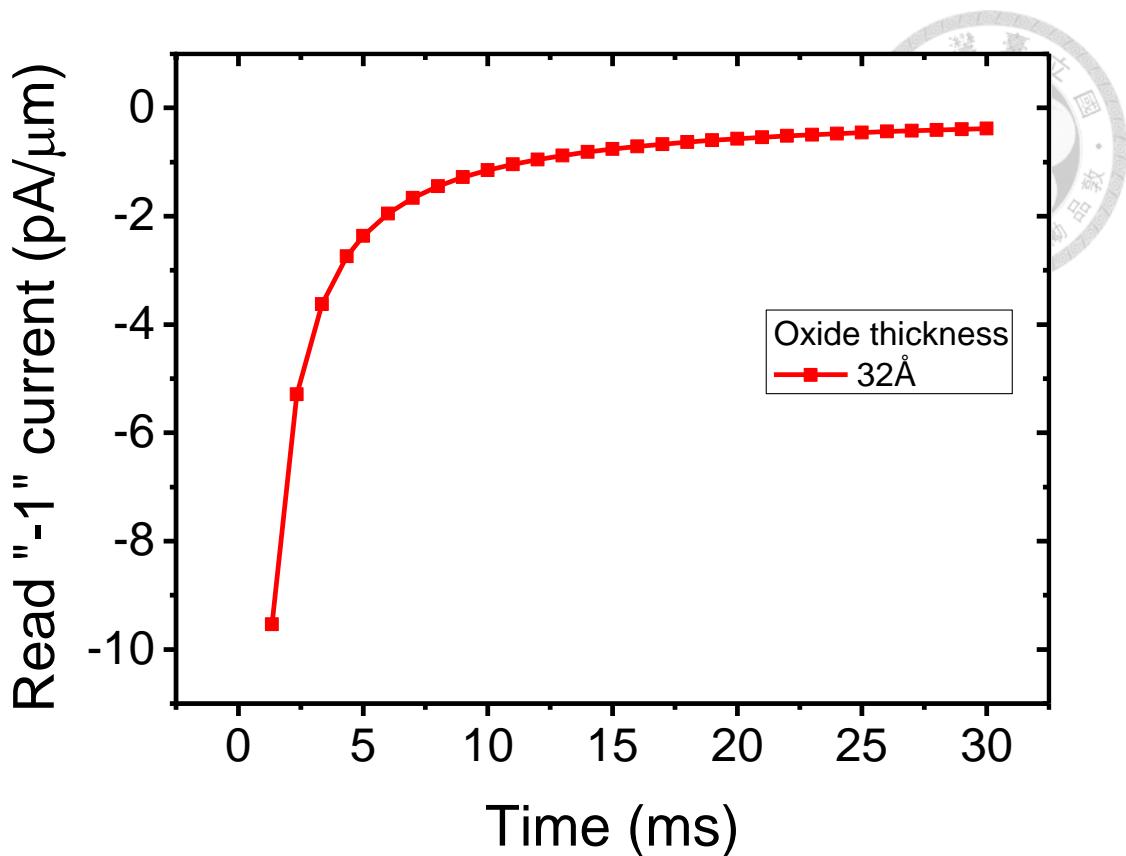


Fig. 3-13. Simulated retention result of trench MIS TD with $d_{ox} = 3.2$ nm under read “-1” operation. Negative read “-1” current that is similar to the experimental result in **Fig. 3-3(a)** can be observed.

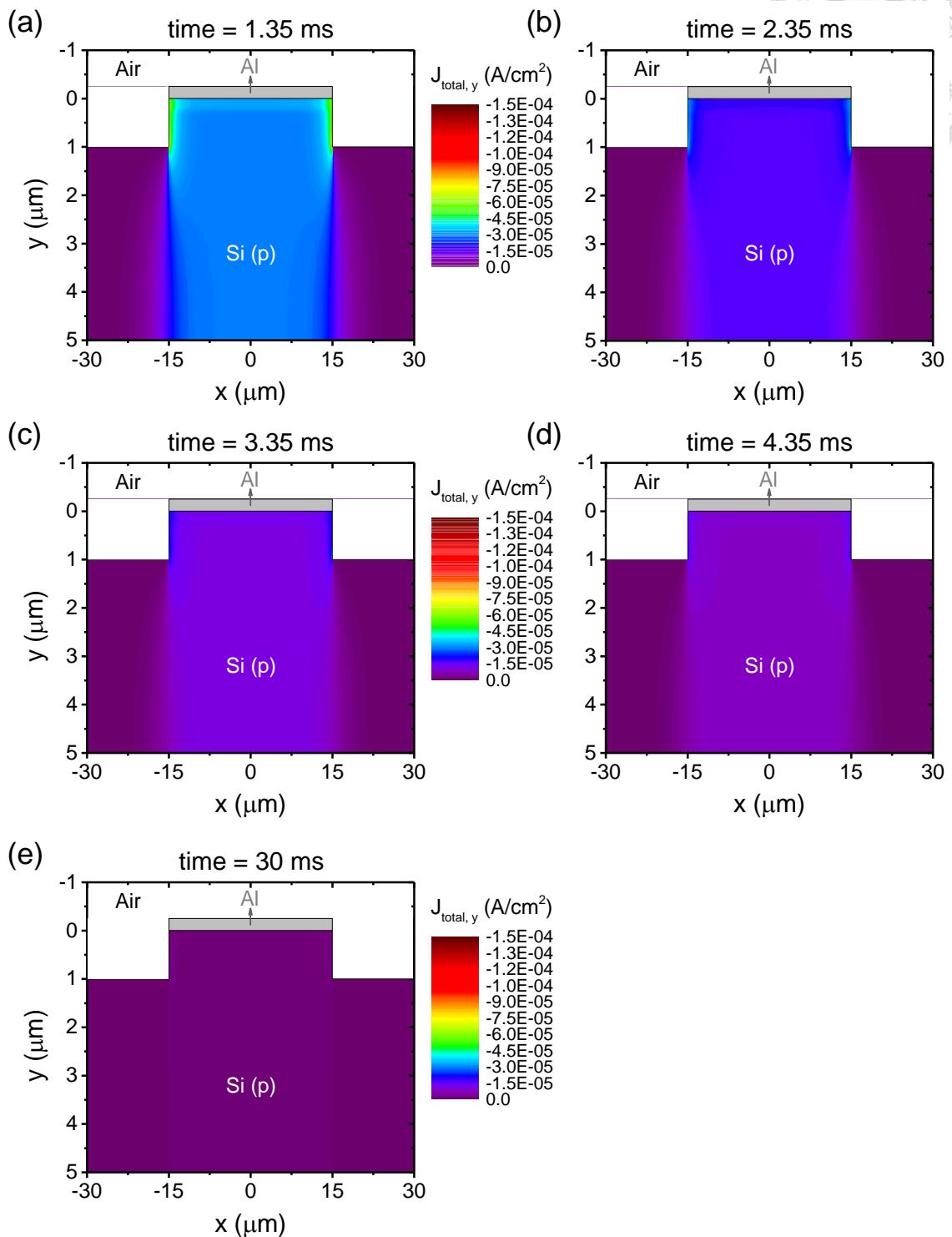
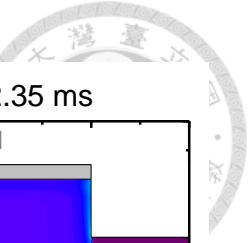


Fig. 3-14. Contour plots of total y-component current density ($J_{total,y}$) of trench MIS TD at (a) time = 1.35 ms, (b) time = 2.35 ms, (c) time = 3.35 ms, (d) time = 4.35 ms, and (e) time = 30 ms under read “-1” operation. As the time goes from 1.35 to 30 ms, the magnitude of $J_{total,y}$ reduces, which is consistent with the simulation in **Fig. 3-13**.

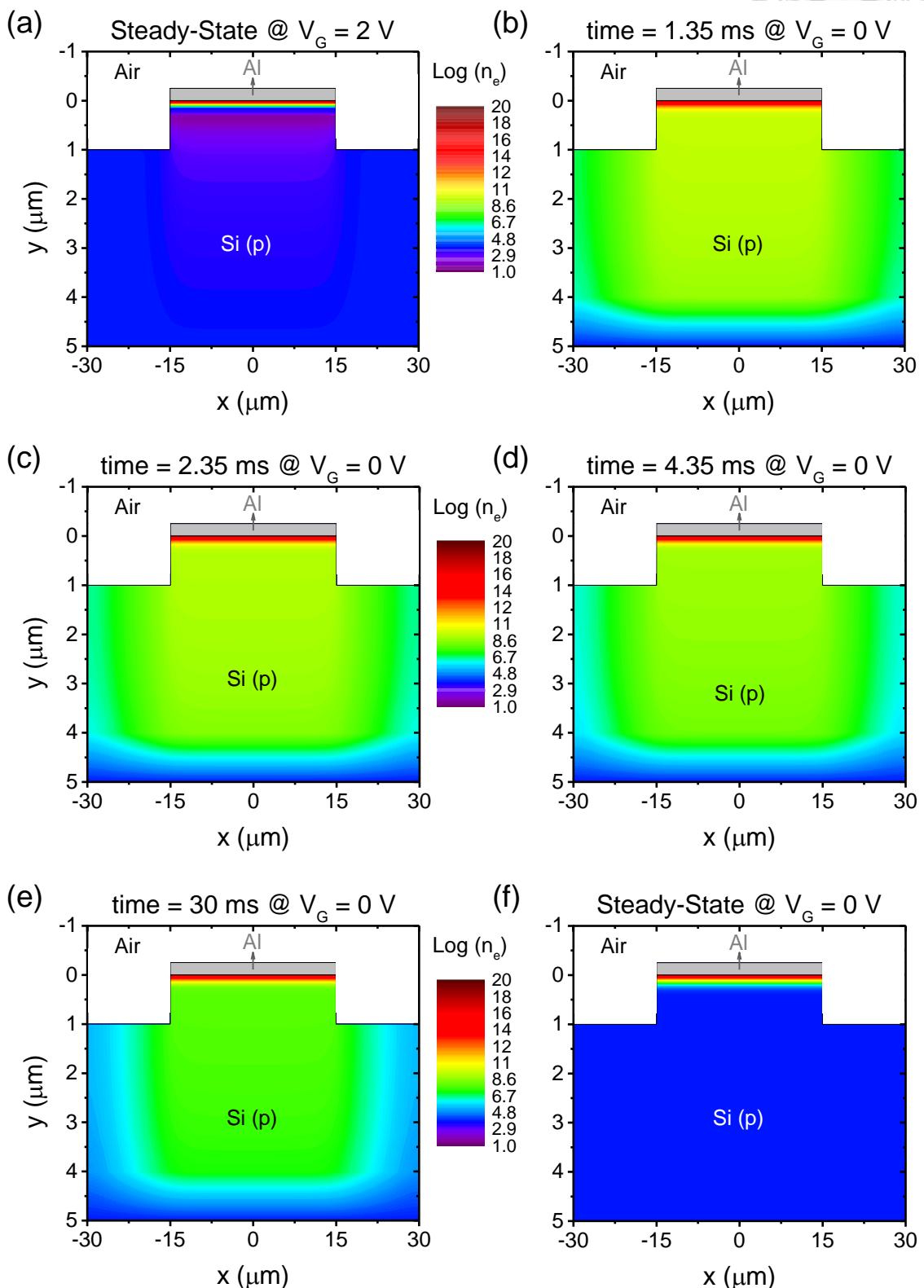
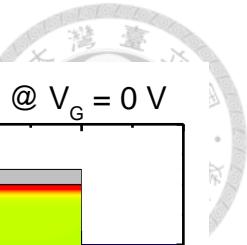


Fig. 3-15. Contour plots of electron concentration (n_e) under log scale. (a) Steady-state n_e at $V_G = +2$ V. (b–e) Transient n_e under read “-1” operation from $t = 1.35\text{--}30$ ms after V_G switches to 0 V. (f) Steady-state n_e at $V_G = 0$ V, which can be viewed as the transient solution of n_e at $t = \infty$.

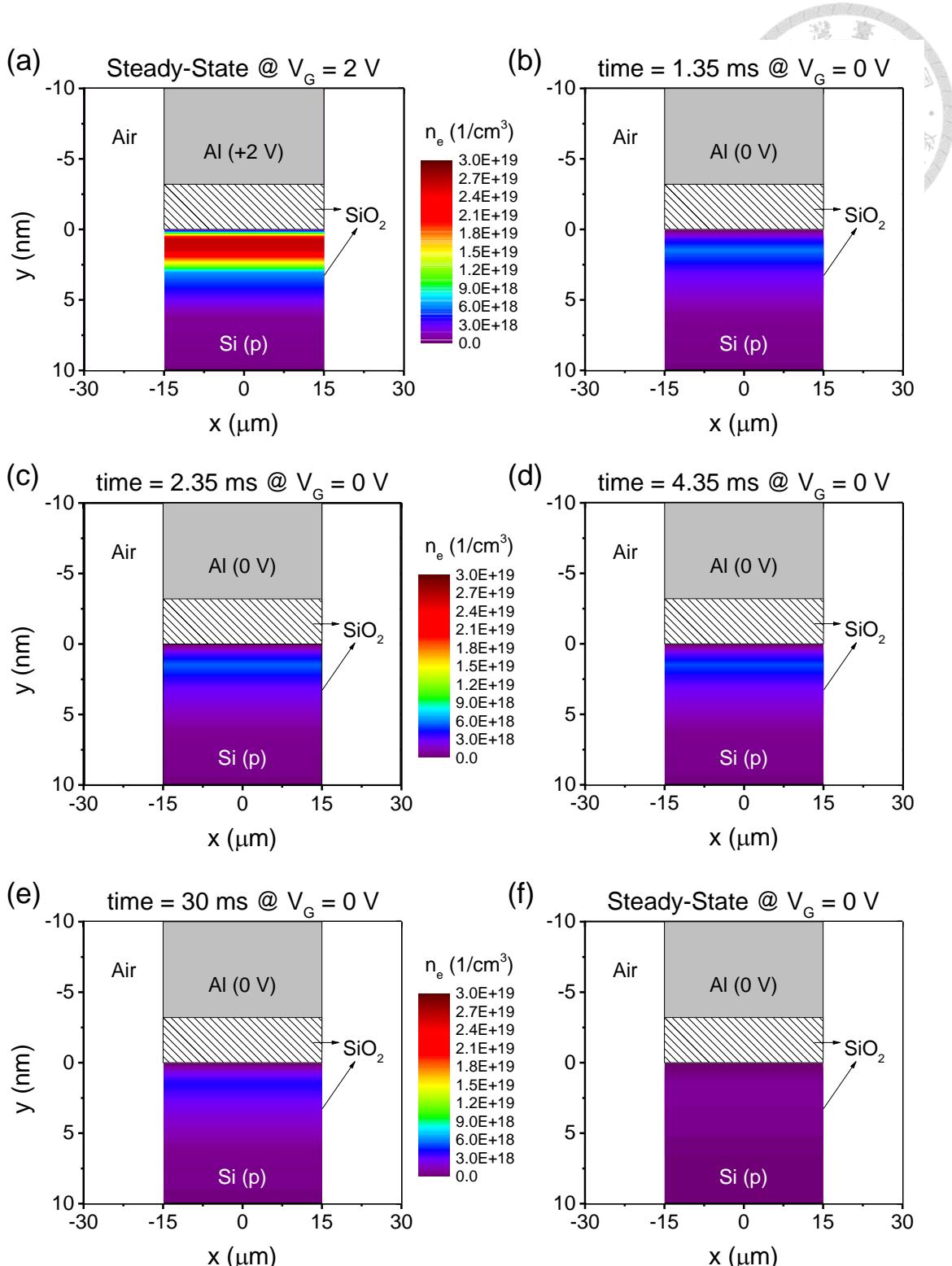


Fig. 3-16. Contour plots of electron concentration (n_e) under linear scale. Notice that compared to **Fig. 3-15**, this figure zooms in the region close to SiO_2 / $\text{Si}(p)$ interface. (a) Steady-state n_e at $V_G = +2$ V. (b–e) Transient n_e under read “ -1 ” operation from $t = 1.35$ – 30 ms after V_G switches to 0 V. (f) Steady-state n_e at $V_G = 0$ V, which can be viewed as the transient solution of n_e at $t = \infty$. Since the oxide layer (3.2 nm) at trench sidewall is too thin under μm scale (x-axis), it cannot be seen in the figures.

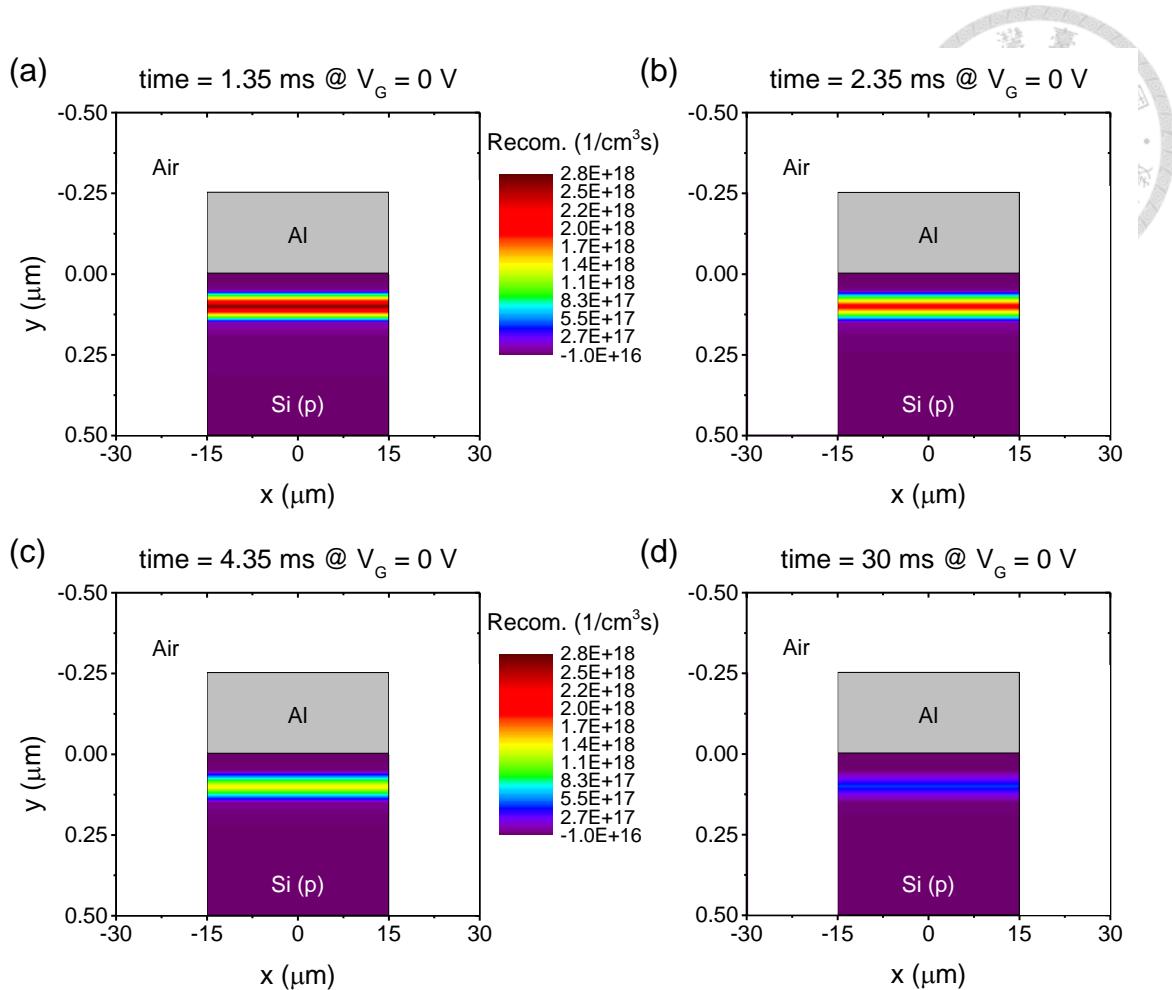


Fig. 3-17. Contour plots of recombination rate (Recom.) near the $\text{SiO}_2 / \text{Si}(p)$ interface of trench MIS TD under read “-1” operation at (a) time = 1.35 ms, (b) time = 2.35 ms, (c) time = 4.35 ms, and (d) time = 30 ms under read “-1” operation. As the time goes, the recombination rate will reduce because of the fewer excess electrons.



Chapter 4

Influence of EOT on Transient Current Behavior of MIS TDs

4-1. Introduction

4-2. Results and Discussion

4-2-1. I-V Curves with Different EOTs

4-2-2. Memory Retention Properties with Different EOTs

4-2-3. Transient TCAD Simulation of MIS TDs with Different EOTs

4-3. Summary



4-1. Introduction

DESPITE the thorough discussion about the enhanced transient current of trench MIS TDs in **Chapter 3**, the study of how different equivalent oxide thicknesses (EOTs) of trench MIS TDs affect the transient current behavior is still absent. As a result, in this chapter, I-V characteristics and memory retention measurements of multiple MIS TDs with various EOTs are investigated. In addition, transient TCAD simulation of MIS TDs with different EOTs is adopted to support the experimental results.

4-2. Results and Discussion

4-2-1. I-V Curves with Different EOTs

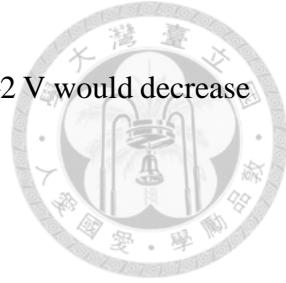
Fig. 4-1 and **Fig. 4-2** show the I-V characteristics of planar and trench MIS TDs with various EOTs respectively. At the first glance, one can notice the reverse bias currents ($I_G @ V_G > 0$ V) of trench devices are all smaller than it of planar devices no matter what EOTs are, which is reasonable based on the discussion in **Section 2-3-1**. To elucidate, according to the previous explanation, the lower reverse bias current of trench MIS TDs results from the insufficient supply of minority carriers from the neighbor Si(p) substrate. Based on this understanding, it can be speculated that whatever the EOT of MIS TDs is, trench MIS TDs always suffer from the lack of enough electrons and therefore, have smaller reverse bias current than it of planar MIS TDs.



Although all trench devices have similar small steady-state reverse bias current, they demonstrate different transient current behavior once they have different EOTs. To begin with, one of the criterion to judge the transient current behavior is the zero current voltages (ZCVs), where the current transition from negative to positive value or in reverse order happens (the same definition as in **Section 3-2-1**). If the devices exhibit strong transient displacement current, the ZCVs of the devices under two voltage sweeping directions would both split from $V_G = 0$ V (according to the discussion in **Section 3-2-1**). The stronger the transient current is, the bigger magnitude of the ZCVs will be. In **Fig. 4-2**, for the thicker oxide samples (EOT = 3.25 – 3.05 nm), the ZCVs of trench MIS TDs apparently deviate from $V_G = 0$ V. On the other hand, for the trench devices with thinner EOT values (EOT = 2.85 – 2.5 nm), the ZCVs almost equal to 0 V. The above observation implies that within the measured EOT range of the study, thicker EOT devices have stronger transient current behavior than thin EOT ones. The same trend can also be seen from the more obvious hysteresis phenomenon in the I–V curves with thicker EOTs.

4-2-2. Memory Retention Properties with Different EOTs

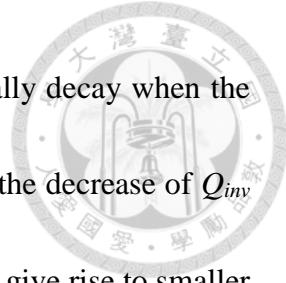
To enable deeper investigation, memory retention measurements as mentioned in **Section 3-2-2** are adopted to MIS TDs with different EOTs [see **Fig. 4-3** and **Fig. 4-4**]. In addition, the relation between EOT (used $|I_G| @ -2$ V to represent) and CW is organized in **Fig. 4-5**. Note that the forward bias current ($|I_G| @ -2$ V) is used to describe



the EOT of the devices. When the EOT becomes thicker, the $|I_G| @ -2 \text{ V}$ would decrease accordingly [see **Fig. 1-1**].

Consistent with the trend of I-V curves, only trench devices with thicker EOTs ($> 2.75 \text{ nm}$) have enhanced read “ -1 ” current $@ t = 0^+ \text{ s}$ [see **Fig. 4-3** and **Fig. 4-4**] and larger CW compared to planar ones [as shown in **Fig. 4-5**]. Nevertheless, for trench devices with thin EOTs ($< 2.75 \text{ nm}$), the negative transient current and CW become similar to them of planar MIS TDs. One of the reason is because when the EOT reduces, the total number of inversion charges (Q_{inv}) and inversion carriers (n_{inv}) accumulated at the $\text{SiO}_2 / \text{Si(p)}$ interface $@ V_G = +2 \text{ V}$ will decrease for the higher tunneling probability (P_t). To elucidate, the number of Q_{inv} and n_{inv} of MIS TDs is determined by two factors: C_{ox} and P_t . Although MIS TDs with thinner oxide would have higher C_{ox} [see (1-4)], which means the device can accumulate theoretically more inversion carriers, the also larger $P_t @ V_G = +2 \text{ V}$ would let the actual number of Q_{inv} and $n_{inv} @ V_G = +2 \text{ V}$ decrease [illustrated in **Fig. 4-6(a)** and **(b)**]. This might cause fewer Q_{excess} (“ -1 state) and smaller CW at thin EOT devices since transient current is proportional to Q_{excess} . Besides Q_{inv} and n_{inv} , higher P_t resulting in larger $|I_{h(T)}| + |I_{e(T)}|$ (positive transient current component) might be another reason for the smaller CW at thin EOTs.

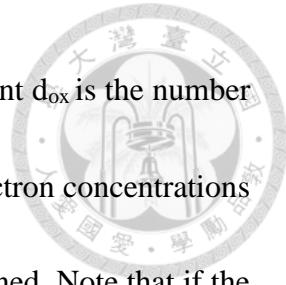
Based on the above discussion and **Fig. 4-5**, it seems that thicker EOTs will have better CW. However, this is not to say the CW of trench MIS TDs would infinitely



increase as EOT getting thicker. It is expected the CW will eventually decay when the EOT becomes too large for the reduction of C_{ox} . This might lead to the decrease of Q_{inv} and Q_{excess} (“-1” state) [illustrated in **Fig. 4-6(b)** and **(c)**] and further give rise to smaller transient current and CW. To sum up, CW of trench MIS TDs should have an optimal value at a specific EOT range, which can be confirmed in the simulation result of the following section.

4-2-3. Transient TCAD Simulation of MIS TDs with Different EOTs

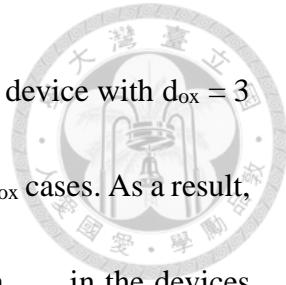
Utilizing the transient TCAD settings mentioned in **Fig. 3-12**, simulated read “-1” current of trench MIS TDs with different EOTs (or d_{ox}) can be studied. **Fig. 4-7** exhibits the simulated retention properties under read “-1” operation. It is worth noting that the simulated results show a similar trend between oxide thicknesses and read “-1” current to the measured retention characteristics at **Fig. 4-4**. To elaborate, both simulation and experiments demonstrate near zero transient current when d_{ox} is thin while large negative transient current at thick d_{ox} . Besides the memory retention results, the simulated CW– d_{ox} relation is also close to the measured CW–EOT trend of trench MIS TDs [see **Fig. 4-8**]. Furthermore, if more simulated CW results with wider range of d_{ox} are added, an optimal CW value, as predicted in the previous section, can be observed at d_{ox} around 3 nm [see **Fig. 4-9**].



To find out whether the cause of the optimal CW among different d_{ox} is the number of excess carriers as stated in **Section 4-2-2**, the contour plots of electron concentrations (n_e) of trench MIS TDs with different d_{ox} (2, 3, and 4 nm) are examined. Note that if the proposed explanation is right, one should find the excess carrier concentrations (n_{excess}) and n_e at $d_{ox} = 3$ nm are larger than at $d_{ox} = 2, 4$ nm because the CW is also larger at $d_{ox} = 3$ nm. **Fig. 4-10(a), (c), and (e)** show the n_e under log scale at $t = 1.35$ ms in the read “-1” operation while **Fig. 4-10(b), (d), and (f)** show the log scale n_e at steady-state $V_G = 0$ V. One can easily observe the trench device with $d_{ox} = 3$ nm have the highest inversion carrier concentrations among these three d_{ox} cases at the beginning of read “-1”, as shown in **Fig. 4-10(a), (c), and (e)**. As for **Fig. 4-10(b), (d), and (f)**, the log scale n_e at steady-state $V_G = 0$ V seem similar to each other. To access more useful information, linear scale contour plots of n_e are taken into account [see **Fig. 4-11**]. Different from the dimension scaling in **Fig. 4-10**, **Fig. 4-11** focuses on the n_e at $\text{SiO}_2 / \text{Si}(p)$ interface. Furthermore, n_{excess} can be extracted by the n_e difference between read “-1” operation at $t = 1.35$ ms condition [**Fig. 4-11(a), (c), and (e)**] and steady-state result @ 0V [**Fig. 4-11(b), (d), and (f)**], which can be written as

$$n_{excess} = n_e (@ t = 1.35 \text{ ms}) - n_e (@ t = \infty) \quad (4-1)$$

where $n_e (@ t = \infty)$ are the n_e at steady-state $V_G = 0$ V.



The extracted n_{excess} are shown in **Fig. 4-12**, which confirms the device with $d_{\text{ox}} = 3$ nm has the highest n_{excess} near the $\text{SiO}_2 / \text{Si(p)}$ interface among three d_{ox} cases. As a result, the proposed explanation that transient current is related to n_e and n_{excess} in the devices can be substantiated. One may have noticed that for the case of $d_{\text{ox}} = 2$ nm [see **Fig. 4-12(c)**], n_{excess} are smaller than zero, which is explicable since inversion carriers at steady-state $V_G = 2$ V are even fewer than them at steady-state $V_G = 0$ V at such thin d_{ox} . This fact results from the higher tunneling probability (P_t) at steady-state $V_G = 2$ V than at steady-state $V_G = 0$ V. Consequently, when V_G switches from 2 V to 0 V for trench MIS TDs with $d_{\text{ox}} = 2$ nm, n_{excess} are not only few but also negative values and contribute to the small transient current.

4-3. Summary

The relation between transient current and EOTs is studied in this chapter. It is found that trench MIS TDs exhibit enhanced transient current behavior when their EOTs are thick enough ($\text{EOT} \geq 2.75$ nm). However, at thin EOTs (≤ 2.6 nm), the transient current of trench devices decays to near-zero current as in planar devices. The reason for the oxide thickness dependent transient current in MIS TDs is attributed to different excess carrier concentrations in various EOTs. Followed by transient TCAD simulation of trench MIS TDs with different d_{ox} , the above explanation can be verified.

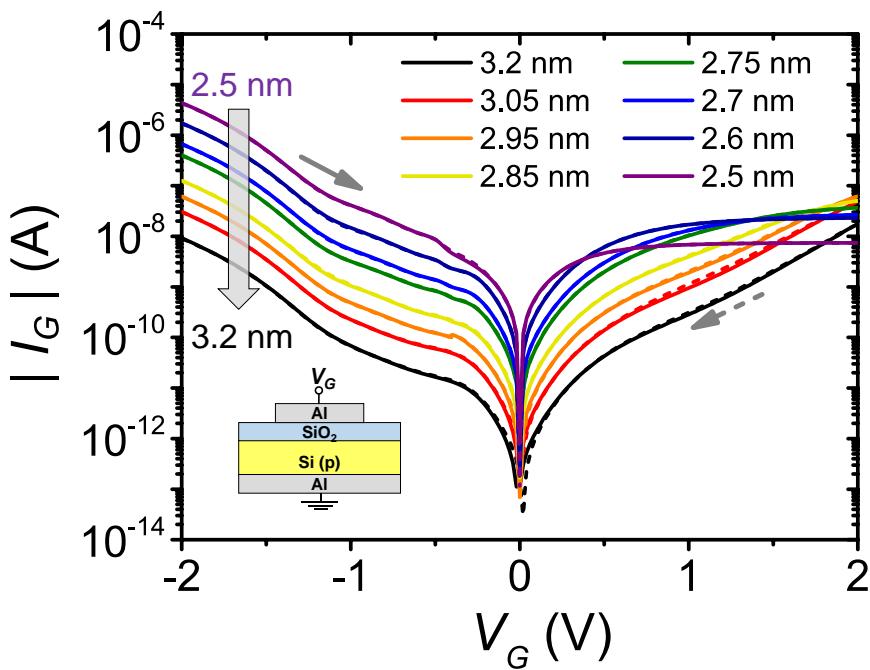
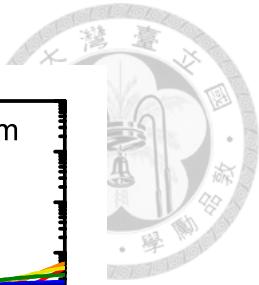


Fig. 4-1. I–V characteristics of planar MIS TDs with various EOTs. Solid: voltage sweeps forward. Dash: voltage sweeps backward. Voltage sweeping rate is about 75 mV/s.

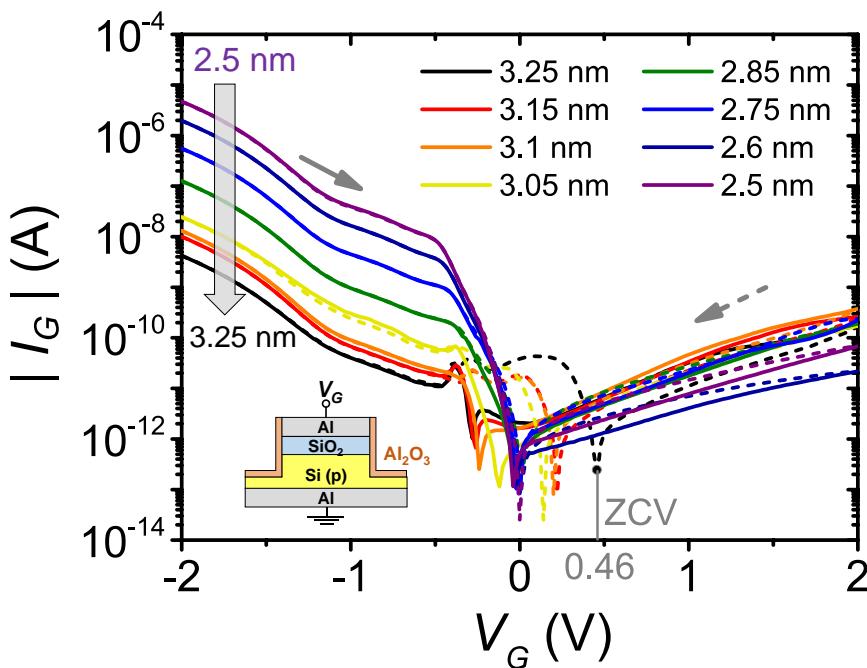


Fig. 4-2. I–V characteristics of trench MIS TDs with various EOTs. The zero current voltage (ZCV) of device with EOT = 3.25 nm at backward direction is 0.46 V. Solid: voltage sweeps forward. Dash: voltage sweeps backward. Voltage sweeping rate is about 75 mV/s.

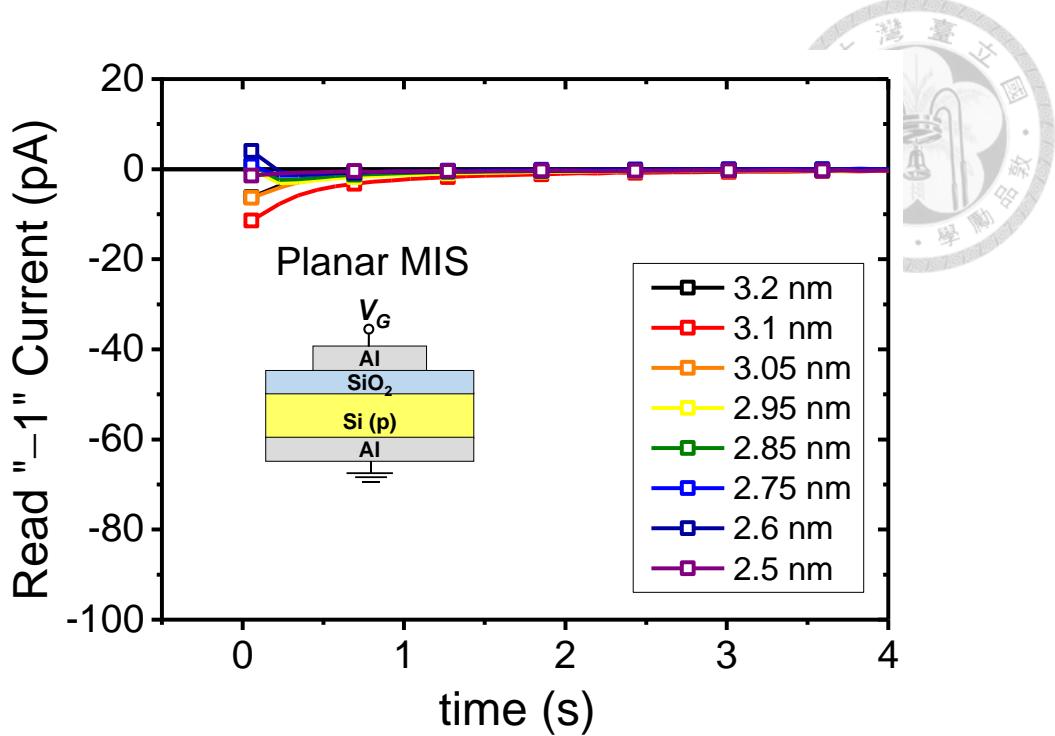


Fig. 4-3. Retention properties of planar MIS TDs with various EOTs (3.2–2.5 nm). Since read “0” current of all MIS TDs are close to 0, they are not shown in the figure for simplicity.

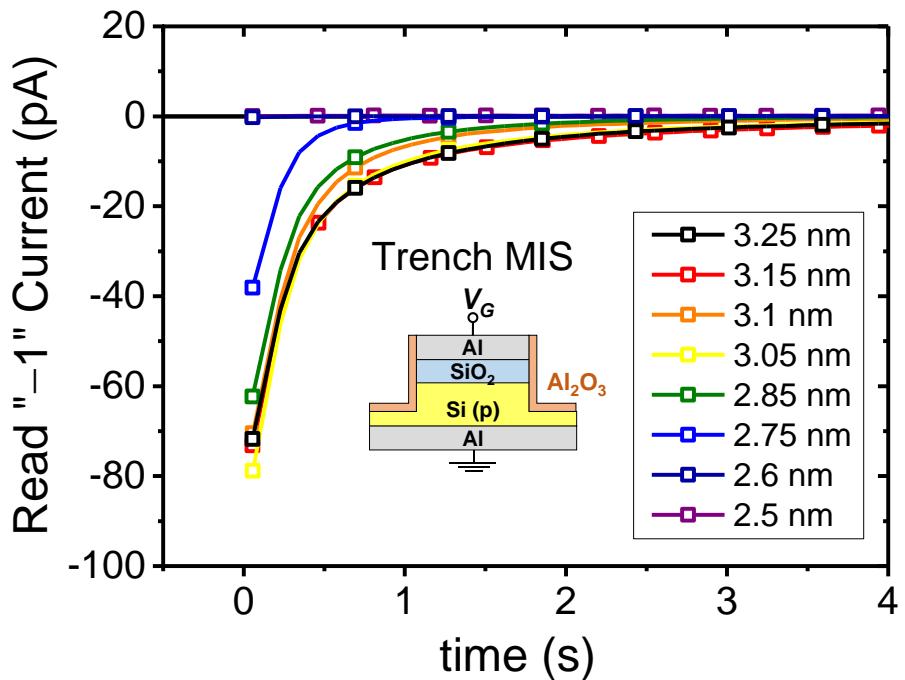


Fig. 4-4. Retention properties of trench MIS TDs with various EOTs (3.25–2.5 nm). Since read “0” current of all MIS TDs are close to 0, they are not shown in the figure for simplicity.

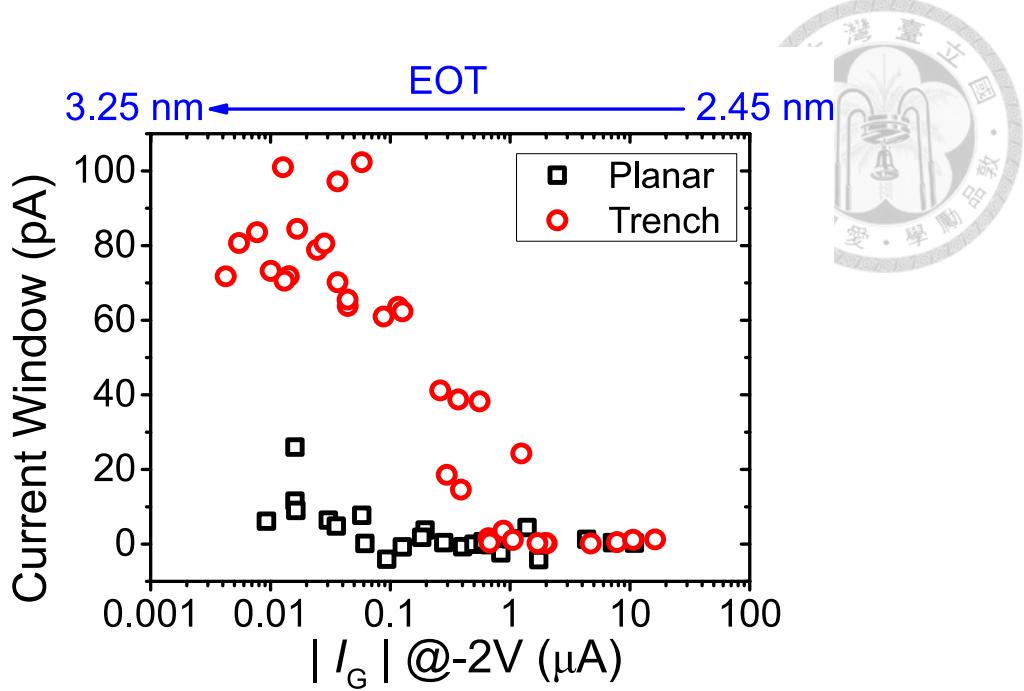


Fig. 4-5. The current window (CW) of MIS TDs with different EOTs. The gate current at forward bias (-2 V) is used to represent the EOT. The thicker the EOT is, the smaller the $| I_G | @ -2\text{ V}$ becomes. Different $| I_G | @ -2\text{ V}$ values correspond to different EOT values of the devices.

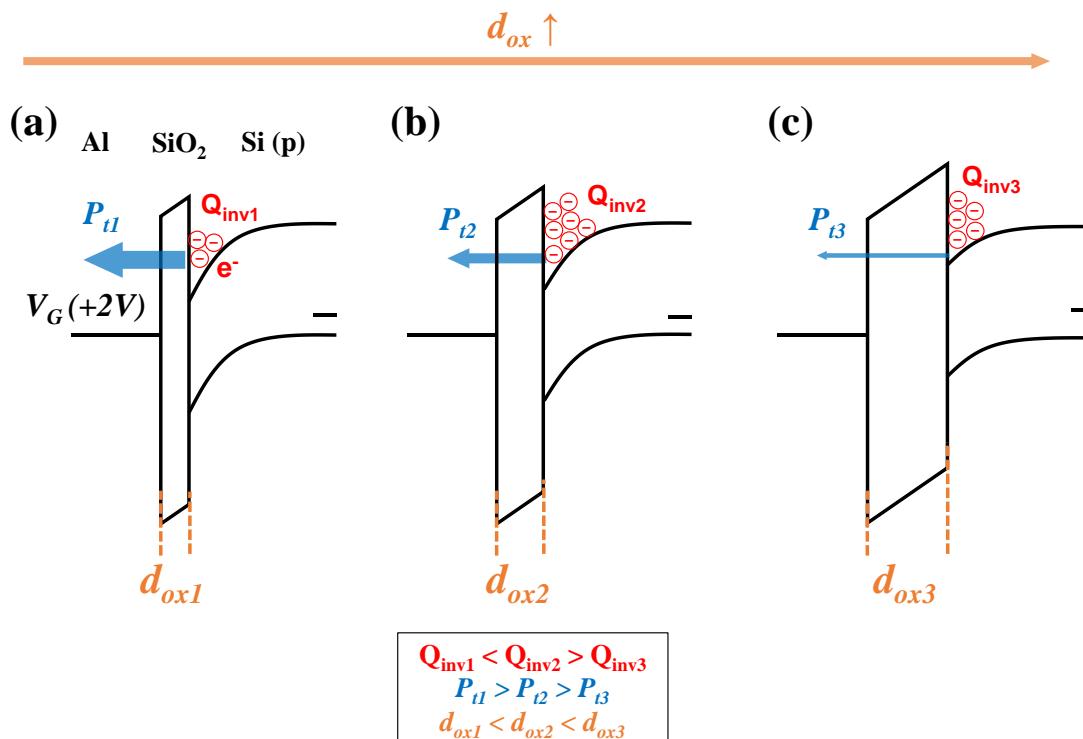


Fig. 4-6. Schematic band diagrams of MIS TDs with different oxide thicknesses (d_{ox}). Q_{inv} : total inversion charges. P_t : oxide tunneling probability.

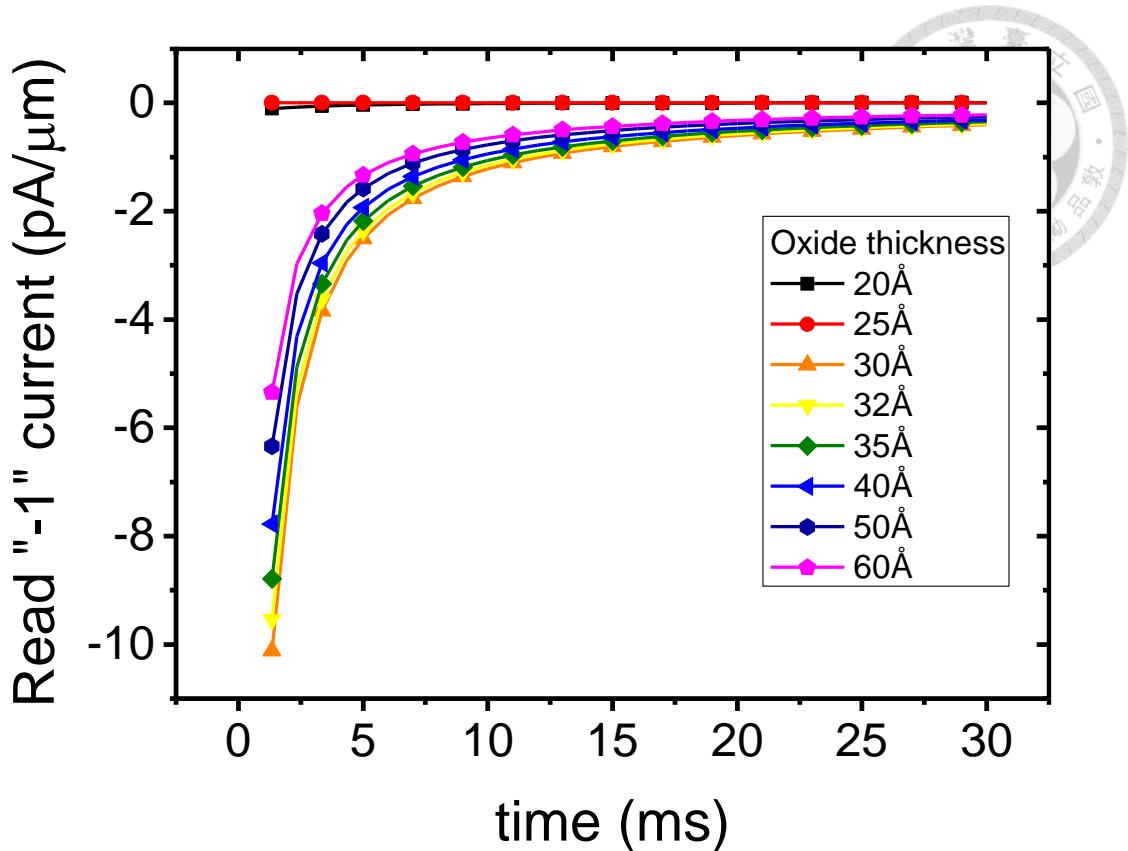


Fig. 4-7. Simulated retention result of trench MIS TDs with various d_{ox} under read “-1” operation. Although the time scale is different from the measured results in **Fig. 4-4**, the trend (thicker oxide have better transient current) of the negative current is almost the same as in **Fig. 4-4**. In the transient TCAD simulation, write “0” and read “0” operations are not simulated for the expected zero read “0” current.

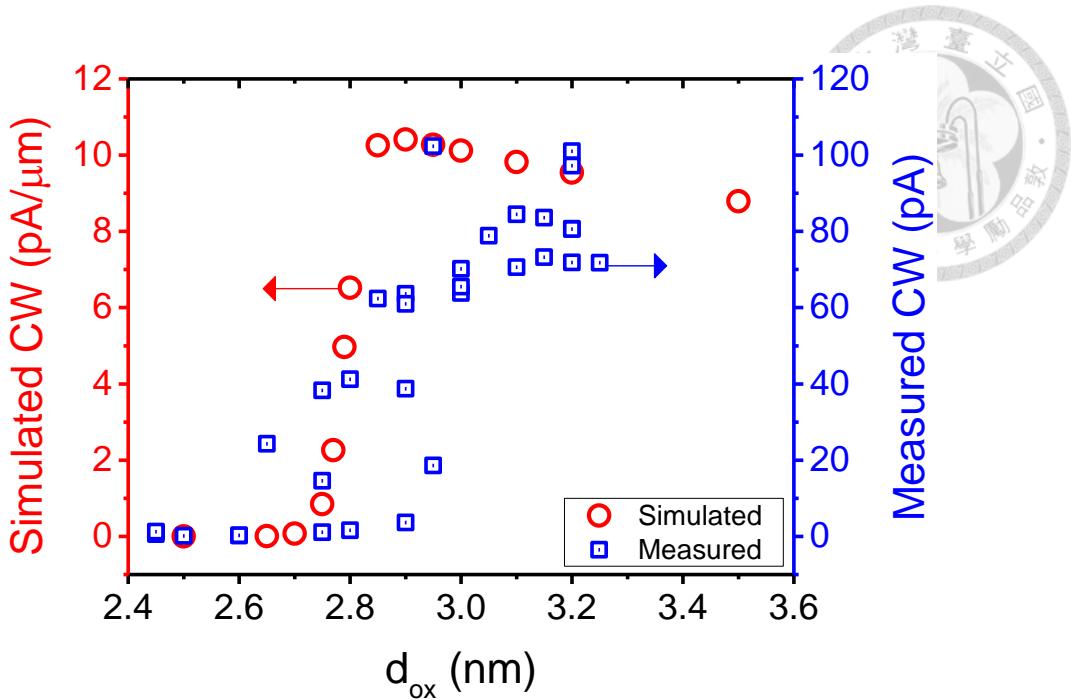


Fig. 4-8. Measured and simulated CW of trench MIS TDs at different d_{ox} (or EOTs). Since write “0” and read “0” operations were not simulated in the study, the simulated CW values are extracted by the modified definition, $| \text{read “-1” current} @ t = 1.35 \text{ ms} |$, based on (3-9). **Red symbols:** simulated data. **Blue symbols:** measured data of trench devices that were shown before in **Fig. 4-5**.

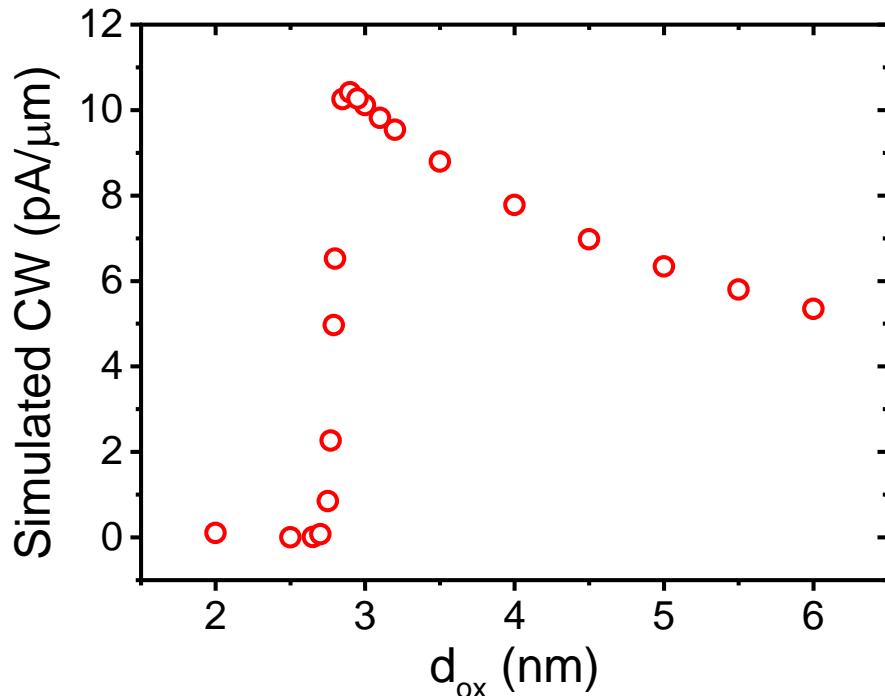


Fig. 4-9. Simulated CW of trench MIS TDs at different $d_{ox} = 2$ to 6 nm. More simulated CW data compared to **Fig. 4-8** are added to enable the discussion of optimal CW.

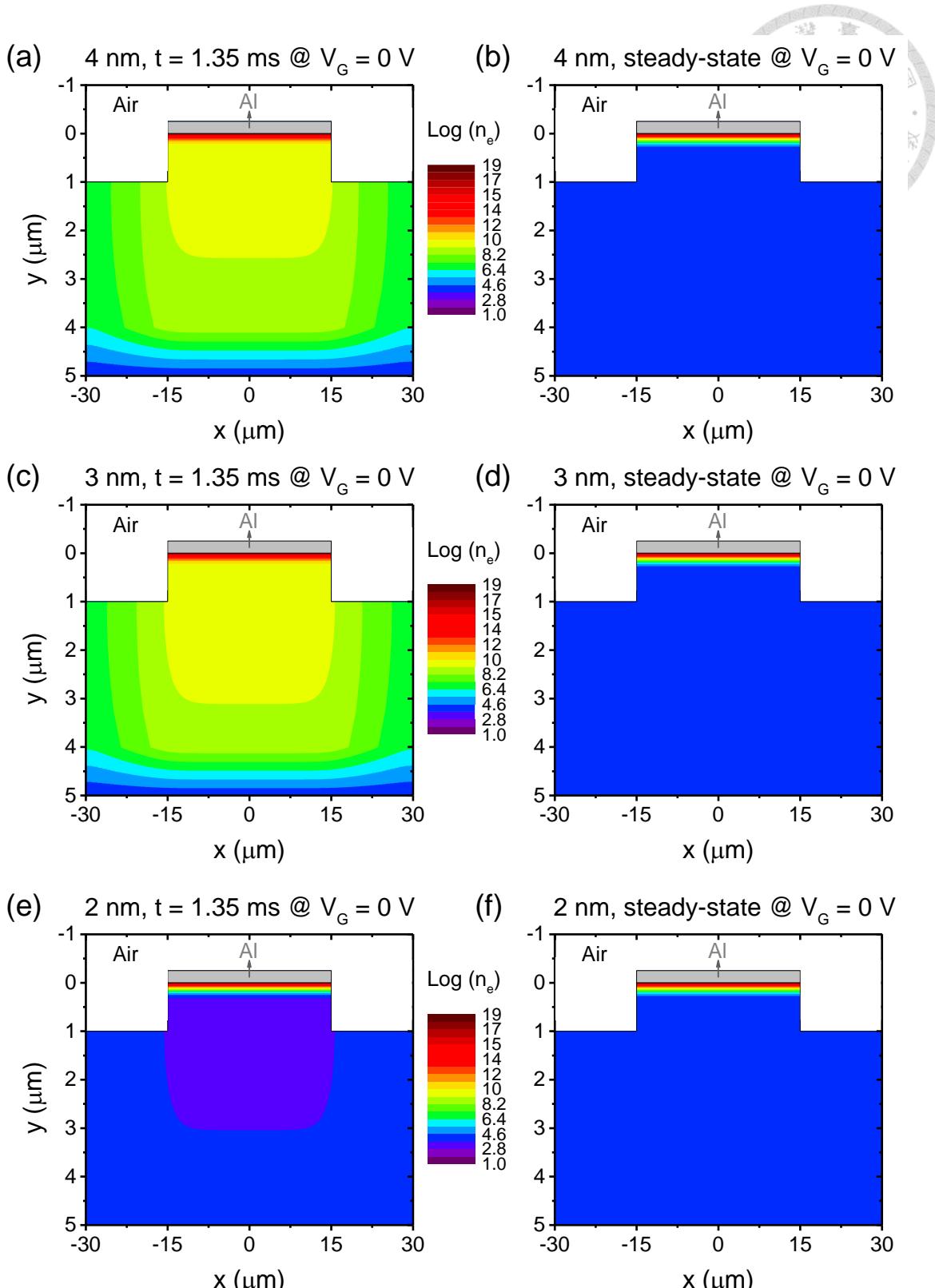


Fig. 4-10. Contour plots of electron concentration (n_e) of trench MIS TDs with (a–b) $d_{\text{ox}} = 4$ nm, (c–d) $d_{\text{ox}} = 3$ nm, and (e–f) $d_{\text{ox}} = 2$ nm under log scale. (a), (c), and (e) show the transient n_e under read “ -1 ” operation at $t = 1.35$ ms. (b), (d), and (f) show the steady-state n_e at $V_G = 0$ V, which can be viewed as the transient solution of n_e at $t = \infty$.

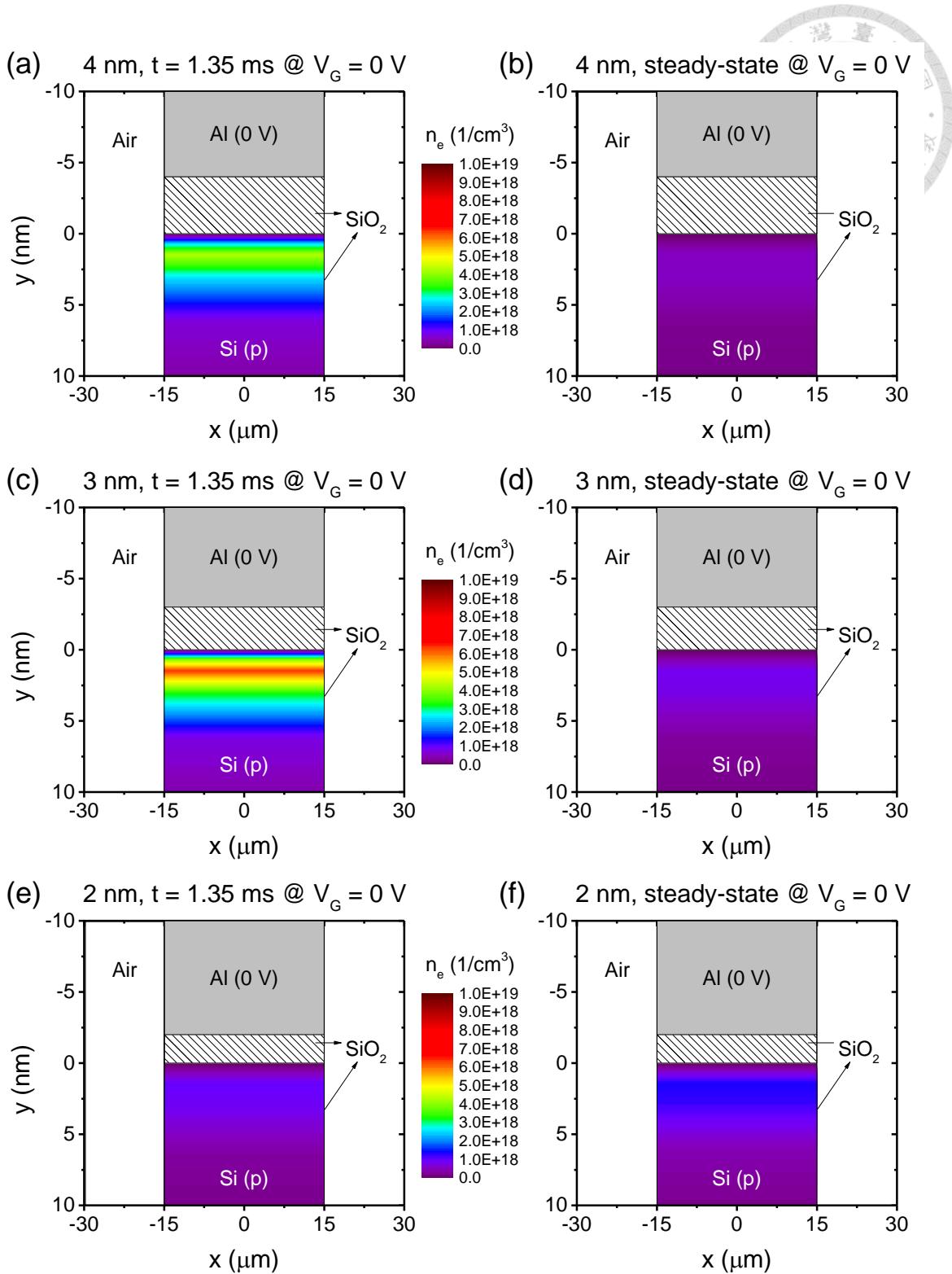


Fig. 4-11. Contour plots of electron concentration (n_e) of trench MIS TDs with (a–b) $d_{\text{ox}} = 4$ nm, (c–d) $d_{\text{ox}} = 3$ nm, and (e–f) $d_{\text{ox}} = 2$ nm under linear scale. (a), (c), and (e) show the transient n_e under read “-1” operation at $t = 1.35$ ms. (b), (d), and (f) show the steady-state n_e at $V_G = 0$ V, which can be viewed as the transient solution of n_e at $t = \infty$.

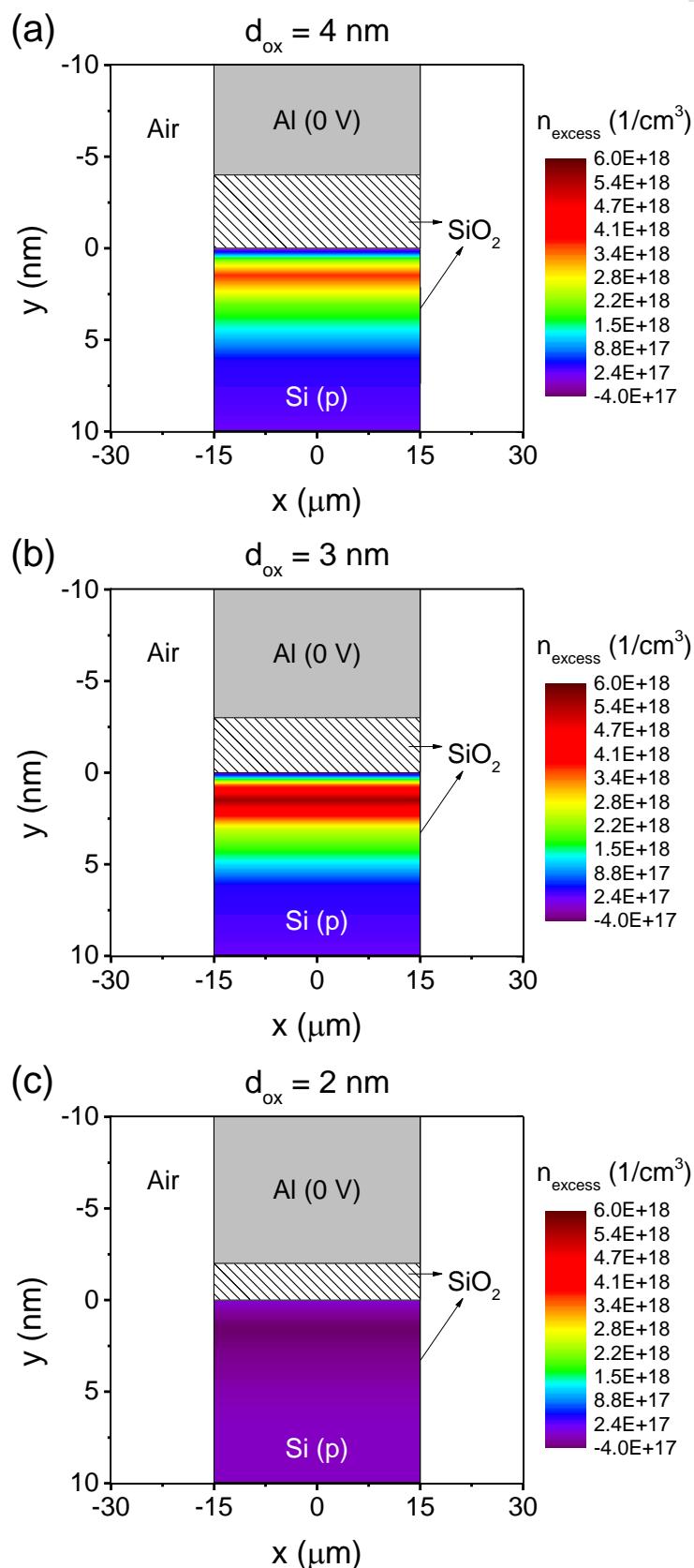


Fig. 4-12. Extracted excess carrier concentration (n_{excess}) of trench MIS TDs with (a) $d_{\text{ox}} = 4 \text{ nm}$, (b) $d_{\text{ox}} = 3 \text{ nm}$, and (c) $d_{\text{ox}} = 2 \text{ nm}$ under linear scale.

Chapter 5

Conclusion and Future Work



5-1. Conclusion

5-2. Future Work

5-2-1. The Distance Between the Gate Edge and the Trench

Edge

5-2-2. The Depth of the Trench

5-2-3. Effect of Different Sidewall Materials on the Transient Current Behavior



5-1. Conclusion

In the thesis, a new structure of MIS TDs, Trench MIS TD, is proposed and comprehensively studied. To sum up, compared with traditional Planar MIS TDs, Trench MIS TDs possess enhanced transient current behavior, which is of importance since it implies the potential of the devices for volatile memory applications. Though in the previous research, it has already been discovered that by changing the structure of MIS TDs, such as thinning down a partial portion of the gate metal thickness [14] and thickening the oxide at the gate edge [15], the transient current behavior of the altered structures MIS TDs can be largely enhanced. However, the altered MIS structures all need at least two masks photolithography process to fabricate. The proposed Trench MIS TDs offer a simpler solution to strengthening the transient current behavior of MIS TDs because they only require one mask photolithography process to fabricate, which can reduce the fabrication cost.

In **Chapter 2**, the I–V and C–V characteristics of trench devices were first studied since they give us an insight about the basic electrical properties difference between trench and planar MIS TDs. From the high frequency C–V measurement, it can be extrapolated that under the same oxide thickness, planar MIS TDs have more minority carriers supplied from the neighbor Si(p) substrate. On the other hand, trench MIS TDs



suffer from the insufficient minority carriers and the equivalently smaller V_{ox} , which results in the lower reverse bias current of trench devices compared with planar ones.

Besides steady-state current and capacitance properties, transient current behavior was also studied in **Chapter 3**. From I–V curves with different voltage sweeping rates, memory retention, and memory endurance measurements, it was confirmed that trench MIS TDs have better transient current and enhanced read “–1” negative transient current than planar MIS TDs. The reason for the stronger transient behavior of trench devices can be elucidated by the proposed “Thermal equilibrium model”, which is also related to the average lower V_{ox} in trench MIS TDs.

Eventually, the relation between EOTs and the transient current is discussed in **Chapter 4**. Because MIS TDs with different EOTs would have different number of excess carriers, the magnitude of the read “–1” negative transient current would also change accordingly. Based on the experimental and transient TCAD simulation results, it is suspected that there is an optimal EOT (around 3 nm) for MIS TDs to have the best transient current and memory CW. Moreover, it has been demonstrated by the experimental results that trench MIS TDs possess better CW at a wide range of EOTs.



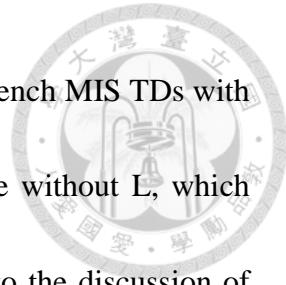
5-2. Future Work

Although the proposed trench MIS TDs have already shown stronger transient current than planar ones, there are still plenty of ways, which are listed in this section as future work, to further improve the transient current of trench devices.

5-2-1. The Distance Between the Gate Edge and the Trench Edge

In the discussion of **Chapter 3** and **Chapter 4**, the key difference between planar and trench devices is that the Si substrate outside the gate edge is partially removed in trench MIS TDs. As a result, for trench MIS TDs, the supply number of minority carriers (electrons) from the Si substrate is fewer than planar MIS TDs. However, it is ideal case that all Si (p) substrate right outside the gate electrode is partially removed and the gate edge aligns well with the trench edge. In fact, because of the Al wet etching process, the Al gate edge of the fabricated device did not well align with the trench edge. For example, one can see the TEM image of one of the trench device, as shown in **Fig. 5-1(b)**. The distance (denoted as L) between the trench sidewall (edge) and the Al gate edge is about 500 nm, which was created by the Al wet etching process [see the step 4 in **Fig. 5-2**]. Ideally, L value should be zero to perfectly limit the supply of minority carriers from the neighbor substrate outside the Al gate edge in trench MIS TDs, as illustrated in **Fig. 5-3(b)**.

On the contrary, in the actual case, the nonzero undercut distance, L, results in some supply (still less than planar structure MIS TDs) of electrons from the neighbor Si (p) to



the edge of trench devices, as shown in **Fig. 5-3(a)**. Consequently, trench MIS TDs with nonzero L will have equivalently larger V_{ox} than the trench device without L, which further degrades the negative transient current behavior according to the discussion of **Section 3-2-3**. In other words, to have maximum negative transient current, near-zero undercut distance L, which can be achieved by Al dry etching, is needed. More comprehensive examination about the influence of the undercut distance can be studied in the future.

5-2-2. The Depth of the Trench

Fig. 5-4 shows the depth of the trench (denoted as D) is about 340 nm. It is intuitive that different D values should have some impact on the transient current of trench MIS TDs, which is not discussed in this thesis. Consequently, thorough study about the influence of the trench depth is suggested as part of the future work.

5-2-3. Effect of Different Sidewall Materials on the Transient Current Behavior

In **Chapter 2**, Al_2O_3 sidewall was used in trench MIS TDs to protect the exposed Si substrate from reacting with air and moisture. However, different sidewall materials should have different effect on the transient current behavior since the interface between the sidewall materials and the Si substrate have different quality and defect density, which



might change the amount of Q_{excess} . To examine the above concern, another type of trench MIS TDs with SiO₂ sidewall, whose process flow is shown in **Fig. 5-5**, was fabricated.

Fig. 5-6 demonstrates the I-V curves of a trench MIS TD with SiO₂ sidewall (denoted as Trench: SiO₂) compared with planar and trench MIS TD with Al₂O₃ sidewall (denoted as Trench: Al₂O₃). One can observe that Trench: SiO₂ also show enhanced transient current similar to Trench: Al₂O₃ device. Moreover, in the memory 1000 cycles endurance measurement [see **Fig. 5-7**], the Trench: SiO₂ exhibit bigger CW than planar MIS TDs. Nonetheless, one can also note that the CW of the Trench: SiO₂ is smaller than it of the Trench: Al₂O₃ device. This might result from the different interface quality at the trench sidewall. In conclusion, **Fig. 5-7** implies that changing the sidewall material is a way to improve the transient current behavior of trench MIS TDs. Hence, this part can also be studied in the future.

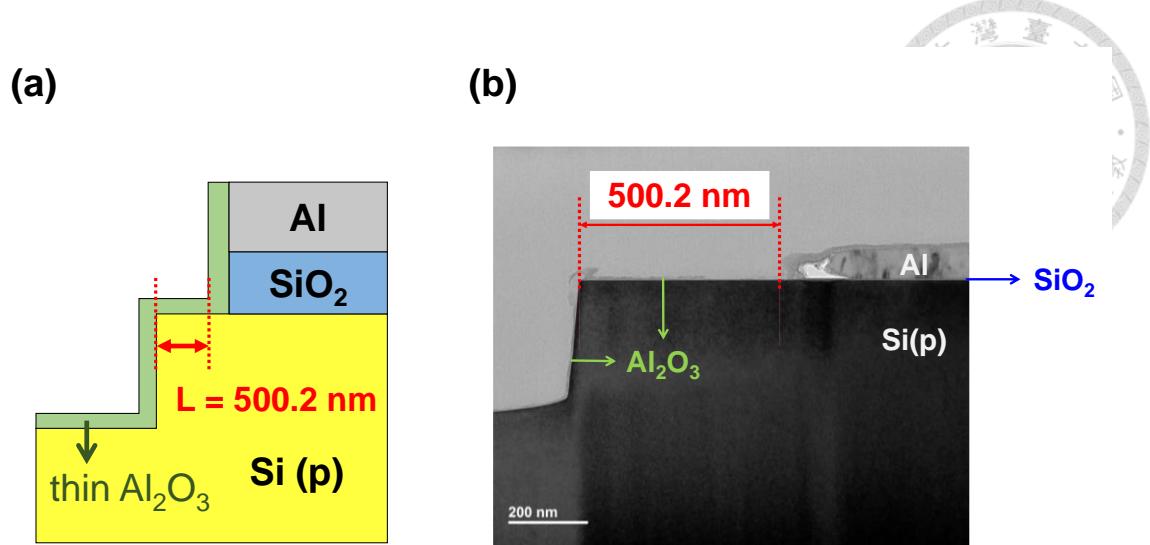


Fig. 5-1. (a) Schematic structure of trench MIS TDs. (b) TEM image of the trench MIS TDs. The distance L between the trench edge and the metal gate is about 500.2 nm.

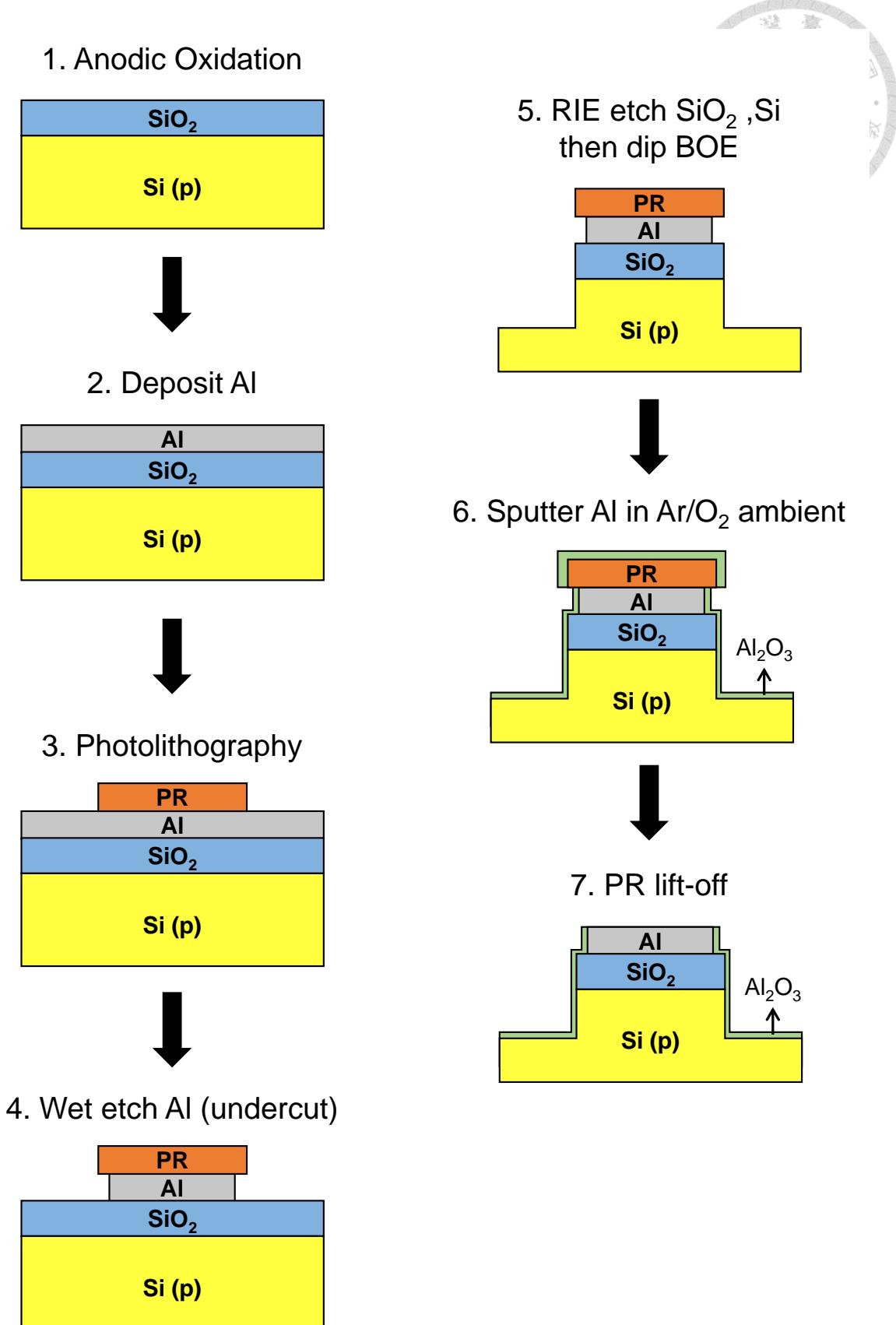


Fig. 5-2. Fabrication process flow of trench MIS TDs. Because of the Al wet etching process (step 4), the generated undercut creates distance between Al and trench edge.

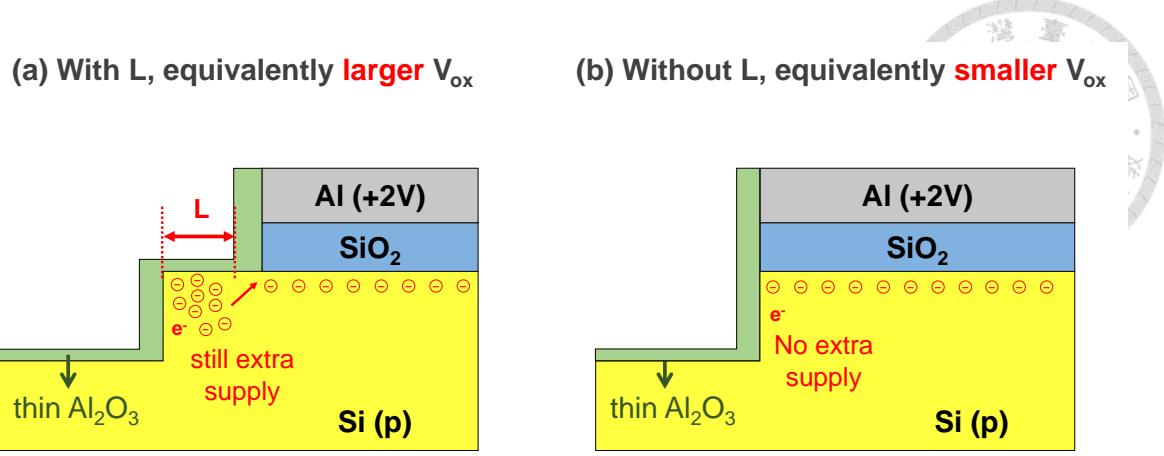


Fig. 5-3. (a) Trench MIS TD with undercut distance L will have equivalently larger V_{ox} because of more minority carriers supply. (b) Trench MIS TD without undercut will have equivalently smaller V_{ox} considering fewer minority carriers supply from neighbor substrate.

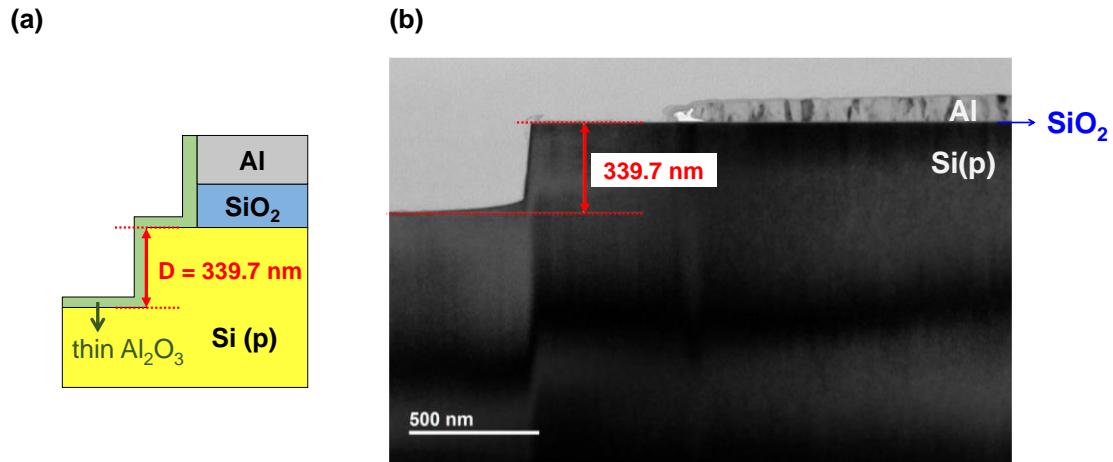


Fig. 5-4. (a) Schematic structure of trench MIS TDs. (b) TEM image of the trench MIS TDs. The depth of the trench structure D is about 339.7 nm.

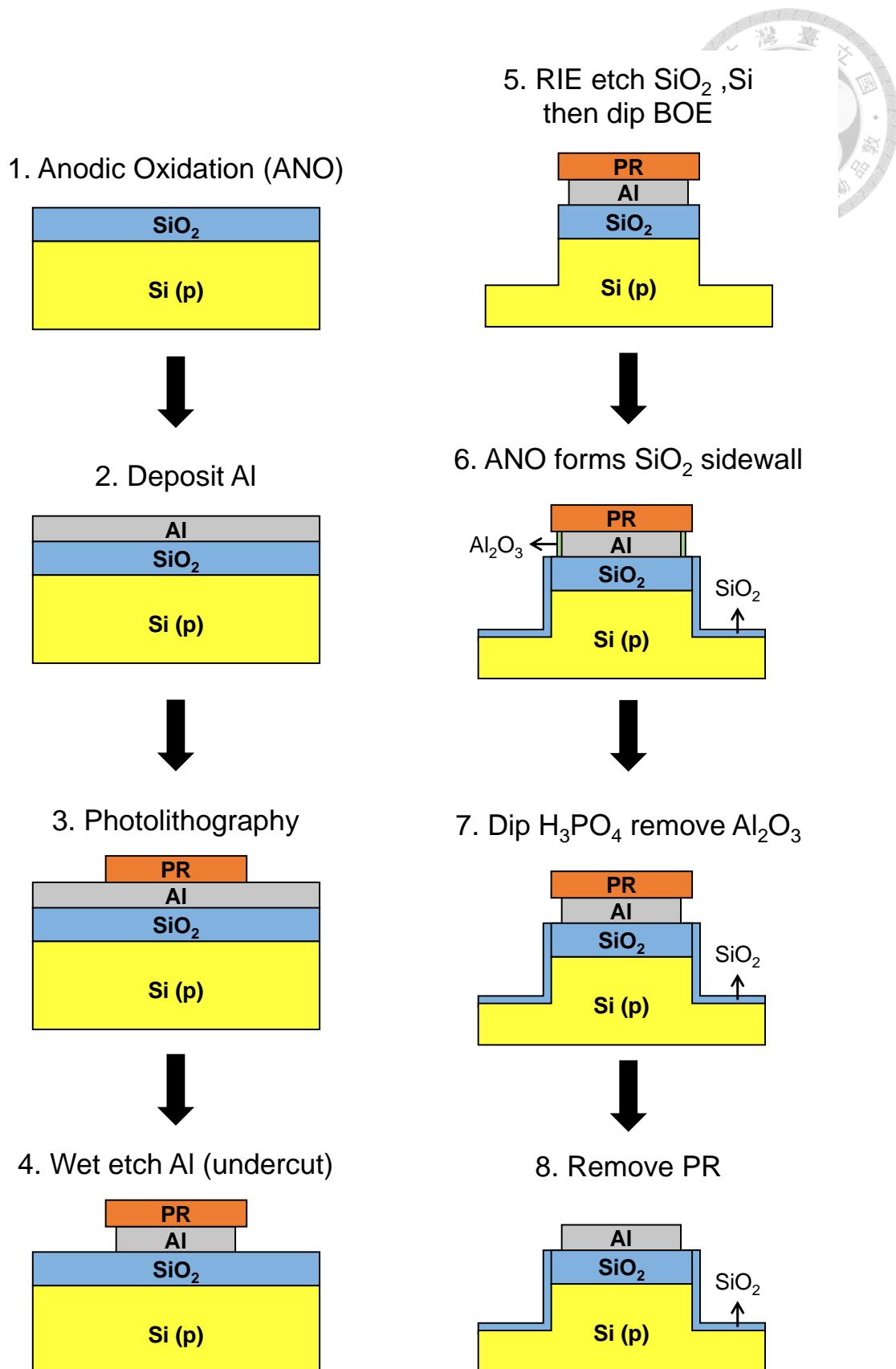


Fig. 5-5. Fabrication process flow of trench MIS TDs with SiO_2 sidewall.

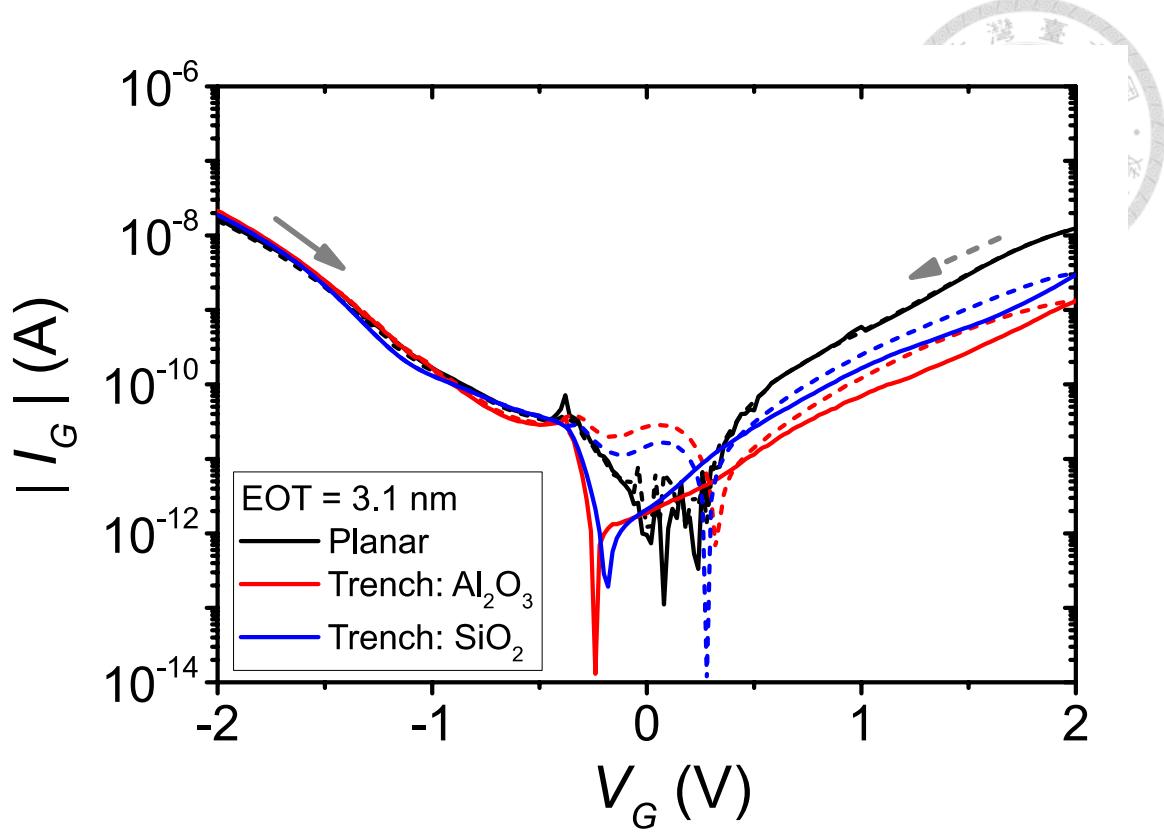


Fig. 5-6. I–V curves of planar and trench MIS TDs with voltage sweeping rate ≈ 75 mV/s. Trench: Al_2O_3 represents the trench MIS TDs with sputtered Al_2O_3 sidewall. Trench: SiO_2 represents the trench MIS TDs with ANO SiO_2 sidewall. Solid: voltage sweeps forward. Dash: voltage sweeps backward.

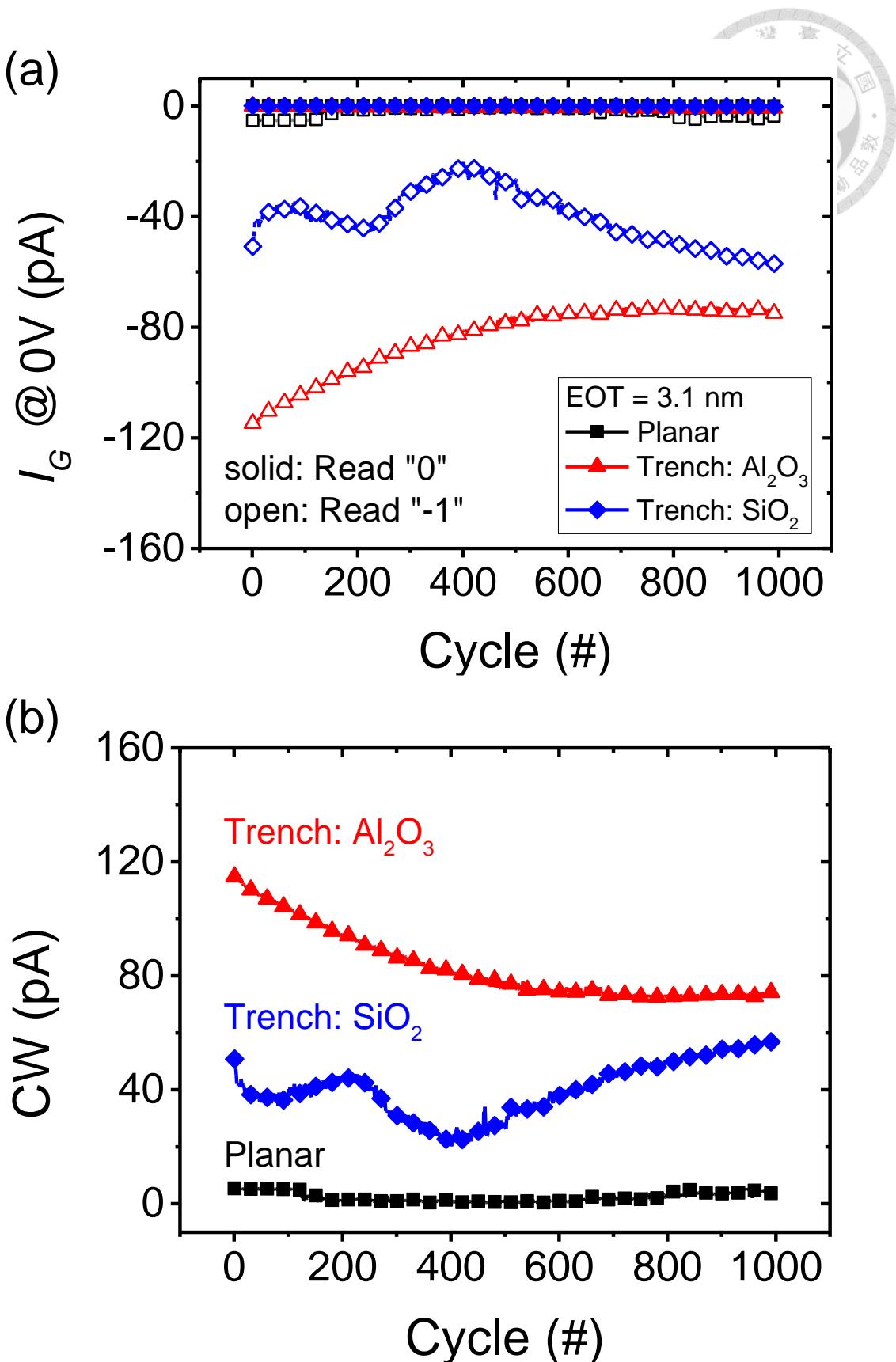
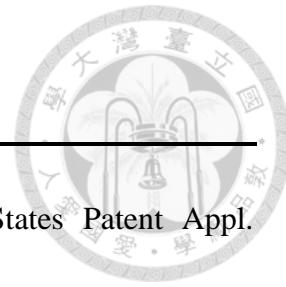
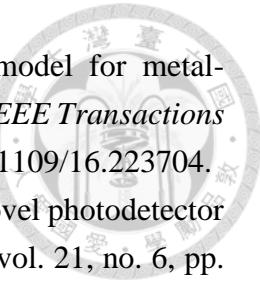


Fig. 5-7. Endurance characteristics using the same read, write “-1”, and write “0” settings as in **Fig. 3-2**. Trench: Al_2O_3 represents the trench MIS TDs with sputtered Al_2O_3 sidewall. Trench: SiO_2 represents the trench MIS TDs with ANO SiO_2 sidewall.



References

- [1] R. H. Dennard, "Field-effect transistor memory," United States Patent Appl. 3387286, 1968.
- [2] S. Okhonin, M. Nagoga, J. M. Sallese, and P. Fazan, "A capacitor-less 1T-DRAM cell," *IEEE Electron Device Letters*, vol. 23, no. 2, pp. 85-87, 2002, doi: 10.1109/55.981314.
- [3] C. Kuo, K. Tsu-Jae, and H. Chenming, "A capacitorless double gate DRAM technology for sub-100-nm embedded and stand-alone memory applications," *IEEE Transactions on Electron Devices*, vol. 50, no. 12, pp. 2408-2416, 2003, doi: 10.1109/TED.2003.819257.
- [4] S. Navarro *et al.*, "Reliability Study of Thin-Oxide Zero-Ionization, Zero-Swing FET 1T-DRAM Memory Cell," *IEEE Electron Device Letters*, vol. 40, no. 7, pp. 1084-1087, 2019, doi: 10.1109/LED.2019.2915118.
- [5] Y. J. Yoon, J. H. Seo, S. Cho, J.-H. Lee, and I. M. Kang, "A polycrystalline-silicon dual-gate MOSFET-based 1T-DRAM using grain boundary-induced variable resistance," *Applied Physics Letters*, vol. 114, no. 18, p. 183503, 2019/05/06 2019, doi: 10.1063/1.5090934.
- [6] J. H. Seo *et al.*, "Fabrication and Characterization of a Thin-Body Poly-Si 1T DRAM With Charge-Trap Effect," *IEEE Electron Device Letters*, vol. 40, no. 4, pp. 566-569, 2019, doi: 10.1109/LED.2019.2901003.
- [7] M. A. Green, F. D. King, and J. Shewchun, "Minority carrier MIS tunnel diodes and their application to electron- and photo-voltaic energy conversion—I. Theory," *Solid-State Electronics*, vol. 17, no. 6, pp. 551-561, 1974/06/01/ 1974, doi: [https://doi.org/10.1016/0038-1101\(74\)90172-5](https://doi.org/10.1016/0038-1101(74)90172-5).
- [8] J. Shewchun, M. A. Green, and F. D. King, "Minority carrier MIS tunnel diodes and their application to electron- and photo-voltaic energy conversion—II. Experiment," *Solid-State Electronics*, vol. 17, no. 6, pp. 563-572, 1974/06/01/ 1974, doi: [https://doi.org/10.1016/0038-1101\(74\)90173-7](https://doi.org/10.1016/0038-1101(74)90173-7).
- [9] M. Y. Doghish and F. D. Ho, "A comprehensive analytical model for metal-insulator-semiconductor (MIS) devices," *IEEE Transactions on Electron Devices*, vol. 39, no. 12, pp. 2771-2780, 1992, doi: 10.1109/16.168723.
- [10] C. Liao and J. Hwu, "Remote Gate-Controlled Negative Transconductance in Gated MIS Tunnel Diode," *IEEE Transactions on Electron Devices*, vol. 63, no. 7, pp. 2864-2870, 2016, doi: 10.1109/TED.2016.2565688.



- [11] M. Y. Doghish and F. D. Ho, "A comprehensive analytical model for metal-insulator-semiconductor (MIS) devices: a solar cell application," *IEEE Transactions on Electron Devices*, vol. 40, no. 8, pp. 1446-1454, 1993, doi: 10.1109/16.223704.
- [12] C. W. Liu, W. T. Liu, M. H. Lee, W. S. Kuo, and B. C. Hsu, "A novel photodetector using MOS tunneling structures," *IEEE Electron Device Letters*, vol. 21, no. 6, pp. 307-309, 2000, doi: 10.1109/55.843159.
- [13] S. Yen-Hao and H. Jenn-Gwo, "An on-chip temperature sensor by utilizing a MOS tunneling diode," *IEEE Electron Device Letters*, vol. 22, no. 6, pp. 299-301, 2001, doi: 10.1109/55.924848.
- [14] K. Tseng, C. Liao, and J. Hwu, "Enhancement of Transient Two-States Characteristics in Metal-Insulator-Semiconductor Structure by Thinning Metal Thickness," *IEEE Transactions on Nanotechnology*, vol. 16, no. 6, pp. 1011-1015, 2017, doi: 10.1109/TNANO.2017.2740943.
- [15] Y.-C. Yang, K.-W. Lin, and J.-G. Hwu, "Transient Two-State Characteristics in MIS(p) Tunnel Diode with Edge-Thickened Oxide (ETO) Structure," *ECS Journal of Solid State Science and Technology*, vol. 9, no. 10, p. 103006, 2020/11/03 2020, doi: 10.1149/2162-8777/abc576.
- [16] S. M. Sze and K. K. Ng, "Tunnel Devices," in *Physics of Semiconductor Devices*, 2006, pp. 415-465.
- [17] K. J. Yang and H. Chenming, "MOS capacitance measurements for high-leakage thin dielectrics," *IEEE Transactions on Electron Devices*, vol. 46, no. 7, pp. 1500-1501, 1999, doi: 10.1109/16.772500.
- [18] K. Yang, K. Ya-Chin, and H. Chenming, "Quantum effect in oxide thickness determination from capacitance measurement," in *1999 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.99CH36325)*, 14-16 June 1999 1999, pp. 77-78, doi: 10.1109/VLSIT.1999.799348.
- [19] Berkeley Device Group QM CV Simulator [Online] Available: <http://www-device.eecs.berkeley.edu/qmcv/qmcv.htm>
- [20] C. Liao, W. Kao, and J. Hwu, "Energy-Saving Write/Read Operation of Memory Cell by Using Separated Storage Device and Remote Reading With an MIS Tunnel Diode Sensor," *IEEE Journal of the Electron Devices Society*, vol. 4, no. 6, pp. 424-429, 2016, doi: 10.1109/JEDS.2016.2591956.
- [21] C.-H. Chang and J.-G. Hwu, "Trapping characteristics of Al₂O₃/HfO₂/SiO₂ stack structure prepared by low temperature in situ oxidation in dc sputtering," *Journal of Applied Physics*, vol. 105, no. 9, p. 094103, 2009/05/01 2009, doi: 10.1063/1.3120942.
- [22] C. Lin and J. Hwu, "Comparison of the Reliability of Thin Al₂O₃ Gate Dielectrics Prepared by In Situ Oxidation of Sputtered Aluminum in Oxygen Ambient With and

Without Nitric Acid Compensation," *IEEE Transactions on Device and Materials Reliability*, vol. 11, no. 2, pp. 227-235, 2011, doi: 10.1109/TDMR.2011.2108300.

