Jian-Yu (Jerry) Lin

ck10100398@gmail.com | jerryjianlin.github.io/ | jian-yu-lin-582683164

Research Interests

- Semiconductor Physics and Devices
- Emerging Memory Devices
- Metal-Oxide-Semiconductor (MOS) Devices
- Transistors

Education

National Taiwan University (NTU) *Taipei, Taiwan*

M.S. in Electronics Engineering *09/2019 - 06/2021*

- Overall GPA: **4.3/4.3**
- Rank: **1/136 (1%)**

National Taiwan University (NTU) *Taipei, Taiwan*

B.S. in Electrical Engineering *09/2015 - 06/2019*

- Overall GPA: **4.15/4.3**
- Rank: **14/190 (7%)**

Publication

Journal

1. **Jian-Yu Lin** and Jenn-Gwo Hwu, "Enhanced Transient Behavior in MIS(p) Tunnel Diodes by Trench Forming at the Gate Edge," *IEEE Transactions on Electron Devices*, vol. 68, no. 9, pp. 4189-4194, Sept. 2021, doi: 10.1109/TED.2021.3095052. [Github link]

Conference

1. **Jian-Yu Lin** and Jenn-Gwo Hwu, "Enhanced Memory Properties in MIS TD by Forming Trench Structure at the Gate Edge," *2020 International Electronic Devices and Materials Symposium (IEDMS)*, 5021, C1-3, Chang Gung University, Tao-Yuan City, Taiwan, ROC, Oct. 2020. (oral presentation) [Github link]
2. **Jian-Yu Lin** and Jenn-Gwo Hwu, "Dependency of Transient Current Behavior on Oxide Thickness in Trench Structure MIS TDs," *2021 International Electronic Devices and Materials Symposium (IEDMS)*, 1032, C3-1, National Cheng Kung University, Tainan City, Taiwan, ROC, Nov. 2021. (oral presentation, Best Paper Award) [Github link]

Patent

1. Jenn-Gwo Hwu and **Jian-Yu Lin**, "MIS-TD Memory with Shallow Trench Edge Passivation Structure," under application through Taiwan Semiconductor Manufacturing Company (TSMC) and NTU.

Research Experience

Capacitance–Voltage Lab, NTU *Taipei, Taiwan*

Graduate and Undergraduate Research Assistant (*with Prof. Jenn-Gwo Hwu*) *09/2018 - Present*

1. Enhanced Memory Property in Trench Structure Metal-Insulator-Semiconductor (MIS) Tunnel Diode (TD) with Thin Oxide (2.5 nm) **(Conference #1)**
   - Designed new device structure for MIS TDs, called **trench structure MIS TDs** (abbreviated as Trench MIS).
   - Improved memory property, current window (CW), of MIS TDs by utilizing **defects and traps** at trench structure.
   - Achieved **5 times larger CW** in Trench MIS devices compared to normal structure MIS TDs (abbreviated as Planar MIS) in long time (>10 s) voltage stress memory endurance measurements.
2. Enhanced Transient Current in Trench Structure MIS TD with Thick Oxide (≥ 2.8 nm)
   - Investigated stronger transient currents in Trench MIS compared to them in Planar MIS.
   - Proposed that **weaker oxide electric field** in Trench MIS is the reason for enhanced transient currents.
   - Utilized Trench MIS as memory devices by using different transient currents of MIS TDs to store memory data.
   - Accomplished **25 times larger CW** in Trench MIS compared to that in Planar MIS devices in short time (1 ms) voltage pulse memory endurance measurements. **(Journal #1)**
   - Examined dependency of transient current on oxide thickness in Trench MIS. **(Conference #2)**

Quantum Electronics Lab, NTU *Taipei, Taiwan*

Undergraduate Researcher (*with Prof. Jiun-Yun Li*) *09/2017 - 08/2018*

◇ GeSn Band Structure Calculations using Empirical Pseudopotential Method (EPM)
- Calculated band structure of Si, Ge, and GeSn based on a program called *Sentaurus Band Structure*.
- Adopted virtual crystal approximation to adjust Sn to Ge ratios in GeSn band structure calculations.

Work Experience

Teaching Assistant of Memory Circuit Technology, NTU — *Taipei, Taiwan*, *03/2021 - 06/2021*

Teaching Assistant of Solid State Electronics, NTU — *Taipei, Taiwan*, *10/2020 - 01/2021*

5 nm Device Department, Taiwan Semiconductor Manufacturing Company (TSMC) — *Hsinchu, Taiwan*, *07/2019 - 08/2019*

R&D Device Engineer, Summer Internship program (supervised by Dr. Chien-Tai Chan)

- Evaluated interface state density (D_{it}) of FinFETs by charge pumping (CP) method.
- Implemented CP measurements via TSMC's wafer acceptance test (WAT) computer programs, which are used by engineers to carry out electrical measurements.
- Authored an instruction document about how to analyze average and energy profiles of D_{it} using my WAT programs.
- **Finalist in the R&D group of the 2019 TSMC Summer Internship Competition (top 15% among all R&D interns)**.

Skills

Semiconductor Fabrication
- Radio Cooperation of America (RCA) clean
- Anodic oxidation
- Rapid thermal annealing (RTA)
- Furnace annealing
- Thermal evaporation
- Optical lithography
- Wet etching
- Reactive ion etching (RIE)
- DC sputtering
- Lift-off process

Electrical Measurement
- Agilent B1500A semiconductor device analyzer
- Capacitance–voltage (*C*–*V*)
- Current–voltage (*I*–*V*)
- Current/Voltage–time (*I*/*V*–*t*)
- Memory endurance & retention measurement

Software
- Silvaco technology computer-aided design (TCAD) simulation
- OriginLab
- Python
- Matlab
- LaTeX

Equipment Management
- Thermal evaporator

Honors & Awards

2021 **Best Paper Award, *2021 International Electronic Devices and Materials Symposium (IEDMS)***, Out of 22 orally-presented papers.

2021 **Honorary Member of Phi Tau Phi Scholastic Honor Society**, Academic performance with rank top 3% among master's graduands in the college.

2020-2021 **TSMC-NTU Research Center Research Assistant Scholarship (for master student)**, Given by TSMC each year to students at NTU based on their academic and research performance.

2019 **Course completion, Applied Materials - Advanced Technologies of Semiconductor and Display**, A course of study offered by Applied Materials Taiwan at NTU.

2019 **Finalist (top 10) in R&D group of 2019 TSMC Summer Internship Competition**, Based on project results and presentation skills (top 15% of all R&D interns).

2019 **Presidential Award, Department of Electrical Engineering, NTU**, Given each semester to students' ranking within the top 5% of their class (Rank: 1/203 at Spring'19).

2017-2019 **TSMC-NTU Research Center Research Assistant Scholarship (for undergraduate), 4 times**, Given by TSMC each semester to students at NTU based on their academic and research performance.

Language

English Proficiency (TOEFL)
- Date: 2021/2/28
- Total score = 108
- R/L/S/W = 29/29/23/27

GRE
- Date: 2020/11/28
- V/Q = 158/170
- AWA = 3.5

References

1. **Prof. Jenn-Gwo Hwu (master thesis and undergraduate research advisor)**, email: jghwu@ntu.edu.tw
2. **Prof. Jiun-Yun Li (undergraduate research advisor)**, email: jiunyun@ntu.edu.tw
3. **Dr. Chien-Tai Chan (intern supervisor and senior manager in Device Dept., N2 Platform Development Div., TSMC)**, email: ct_chan@tsmc.com