Dependency of Transient Current Behavior on Oxide Thickness in Trench Structure MIS TDs

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***Abstract* — In this article, the influence of various oxide thicknesses on the transient current behavior of trench structure metal-insulator-semiconductor (MIS) tunnel diodes (TDs) was examined. By current–voltage (*I–V*), retention measurements, and Technology Computer Aided Design (TCAD) simulation, we found that the magnitude of the transient current relates to the number of excess electrons.**

***Index Terms* — Metal–insulator–semiconductor (MIS), tunnel diode (TD), transient behavior, volatile memory, trench structure.**

I. Introduction

Because of the rising demand for memory in many applications, such as internet of things (IoT), artificial intelligence (AI), and Big data, research related to memory devices has become more and more important as well. Among this research area, transient behavior in semiconductor devices has gained a lot of interest because it can be utilized for volatile memory applications [1], [2]. Recently, metal-insulator-semiconductor (MIS) tunnel diodes (TDs) with special trench structure (denoted as trench MIS TDs) have been found with enhanced transient current behavior compared with traditional planar structure MIS TDs (denoted as planar MIS TDs) [3]. Although Lin *et al*. [3] demonstrated the potential of trench MIS TDs for memory application, the effect of various oxide thicknesses on the transient current was not comprehensively investigated. As a result, in this work, we used *I–V*, memory retention, and TCAD simulation to further investigate the oxide thickness dependency of the transient current in trench MIS TDs.

II. Experimental

Fig. 1 shows the schematic structure of planar and trench MIS TDs. The detailed fabrication processes of planar and trench devices were described in [3]. As for the simulation part, we utilized Silvaco TCAD to implement steady-state and transient simulation.

III. Results and Discussion

Fig.2 shows the current–voltage (*I–V*) curves of planar and trench MIS TDs. At EOT = 3.05 nm, the more obvious hysteresis phenomenon of the *I–V* curves indicates the trench device has larger transient current than planar devices. However, this transient current behavior seems to degrade as EOT keeps decreasing to 2.6 nm for one can find the hysteresis gradually disappear as EOT decreases.

The above trend can be further examined by memory retention measurements in **Fig. 3**, which also demonstrates the transient current of trench devices can be used to store different memory states. Although at thick oxide (3.05 nm), the trench MIS TD has stronger negative read "–1" current, this negative transient current declines as EOT becomes thinner. According to the previous work [3], negative read "–1" current originated from the fact that excess electrons generated in the process of V_G quickly switching from +2V to 0V are partly recombined by the displacement current ($I_{e(D)}$ and $I_{h(D)}$) [illustrated in **Fig. 4**]. As a result, the magnitude of the negative read "–1" current is believed to be proportional to the number of excess electrons, which is further proportional to the number of electrons at V_G = +2V. Since trench devices with thin EOT have higher oxide tunneling probability implying they could not hold too many electrons near the SiO_2/Si(p) interface, the excess electron concentration (n_{excess}) and the electron concentration (n_e) @ V_G = +2V of thin EOT (e.g. 2.6 nm) device should be less than them of thicker EOT (e.g. 3.05 nm) sample. This explains why trench MIS TDs with thin EOTs have smaller transient current and near-zero read "–1" current because they have less n_e @ V_G = +2V and fewer excess electrons.

The above explanation can be supported by transient TCAD simulation, whose process is shown in **Fig. 5**. **Fig. 6** and **Fig. 7** demonstrate the simulated results of read "–1" operation in the transient TCAD simulation. In **Fig. 6(c-d)**, one can observe that, as the oxide thickness (d_{ox}) increasing from 2.5 nm to 3 nm, excess electron concentration (n_{excess}) near the SiO_2/Si(p) interface in simulated read "–1" operation does rise as expected for lower tunneling probability can maintain more electrons near oxide at V_G = +2V. Furthermore, in **Fig. 7**, the thicker d_{ox} (3 nm) device also has a larger magnitude of read "–1" current than thinner d_{ox} (2.5 nm) devices, whose trend is similar to the experimental results in **Fig. 3**. Nonetheless, this is not to say trench MIS TDs would have infinitely larger transient current when d_{ox} keeps increasing. **Fig. 6(b)** shows that when d_{ox} is too thick (5 nm), the n_{excess} would decrease for the smaller oxide capacitance (C_{ox}) holding less n_e @ V_G = +2V, which further leads to the decline of read "–1" transient current [see **Fig. 7**]. To sum up, the transient current of trench MIS TDs should exist an optimal value at a specific d_{ox} range.

IV. Conclusion

In this work, we investigated the effect of oxide thickness on the transient current behavior of trench MIS TDs with experimental data and TCAD simulation support. The above results can enable us with deeper understanding of the transient current in trench MIS TDs.

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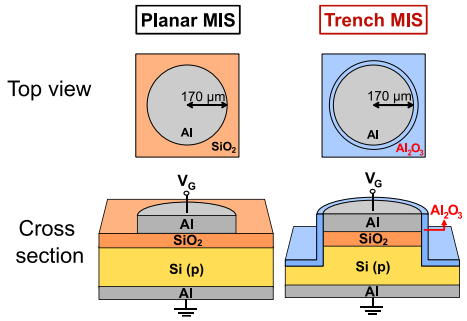

Fig. 1. Schematics of top views and cross-section views of planar MIS TDs (abbreviated as planar MIS) and trench MIS TDs (abbreviated as trench MIS).

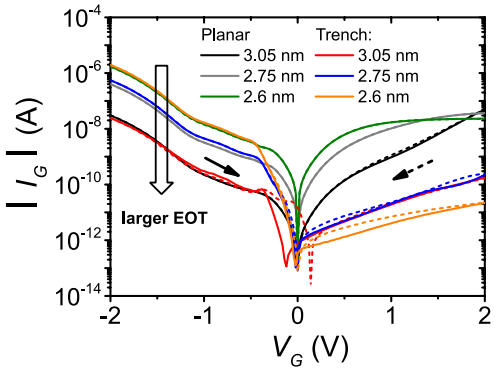

Fig. 2. Current–voltage (*I*–*V*) curves of planar and trench MIS with different EOTs and two voltage sweeping directions (solid: sweep forward, dash: sweep backward).

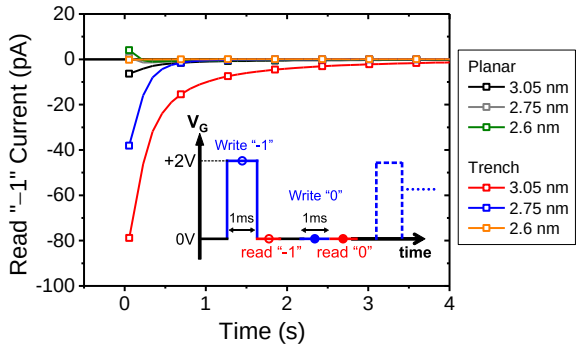

Fig. 3. Memory retention properties of planar and trench MIS. Inset shows the write voltage and read voltage settings used in the memory measurement. Since read "0" current curves of all MIS TDs are close to 0 A and independent of time, they are left out in this figure for simplicity.

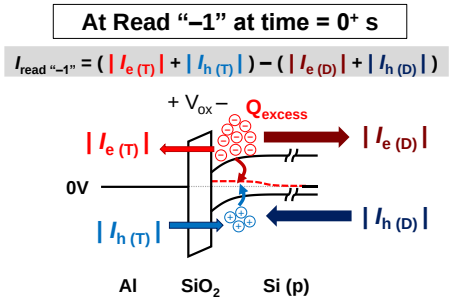

Fig. 4. Schematic band diagram that explains the origin of read "–1"transient current in MIS TDs. Arrows represent the flowing directions of carriers (electrons and holes).

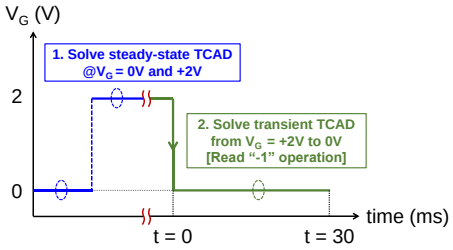

Fig. 5. TCAD simulation steps. After solving the steady-state solution at 0V and +2V, transient simulation switching from +2V to 0V is conducted, which emulates read "–1" operation.

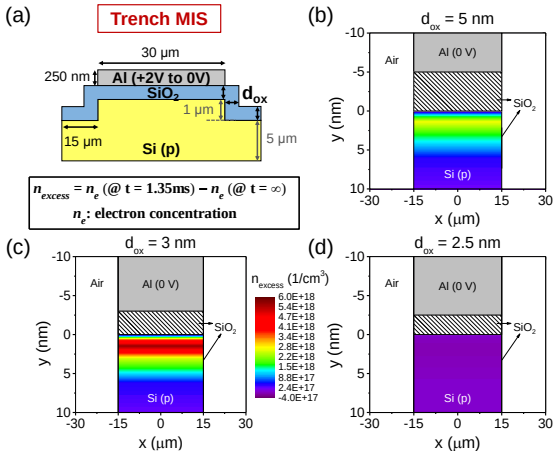

Fig. 6. (a) Schematic structure of trench MIS used in the TCAD simulation. Contour plots of excess electron concentration (n_{excess}) of trench MIS with (b) d_{ox} = 5 nm, (c) d_{ox} = 3 nm, and (d) d_{ox} = 2.5 nm under linear scale. n_{excess} is defined as the difference between n_e (@ t = 1.35 ms) and n_e (@ t = ∞), which is the steady-state n_e at V_G = 0 V.

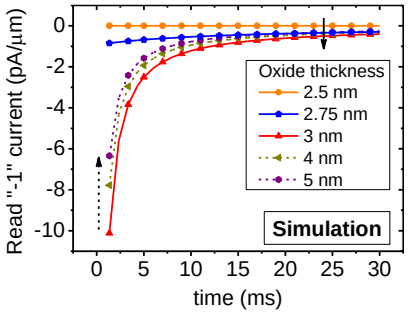

Fig. 7. Simulated retention results of trench MIS TDs with various d_{ox} under read "–1" operation.