IEDMS 2020

Enhanced Memory Properties in MIS TD by Forming Trench Structure at the Gate Edge

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NTUEE C-V LAB

Outline

- Introduction
  - Metal-Insulator-Semiconductor (MIS) Tunnel Diode (TD)
  - Memory Properties of MIS-TD
- Device Structure and Fabrication
- Results and Discussion
- Conclusion

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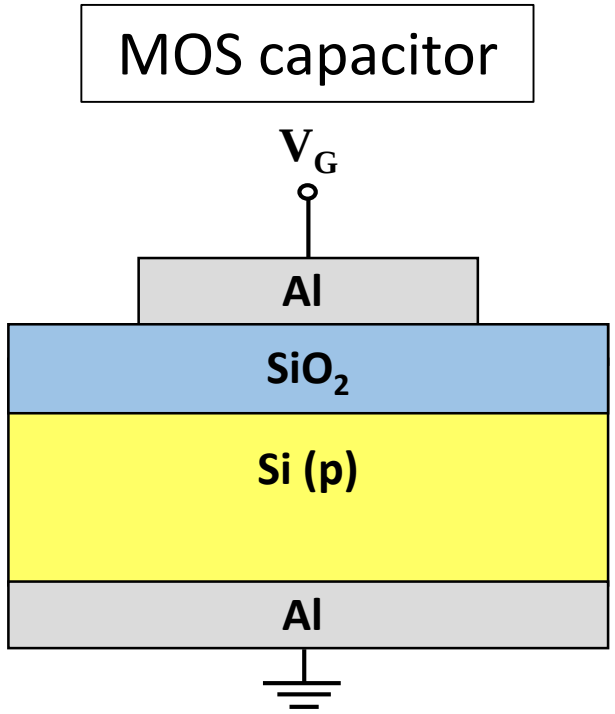
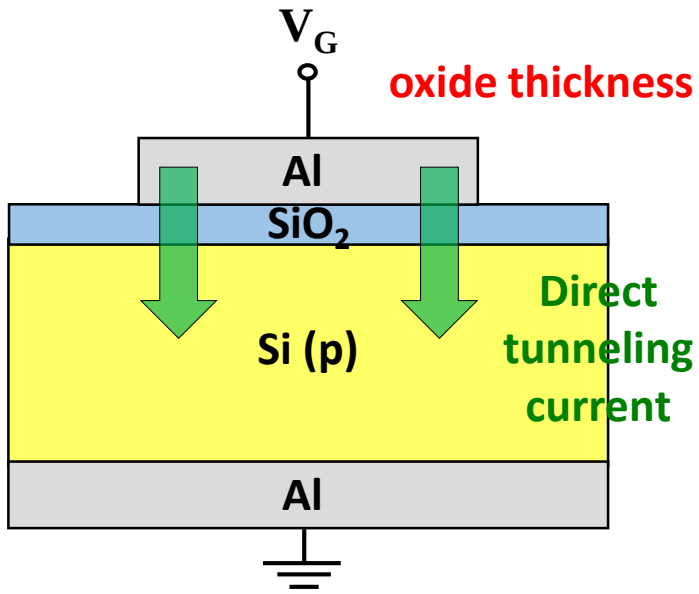
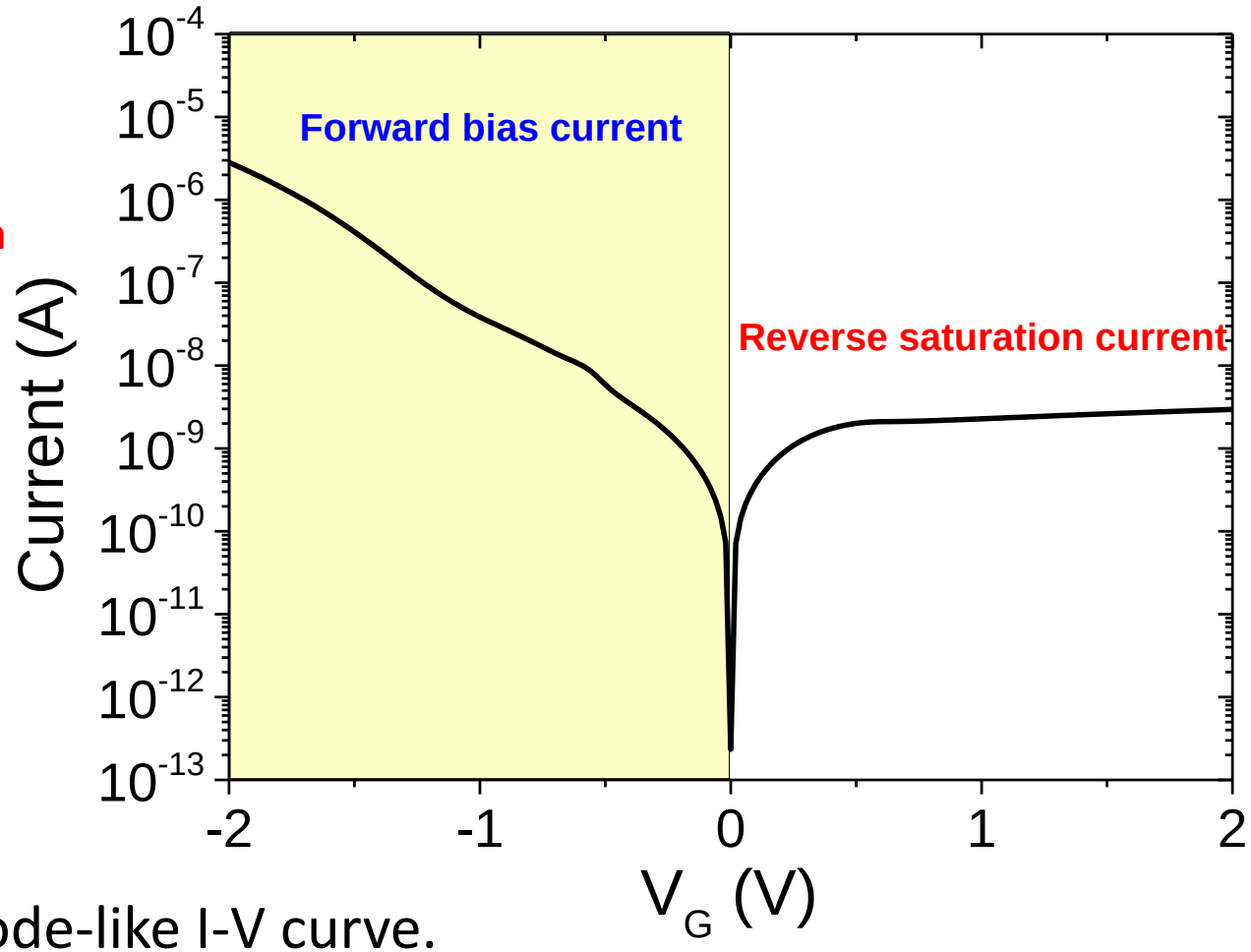
What is MIS Tunnel Diode?



What is MIS Tunnel Diode?

MIS tunnel diode (TD)

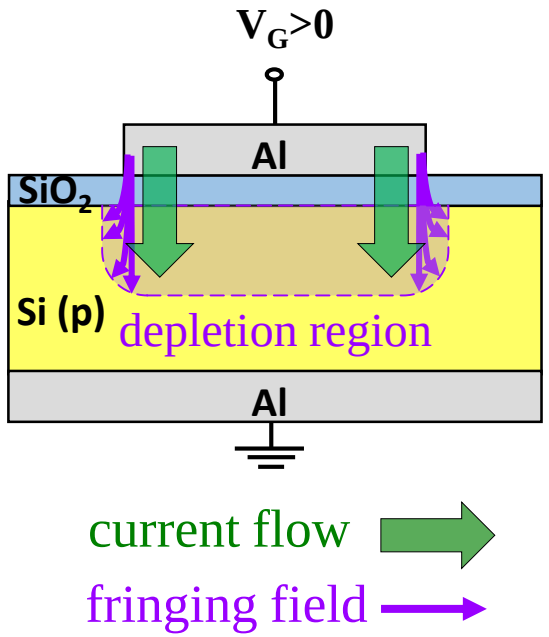


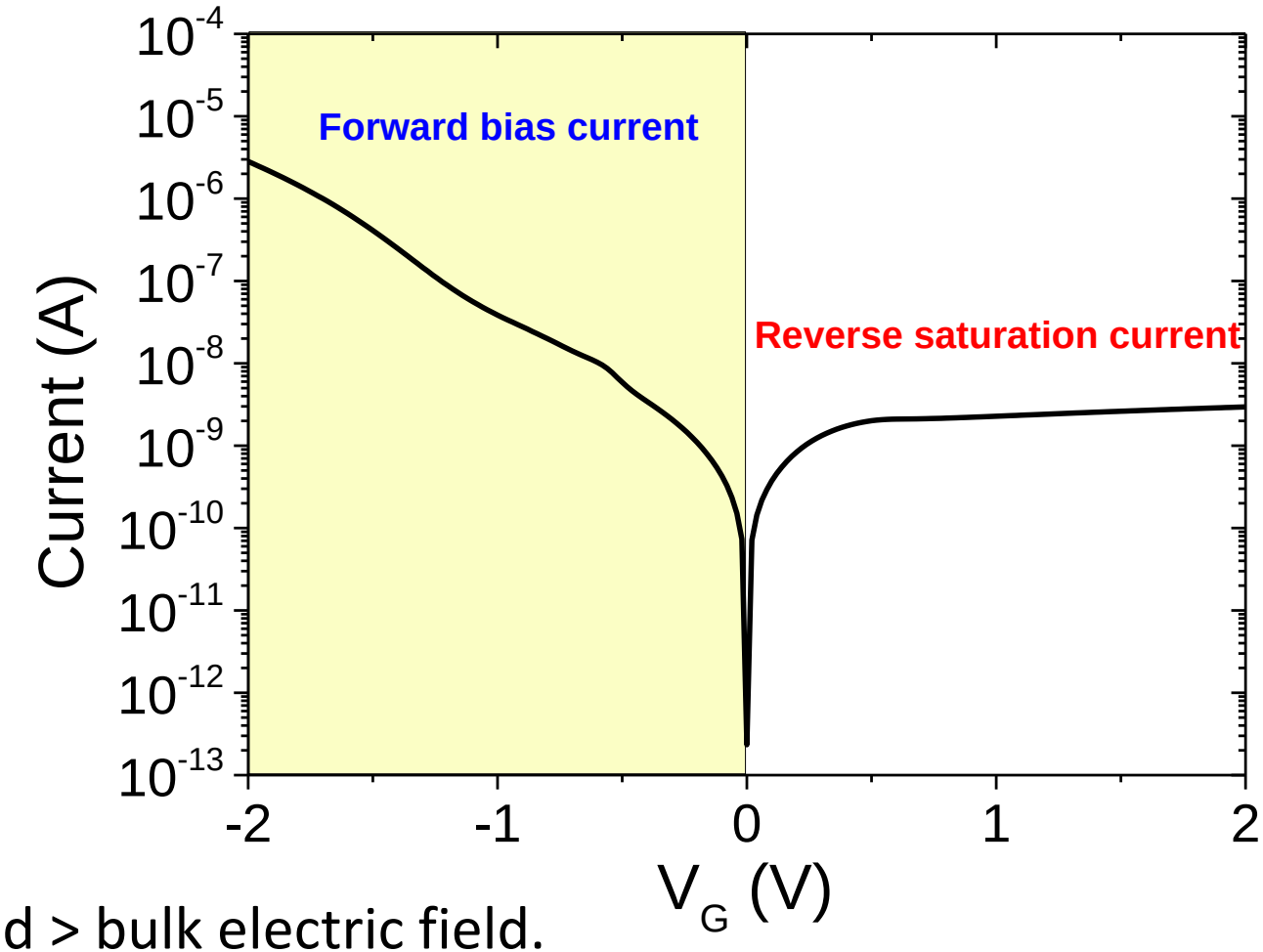


- Diode-like I-V curve.

MIS Tunnel Diode (Reverse Bias)

At reverse bias



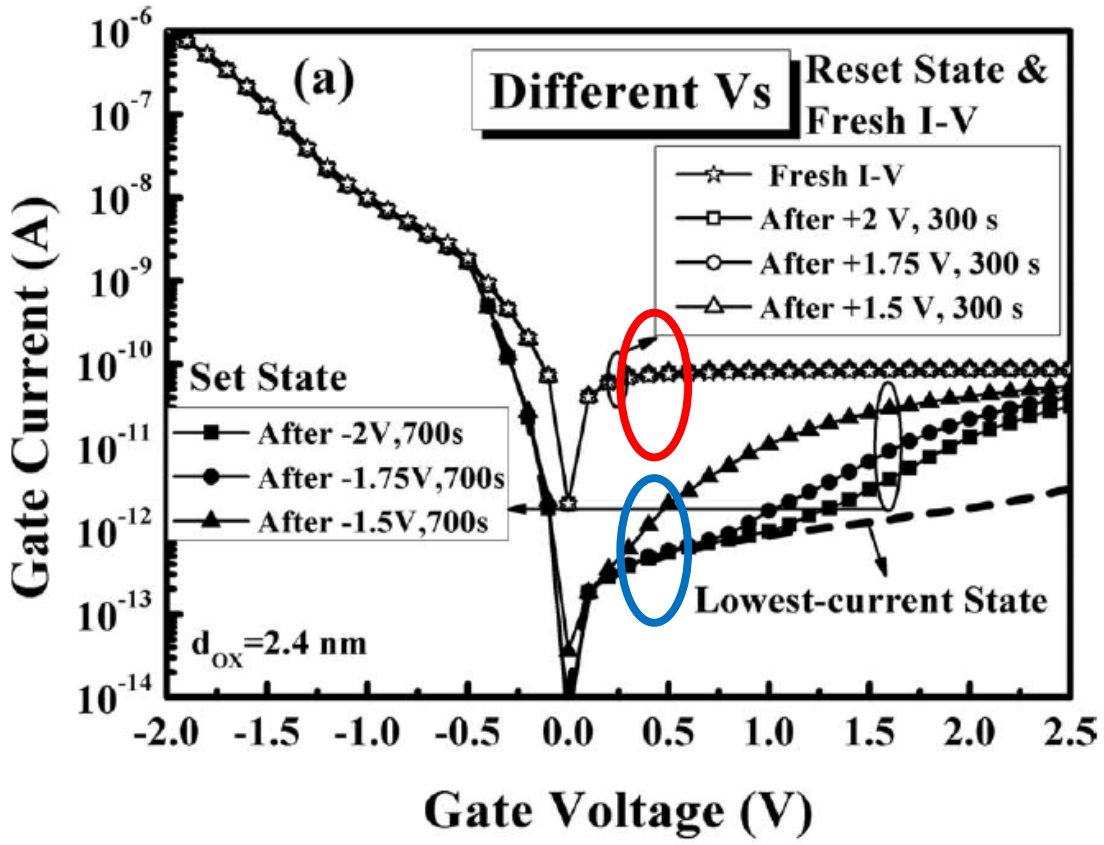


- Fringing electric field > bulk electric field.
- Saturation current mainly flow through gate edge.

Memory Properties of MIS-TD

- In previous work:
  - Apply negative and positive stress to MIS-TD.
  - Lower and higher current was measured.
  - 2-state current phenomenon.

Potential for memory device use.

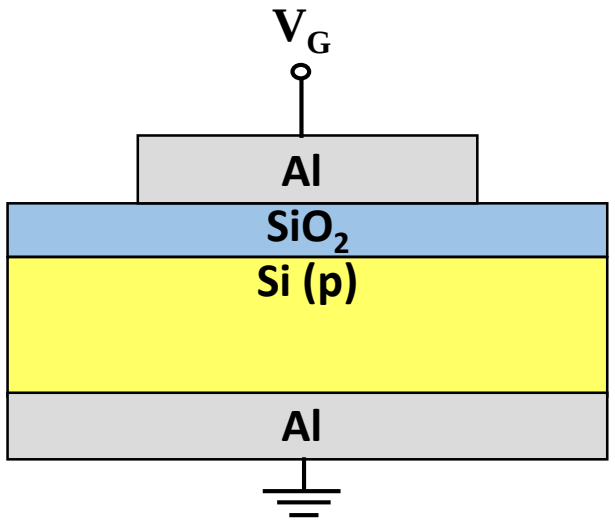


Reference: Tzu-Yu Chen *et al.*, "Effect of Electrons Trapping/De-Trapping at Si-SiO2 Interface on Two-State Current in MOS(p) Structure with Ultra-Thin SiO2 by Anodization," *ECS Journal of Solid State Science and Technology*, 2 (9) Q159-Q164, 2013. DOI: 10.1149/2.025309jss

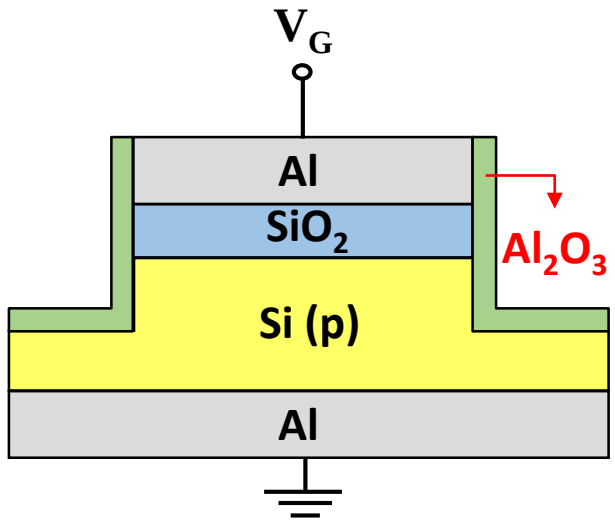
In this work…

- New structure of MIS-TD is proposed.

Conventional: Planar MIS

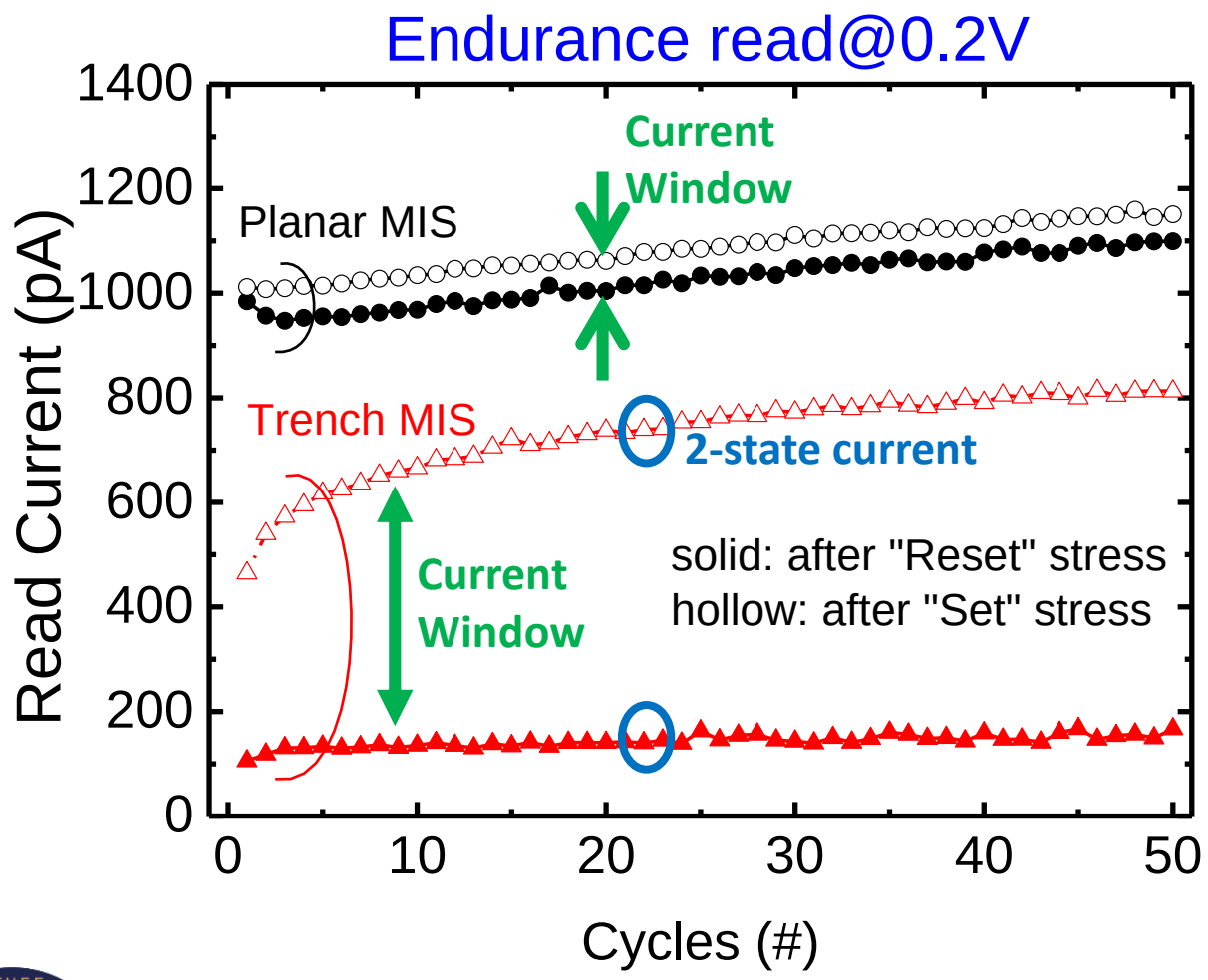


New Structure: Trench MIS



➢ **better memory properties.**

In this work…



Reset: -1.75V for 20s
Set: +1V for 10s

- Trench MIS TDs have **better memory properties**.
  - more **obvious 2-state current.**
  - 10 times **larger current window.**

Current Window (CW)=
read current (after “Set”, open)-
read current (after “Reset”, solid)

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- Results and Discussion
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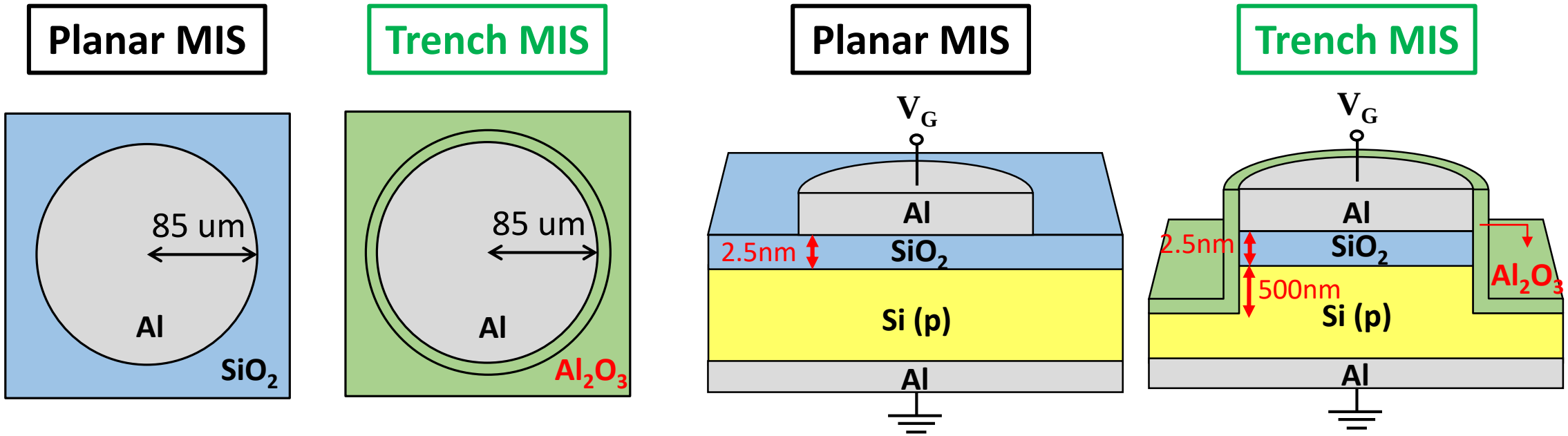
Device Structure and Fabrication

Top view

Cross section



Effective oxide thickness (EOT)=2.5 nm

Device Structure and Fabrication

Radio Corporation of America (RCA) clean

Si (p)

p-type (100)-oriented silicon wafers with a resistivity of 1–10 Ω·cm

Device Structure and Fabrication

- Radio Corporation of America (RCA) clean
- Grow SiO_2 by anodic oxidation

Device Structure and Fabrication

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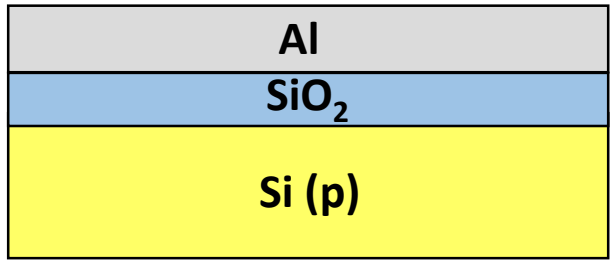
- Grow SiO_2 by anodic oxidation
- Rapid thermal annealing (RTA) in N_2 ambient @ 950 °C for 15 s.

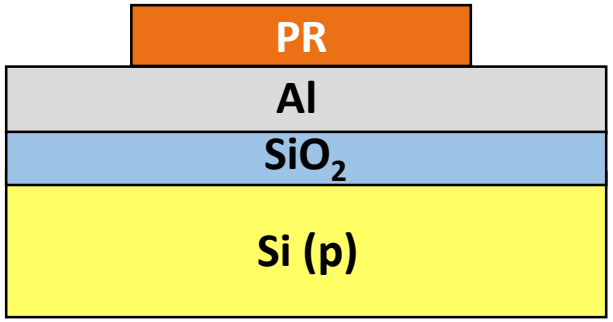
Device Structure and Fabrication



- Radio Corporation of America (RCA) clean
- Grow SiO_2 by anodic oxidation
- Rapid thermal annealing (RTA) in N_2 ambient @ 950 °C for 15 s.
- Deposit 200 nm Al by thermal evaporation

Device Structure and Fabrication

Circle structure patterned by photolithography



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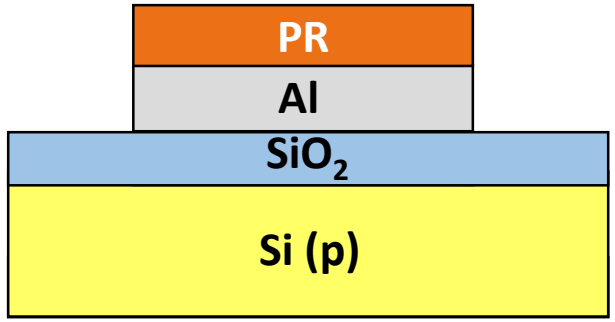
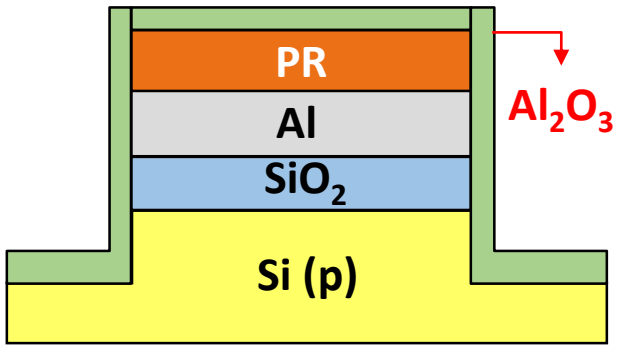


- Circle structure patterned by photolithography
- Etch Si substrate by reactive ion etch (RIE)

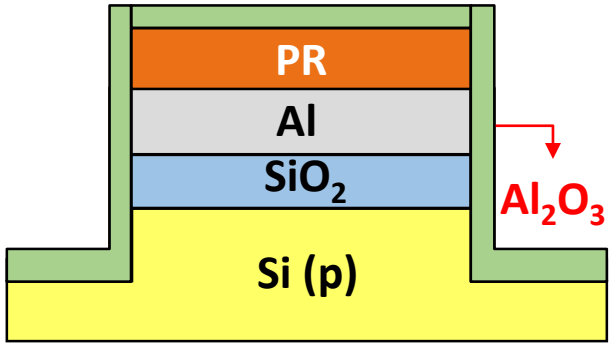
Device Structure and Fabrication



Al_2O_3 layer:
protect Si substrate from being exposed to air.

- Circle structure patterned by photolithography
- Etch Si substrate by reactive ion etch (RIE)
- Form a layer of Al_2O_3 : (1) thermal evaporate Al. (2) dip into nitric acid (HNO_3) to oxidize Al.

Device Structure and Fabrication



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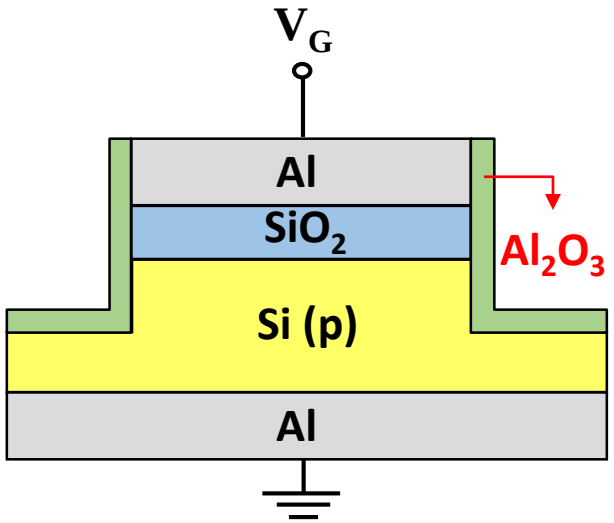
- Lift-off PR

Device Structure and Fabrication



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protect Si substrate from being exposed to air.

- Circle structure patterned by photolithography
- Etch Si substrate by reactive ion etch (RIE)
- Form a layer of Al_2O_3 : (1) thermal evaporate Al. (2) dip into nitric acid (HNO_3) to oxidize Al.
- Lift-off PR
- removed backside native oxide by buffer oxide etchant (BOE)
- 200nm Al formed as back electrode by thermal evaporation

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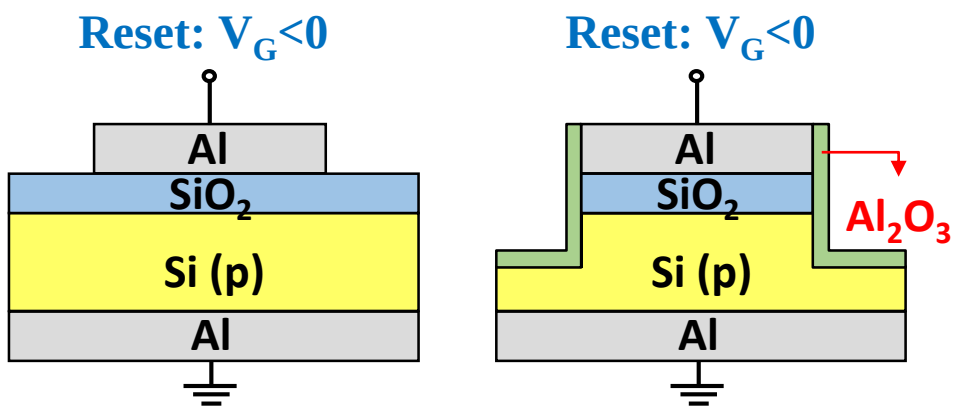
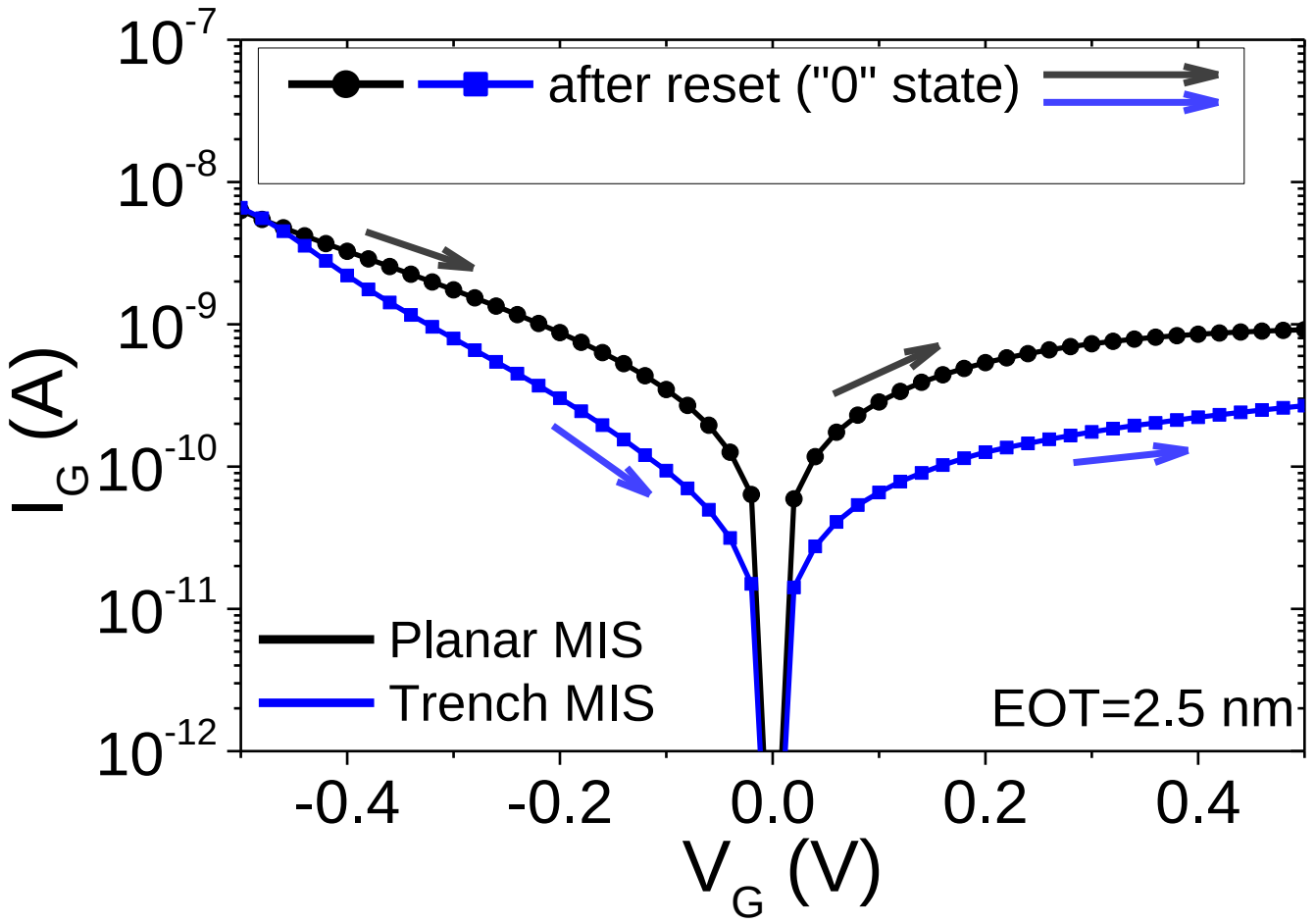
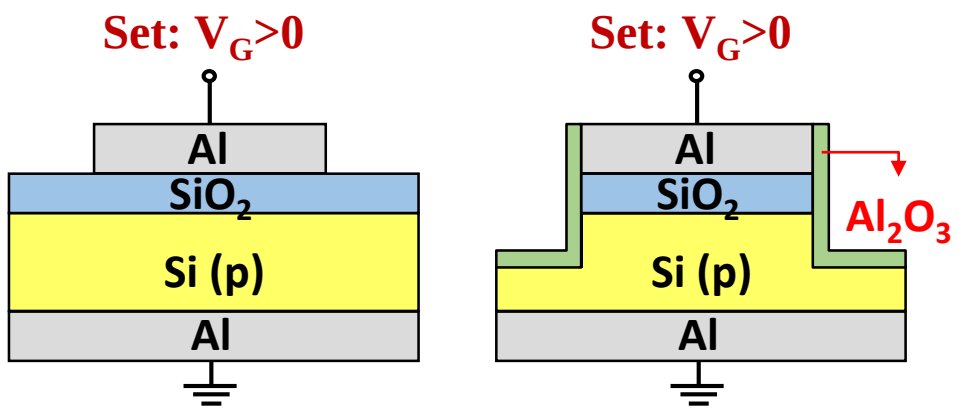
I-V Curves: After Reset Stress



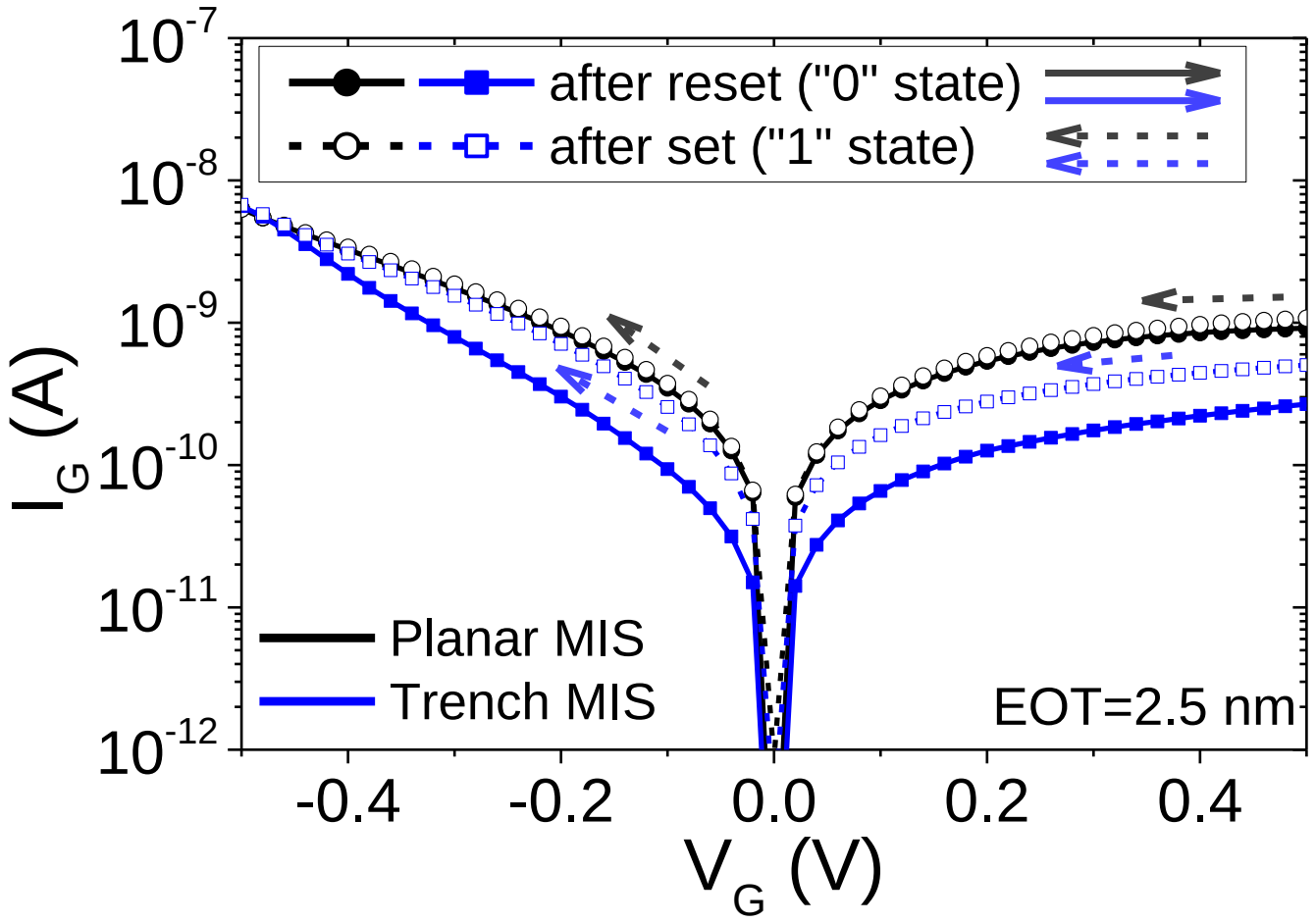
1. Apply -1.5V for 120s and then -1.75V for 20s to gate as **"Reset" stress**.
2. Measure I-V from **-0.5V~0.5V (solid symbol)**.



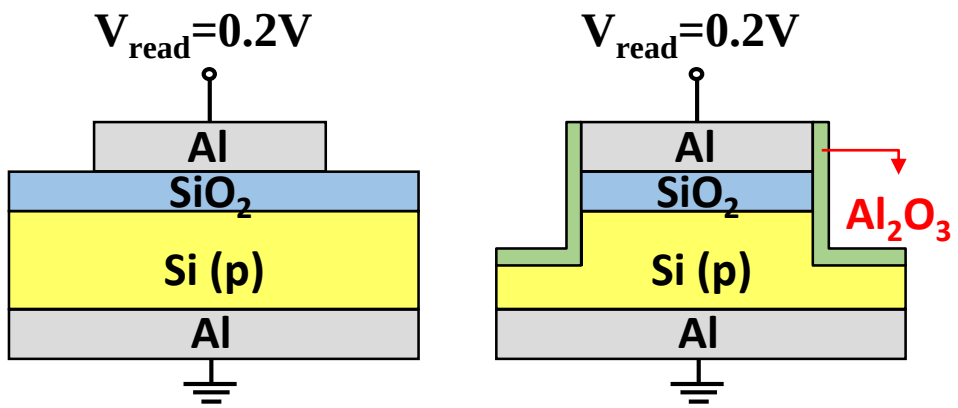
I-V Curves: After Set Stress



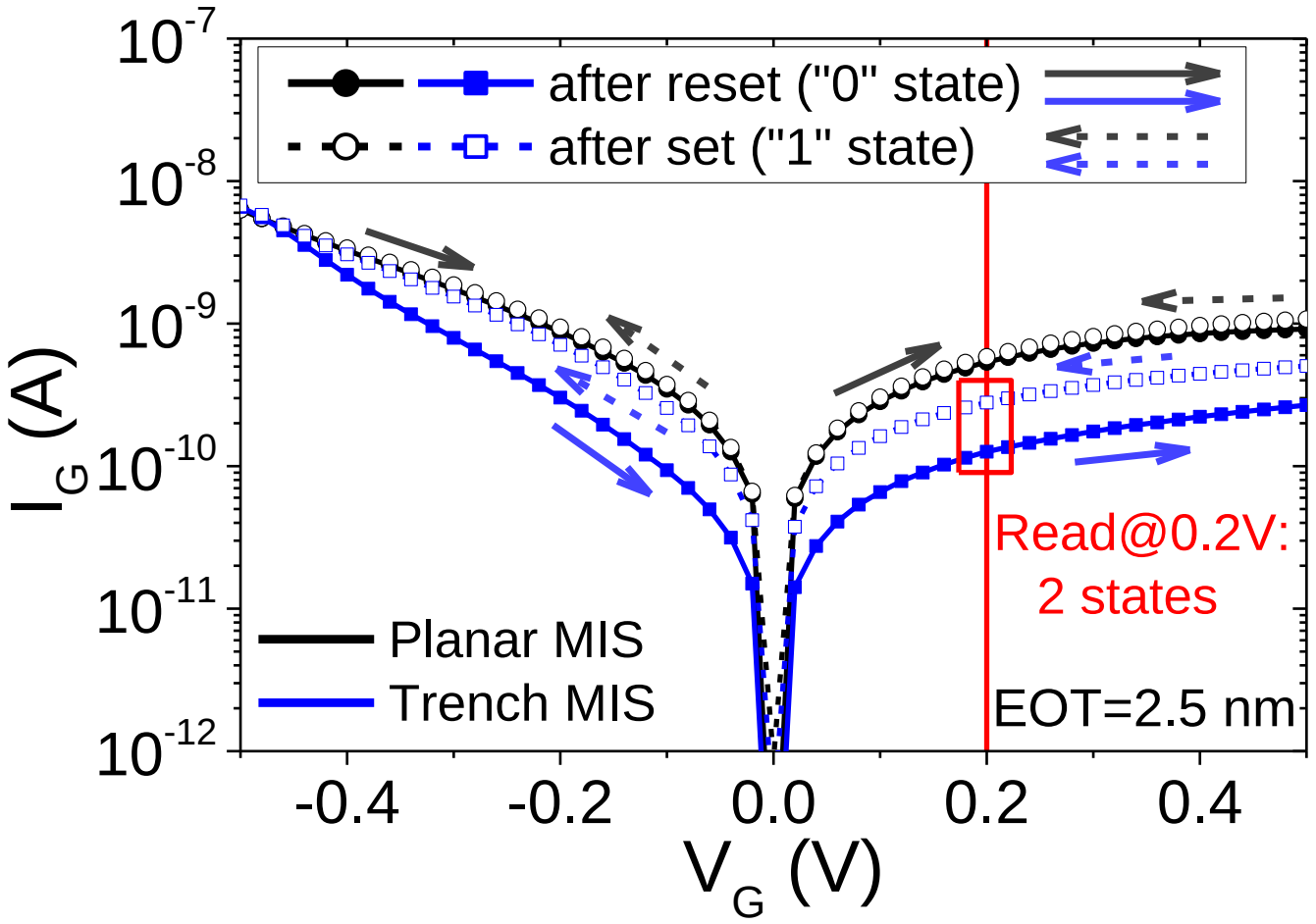
3. Apply +1V for 20s to gate as **"Set" stress**.
4. Measure I-V from **+0.5V~-0.5V (open symbol)**.



I-V Curves: 2-state Current



- Trench MIS has a more obvious 2- state current phenomenon.



Memory Endurance Measurement

1st Endurance

- 1. reset (“0”): -1.75V, 20s → read @ 0.2V
- 2. **set (“3”): +1V, 10s** → read @ 0.2V
- 3. repeat 1.~2. for 50 cycles.

2nd Endurance

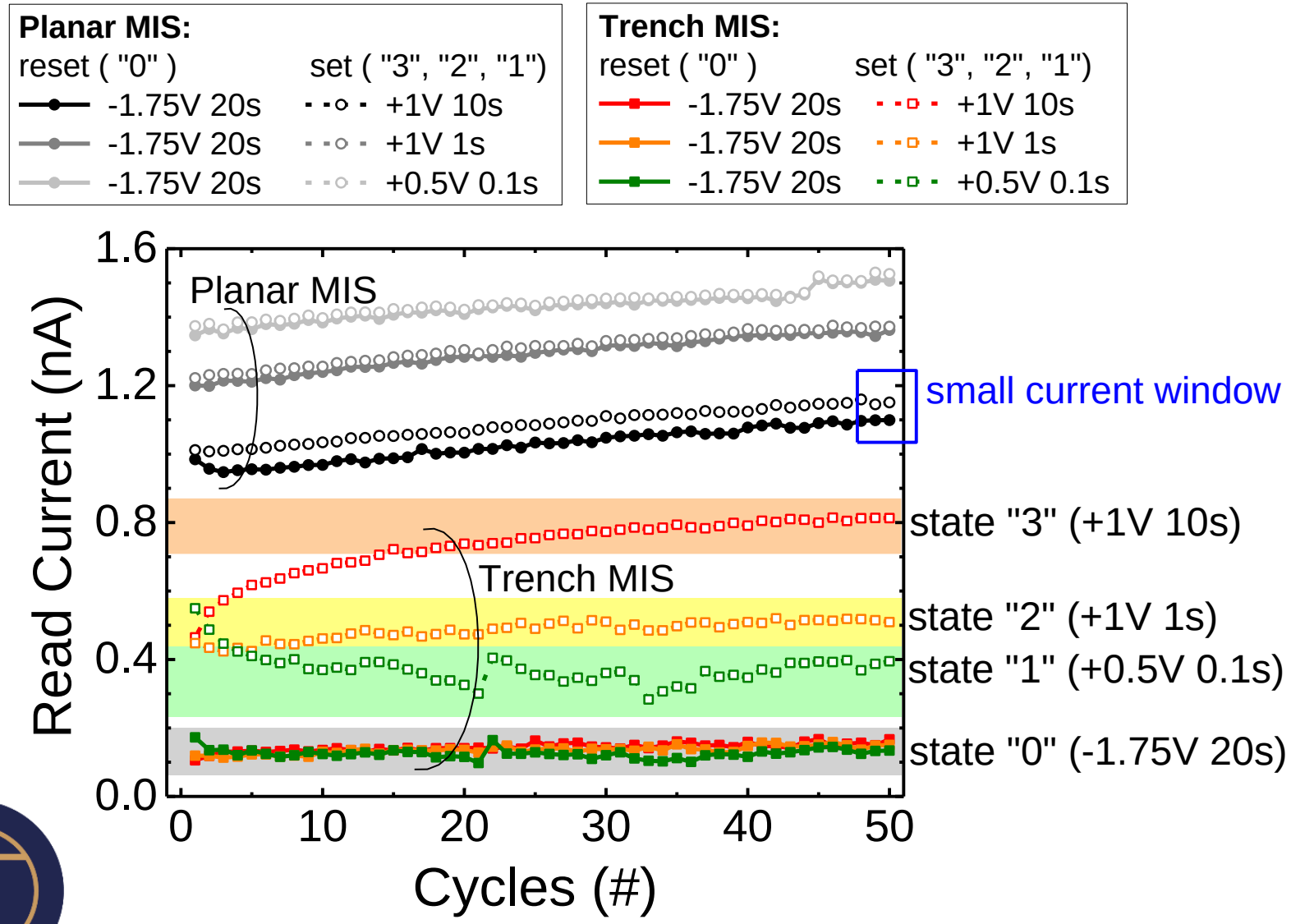
- 1. reset (“0”): -1.75V, 20s → read @ 0.2V
- 2. **set (“2”): +1V, 1s** → read @ 0.2V
- 3. repeat 1.~2. for 50 cycles.

3rd Endurance

- 1. reset (“0”): -1.75V, 20s → read @ 0.2V
- 2. **set (“1”): +0.5V, 0.1s** → read @ 0.2V
- 3. repeat 1.~2. for 50 cycles.

- 3 endurance measurements with different “set stress”.
- same reset stress.
- read @V_G=0.2V
- each 50 cycles.

Memory Endurance Results

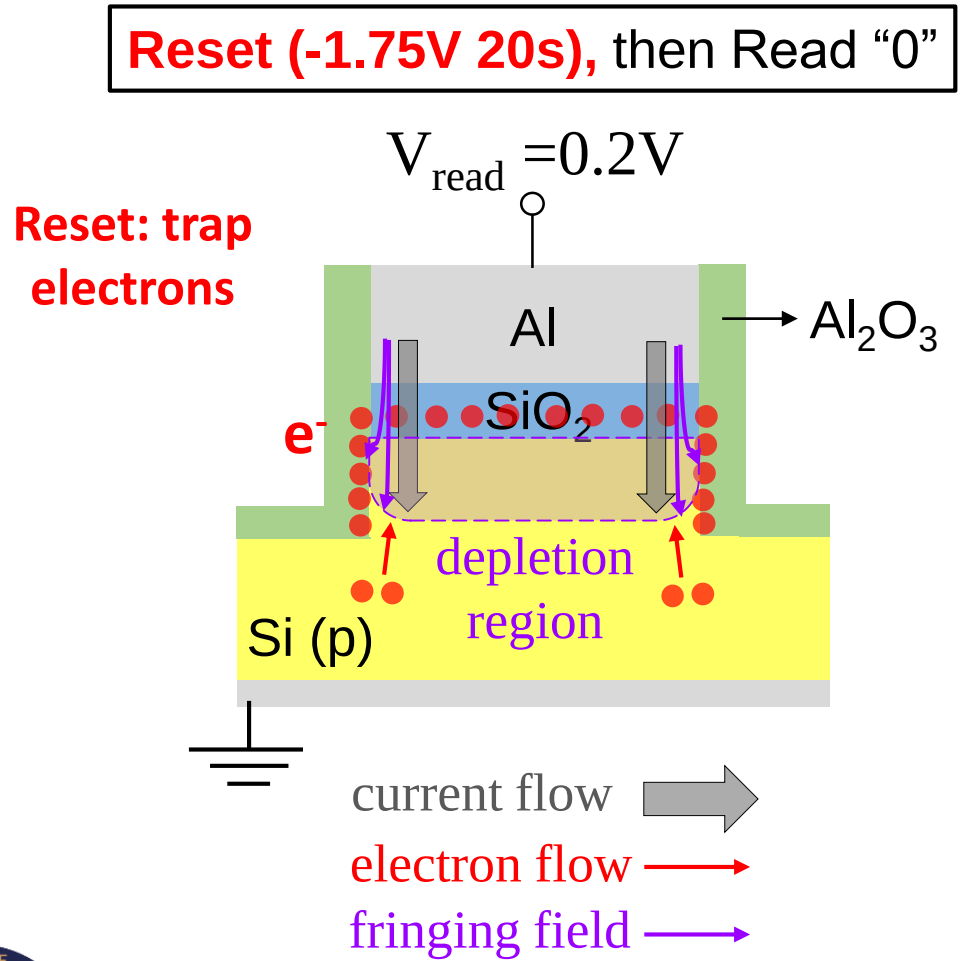


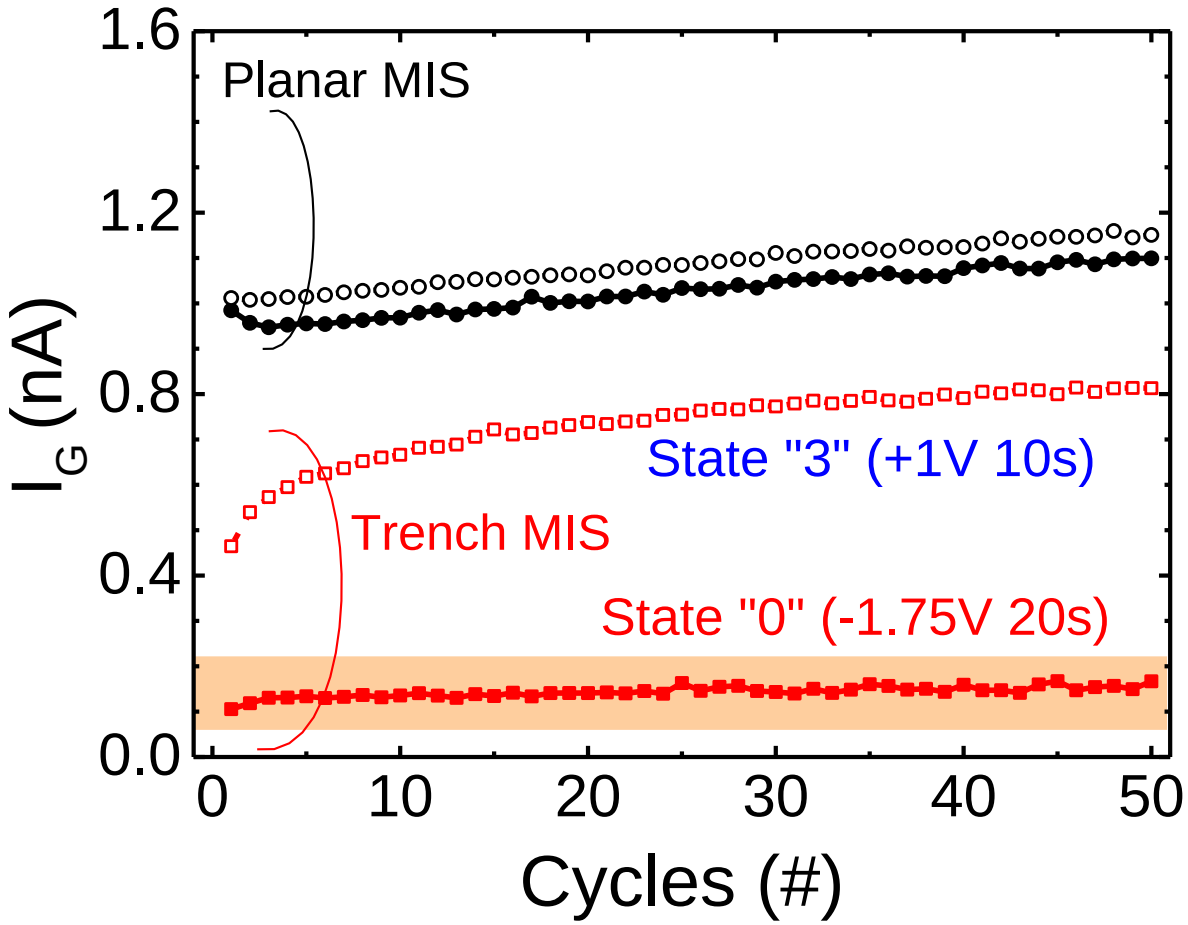
- Reset (solid), Set (open).
- Trench MIS:
  - stabler multi-level memory function.
  - larger current window.

Current Window=
read current (after “Set”, open)-
read current (after “Reset”, solid)

Electron Traps Mechanism: Reset

Reset (-1.75V 20s), then Read "0"



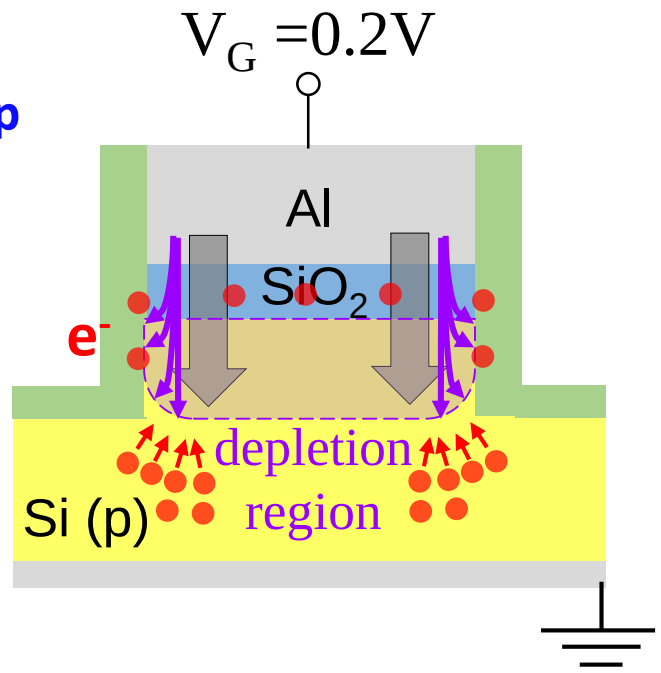


Electrons trap in Al_2O_3/SiO_2 interface and SiO_2 layer.

Electron Traps Mechanism: Set

Set (+1V 10s), then Read "3"

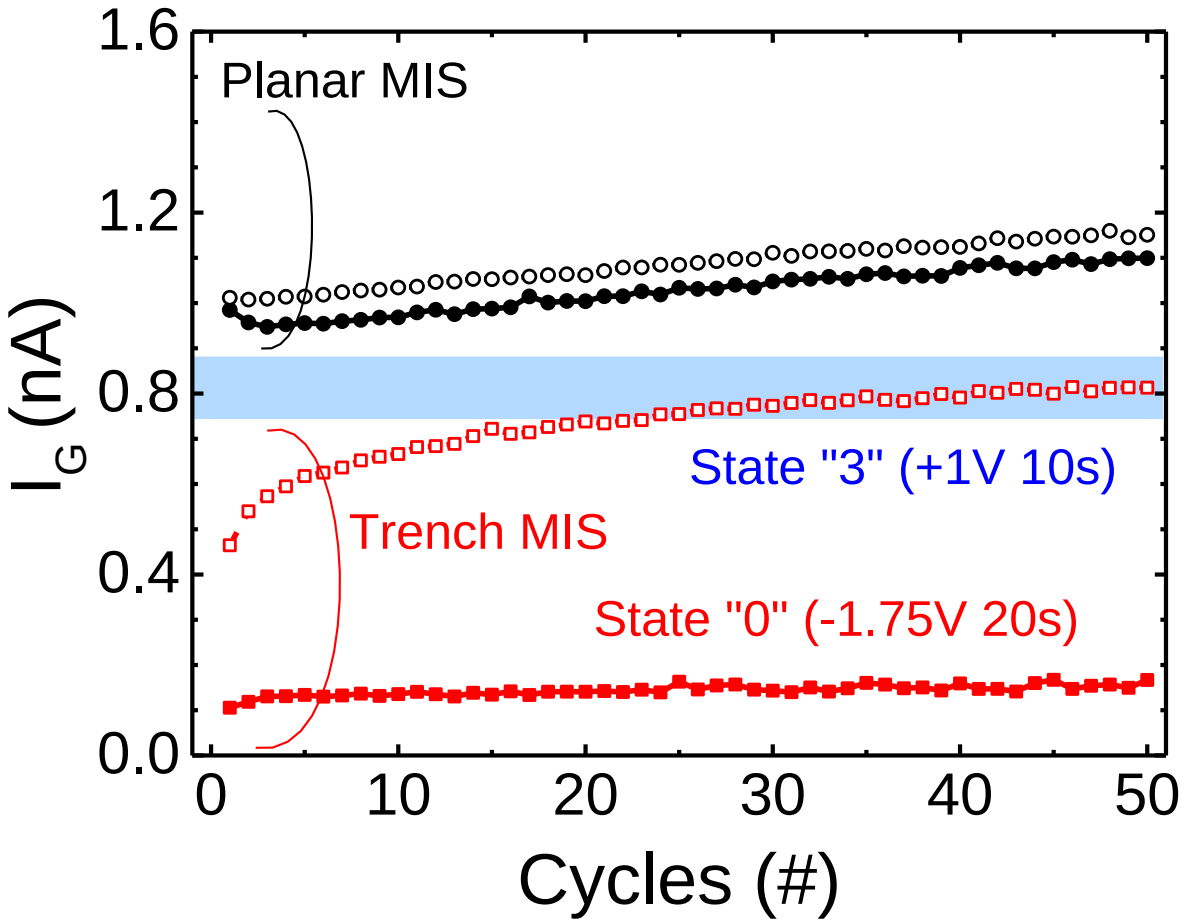
Set: detrap electrons



current flow

electron flow

fringing field



◆Trench structure offers extra electron traps.

➢ Better memory properties.

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Conclusion

- In this work, a new structure of MIS TD, trench MIS TD, is proposed.
- Trench MIS TDs have better memory properties than planar MIS TD.
- Electron trap mechanism : more electron traps offered by trench structure.
  - However, we still need more study to verify this mechanism.

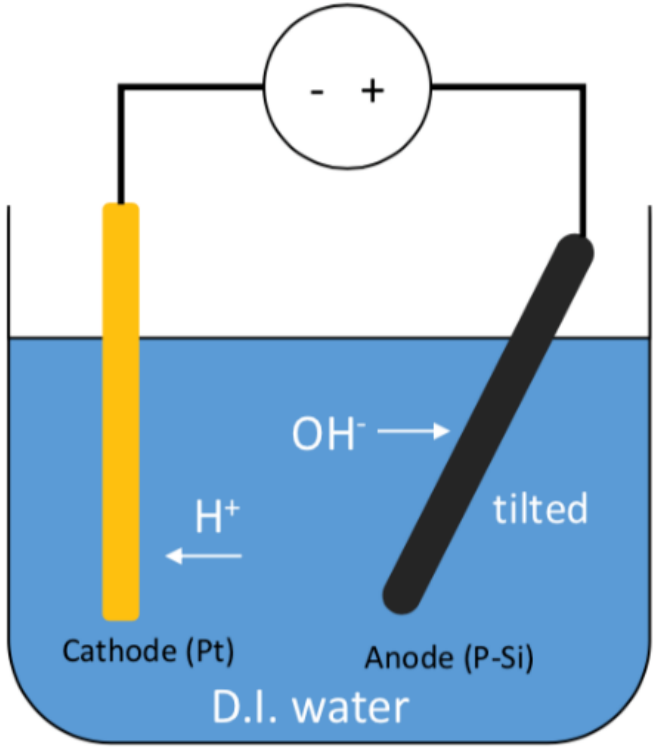
Thank you for listening !

Q&A

Anodic Oxidation (ANO)

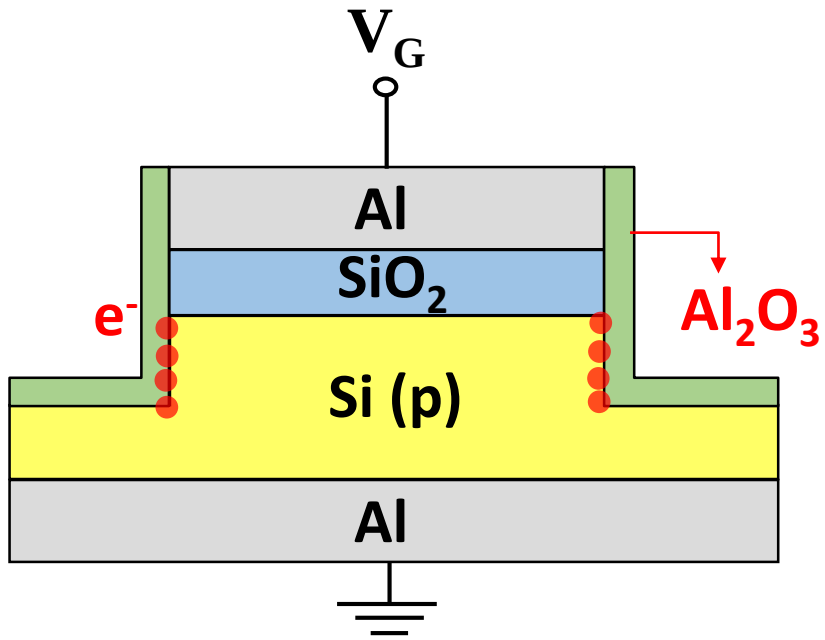
- Can be performed in room temperature, then RTA.
- Uniform oxide layer.

$$Si^{2+} + 2e^{-} + 2H_2O \rightarrow SiO_2 + 2H_2$$



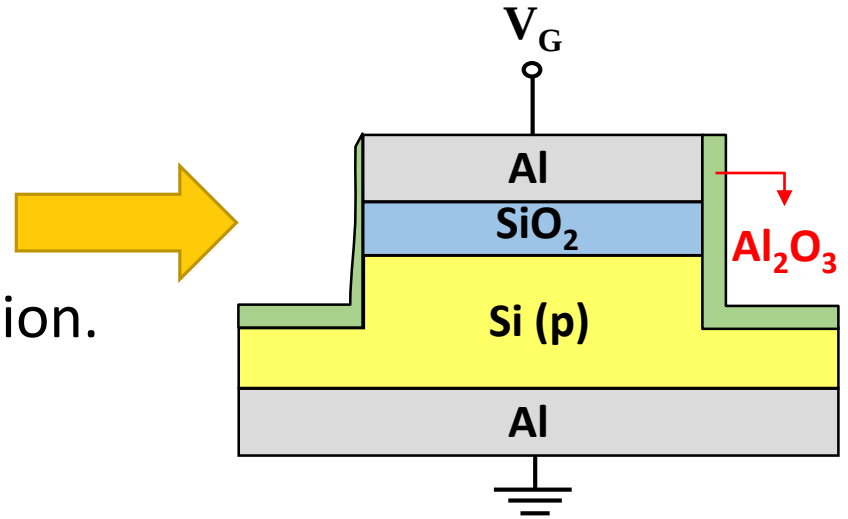
Functions of Al_2O_3 Layer

- Functions of this layer:
  1. protect Si substrate from moisture and air.
  2. provide electron traps in Al_2O_3/Si interface.

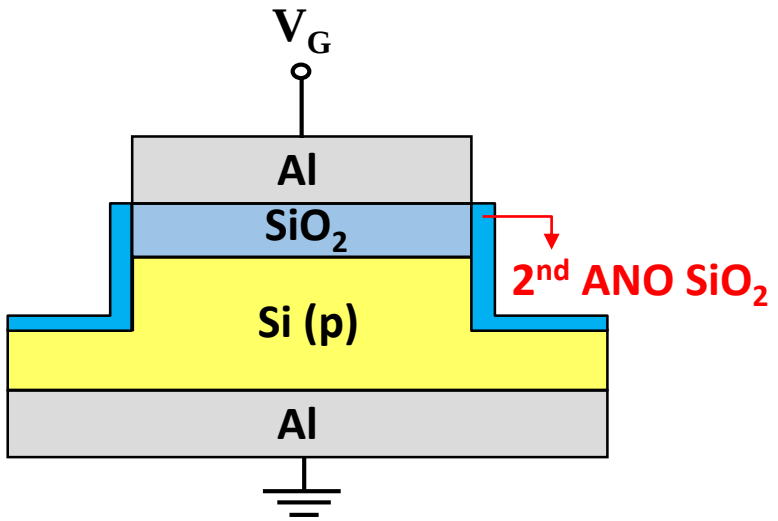


Uniformity of Al_2O_3 layer

- Evaporated Al oxidized by nitric acid.
- The Al_2O_3 layer is non-uniform:
  - may influence the moisture and air protection.



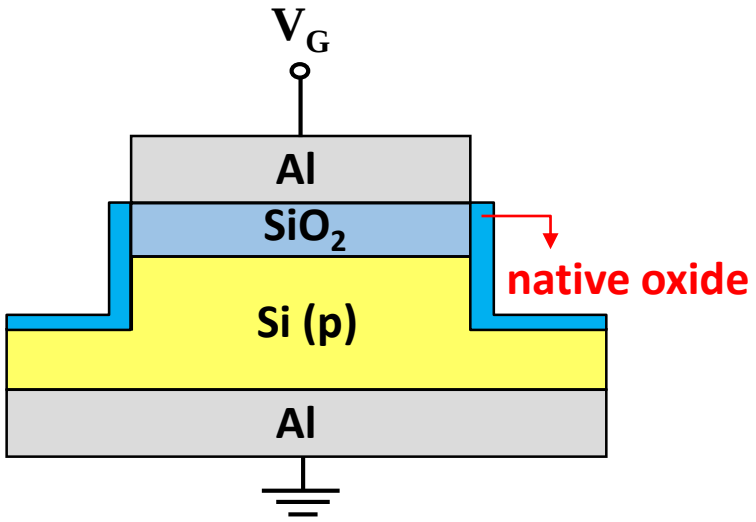
- Solutions (different ways to form sidewall):
  a) Al_2O_3 sidewall: by sputter Al target in Ar/O_2 ambient.
  b) SiO_2 sidewall: by anodic oxidation.



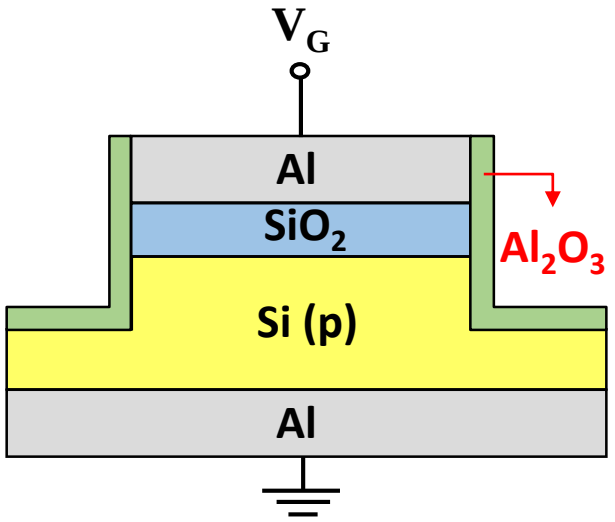
Quality of Al_2O_3 Layer

- Purpose of this layer: protect Si substrate from moisture and air.

Prototype trench MIS (native oxide)



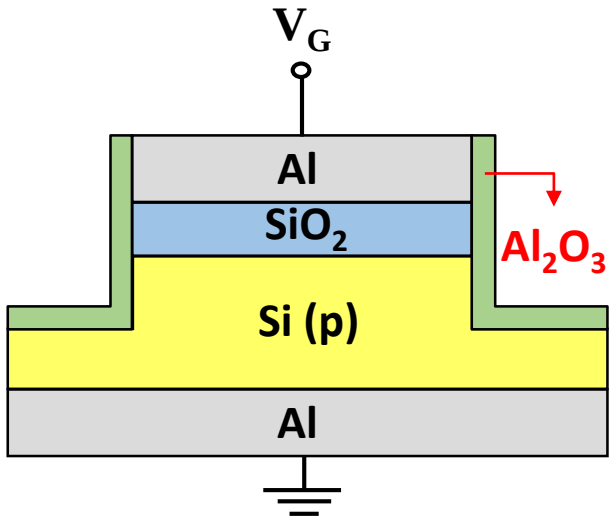
trench MIS in this work



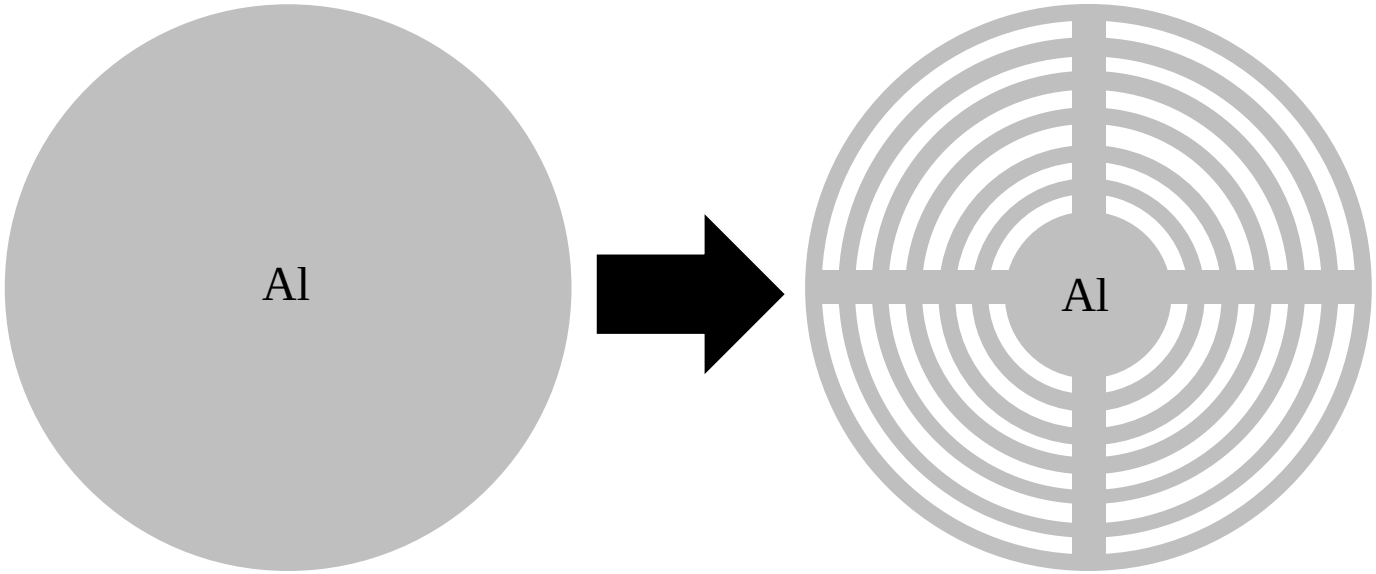
- Current window **easily degrades**.
- might because the instability of native oxide.

- Current window is more stable.
- Acceptable quality of Al_2O_3 Layer.
- but can be improved.

Further Verification of the Mechanism



Top view:



- Trench structure offers electron traps at gate edge
  - More edge (by different mask pattern design).
  - Better current window.

Improvement of Stress Time

◆Currently, the “Reset” and “Set” stress time is still too long (>1s)

◆Possible ways to improve:

① increase the edge of the pattern under the same footprint.

② increase the depth of the trench structure.

∵ more edge or more trench → more electron traps.