Enhanced Transient Behavior in MIS(p) Tunnel Diodes by Trench Forming at the Gate Edge

Jian-Yu Lin and Jenn-Gwo Hwu, *Senior Member, IEEE*

***Abstract*— In this article, a new type of metal–insulator–semiconductor (MIS) tunnel diode (TD), trench MIS TD, was investigated. From the current–voltage characteristics, memory retention, and memory endurance measurements, we found that the trench MIS TDs not only have lower reverse bias current, but also show stronger transient current compared to traditional planar structure MIS TDs. For example, in the 1000-cycle memory endurance test, we observed a 25 times larger current window (CW) in trench devices than the CW of planar devices. We attribute the lower reverse bias current to the fewer minority carriers (electrons) in trench MIS TDs, which is supported by the high-frequency capacitance–voltage (*C–V*) measurement. As for the enhanced transient behavior of trench MIS TDs, we proposed a mechanism based on the understanding of fewer minority carriers in trench devices to explain our observation. Eventually, we examined the effect of different equivalent oxide thicknesses (EOTs) on the CW and found that the trench devices have better CW in a wide EOT range. Because of the enhanced transient behavior leading to better memory CW, trench MIS TDs have the potential to serve as memory devices.**

***Index Terms*— Metal–insulator–semiconductor (MIS), transient behavior, trench structure, tunnel diode (TD).**

I. Introduction

TRANSIENT behavior is an important property in electronic devices since it represents the potential for memory applications. For example, traditional one transistor and one capacitor (1T–1C) dynamic random access memory (DRAM) uses the capacitor to store charges, and the memory states can be read by the voltage transient behavior caused by the charges stored in the capacitor. Besides 1T–1C DRAM, capacitor-less DRAM or 1T-DRAM, which have attracted great attention in recent years for its smaller cell size [1], also exploit current transient behavior of the 1T-DRAM to store memory states [2], [3]. Although metal–insulator–semiconductor (MIS) tunnel diodes (TDs) have been studied by many research groups before [4]–[6], special current transient behavior has been observed in MIS TDs with unconventional structures in recent research [7], [8]. To be more specific, compared to traditional planar structure MIS TDs (planar MIS TDs), by thinning down a partial portion of the gate metal thickness [7] or thickening the oxide at the gate edge [8], the transient behavior of the altered structure MIS TDs can be largely enhanced. However, all the above special structures need two mask fabrication processes, which increases the fabrication cost and the process complexity.

In this work, we comprehensively investigate the electrical characteristics of MIS TDs with a new structure, trench structure MIS TDs (trench MIS TDs), which only need one mask process to fabricate. By using planar MIS TDs as comparisons, we find the trench MIS TDs not only have reduced reverse bias current, but also show enhanced transient current behavior. We suggest that this large difference in electrical properties is attributed to the fewer minority carriers (electrons) in the trench devices. In addition, by applying memory retention and endurance measurements, we are able to investigate the enhanced transient behavior in more detail and moreover demonstrate that this transient current can be harnessed to store two different memory states. With the advantages of low power consumption, CMOS-compatible process, and low fabrication cost, the proposed trench MIS TD may find its use in memory applications.

II. Experimental

Boron-doped p-type (100)-oriented silicon wafers with a resistivity of 1–10 Ω·cm were used as the substrate. After standard Radio Cooperation of America (RCA) cleaning process, we used anodic oxidation (ANO) to grow a layer of SiO_2 in deionized water under room temperature. Rapid thermal annealing (RTA) was then performed under a 20-torr N_2 ambient at 950 °C for 15 s. Next, a layer of 250-nm-thick aluminum metal was thermally evaporated and patterned by photolithography and wet etching, which forms the metal gates of MIS TDs. It should be noted that after the wet etching process, the photoresist (PR) on the aluminum layer was kept for the following process.

By using this PR layer as a soft mask, we employed reactive ion etching (RIE) to etch the Si substrate outside the metal gate and formed a trench structure at the gate edge. Since the etched Si substrate was exposed to the air after the RIE process, we deposited a layer of Al_2O_3 by *in situ*

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Jian-Yu Lin is with the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 10617, Taiwan (e-mail: r08943076@ntu.edu.tw).

Jenn-Gwo Hwu is with the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 10617, Taiwan, and also with the Department of Electrical Engineering, National Taiwan University, Taipei 10617, Taiwan (e-mail: jghwu@ntu.edu.tw).

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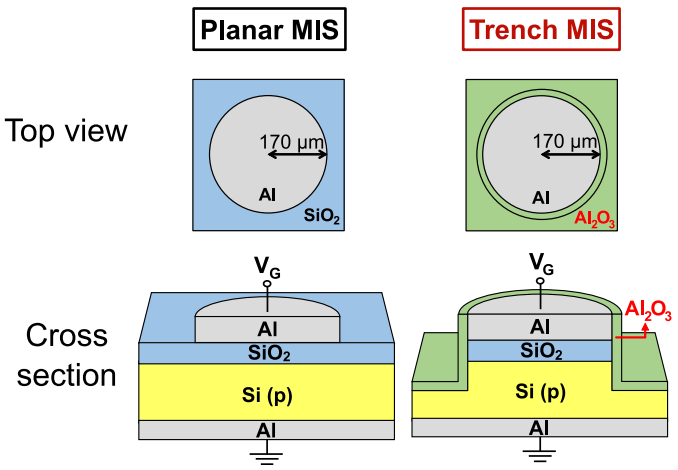

Fig. 1. Top views and schematic cross section views of traditional planar MIS TDs and the proposed trench structure MIS TDs. The top Al metal gates were all patterned as the circle shape with a radius of 170 μm.

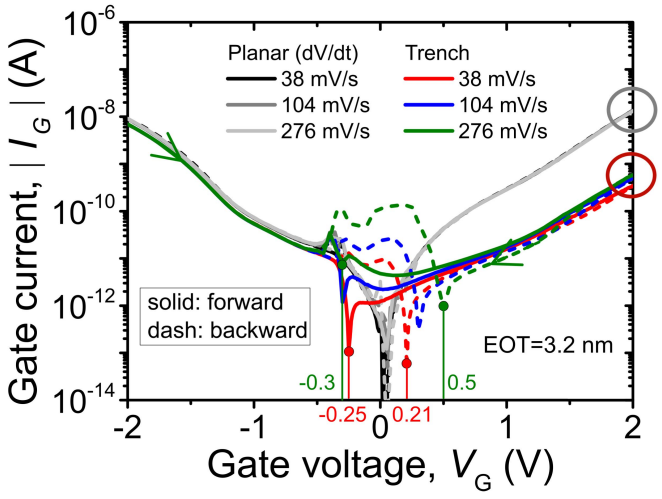

Fig. 2. *I–V* characteristics of the planar and the trench MIS TDs with two voltage sweeping directions and different voltage sweeping rates (d*V*/d*t*). At $V_G > 0$ V, MIS TDs are in the reverse bias region. At $V_G < 0$ V, MIS TDs are in the forward bias region. Voltage sweeps forward (solid line). Voltage sweeps backward (dashed line).

oxidation of dc sputtering to prevent it from the degradation caused by moisture in the air. In the dc sputtering process, we sputtered Al targets in a mixed Ar/O_2 ambient with a ratio of 1:3 at 2.5×10^{-2} torr. The details of the *in situ* oxidation sputtering and the reliability analysis of the sputtered films were illustrated and discussed elsewhere [9], [10]. After depositing Al_2O_3, PR was removed by the lift-off process. Furnace annealing at 200 °C for 10 min in N_2 ambient was then used to improve the quality of Al_2O_3. Finally, the 200-nm-thick aluminum layer was deposited by thermal evaporation as the back electrode after removing the backside native oxide by buffered oxide etchant. The above-mentioned process finished the fabrication of trench structure MIS TDs (trench MIS TDs).

Another group of devices, traditional planar structure MIS TDs (planar MIS TDs), were also fabricated to use as control groups. The difference between the process of trench MIS TDs and planar MIS TDs is that there were no RIE Si etching, Al_2O_3 deposition, and furnace annealing in the process of planar MIS TDs. Schematic structures of the planar and trench MIS TDs are shown in Fig. 1. Electrical characteristics of the devices were measured by Agilent B1500A semiconductor device analyzer at room temperature. As for the equivalent oxide thickness (EOT) of our devices, it was extracted by fitting the two-frequency corrected capacitance–voltage (*C–V*) curves [11], which were extracted by *C–V* curves of 100 and 10 kHz, under consideration of quantum mechanical effect [12]. Note that the EOT of our devices ranges from 2.45 to 3.25 nm.

III. Results and Discussion

Fig. 2 shows the current–voltage (*I–V*) characteristics of the planar and trench devices with voltage sweeping forward, backward, and different sweeping rates. Compared to planar MIS TDs, there are two major differences in the *I–V* curves of trench MIS TDs.

1) The lower reverse bias steady-state current at the large gate voltage (e.g., at $V_G = +2$ V).
2) The enhanced transient displacement current, which can be observed from the larger hysteresis in Fig. 2 at the low voltage region.

In the following, we will first discuss the lower reverse bias steady-state current of trench devices in Section III-A since it gives us an insight into the basic steady-state current difference between the planar and trench MIS TDs. Based on this discussion, we will then investigate the reason behind the enhanced transient displacement current of trench devices in Section III-B.

A. Lower Reverse Bias Steady-State Current at the Large Gate Voltage in Trench MIS TDs

Compared to the planar device, the trench device shows a smaller reverse bias current at +2 V [see Fig. 2]. We choose I_G @ +2 V for comparison because the contribution of the transient displacement current is smaller than the conduction current at high V_G, which can be seen from the relatively smaller deviation of the current from two directions at the high voltage than at the low voltage region. This indicates I_G @ +2 V is dominated by the steady-state conduction current.

In order to find the cause of the reduced reverse bias current, high-frequency *C–V* curves were measured, as shown in Fig. 3. The effective oxide charge number density (N_{eff}), which are around 2.81×10^{11} cm^{-2} for planar MIS TD and 3.77×10^{11} cm^{-2} for trench MIS TD, can be extracted from the flat band voltage shift of the *C–V* curves. Notice that the *C–V* curves also exhibit big difference between the planar and trench devices when $V_G > 0$ V. To be more specific, the planar MIS TD is in stronger inversion condition, while the trench MIS TD shows a classical deep depletion phenomenon as the gate voltage keeps increasing to $V_G = +2$ V. This means that in planar devices, there are more minority carriers (electrons) supplied from the neighbor Si (p) substrate outside the gate edge to the surface region (at SiO_2/Si (p) interface) [illustrated

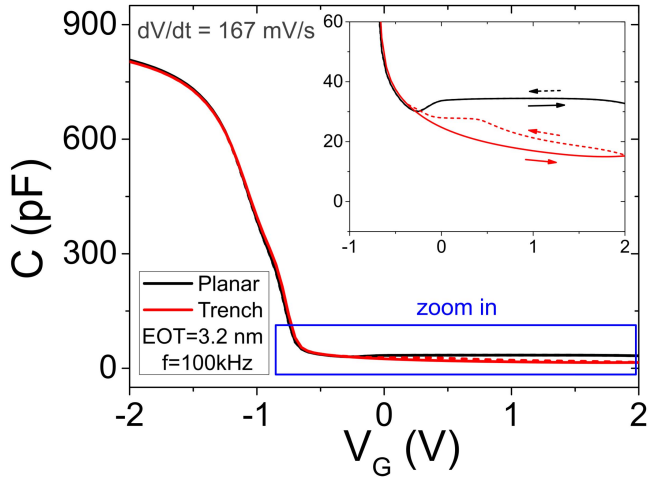

Fig. 3. High-frequency C–V characteristics of the planar and trench MIS TDs with two voltage sweeping directions. Zoomed-in-view of the C–V curves (inset), which shows trench MIS TD is in deep depletion state, while planar MIS TD is in inversion state. The voltage sweeping rate ≈167 mV/s. Voltage sweeps forward from −2 to +2 V (solid line). Voltage sweeps backward from +2 to −2 V (dashed line).

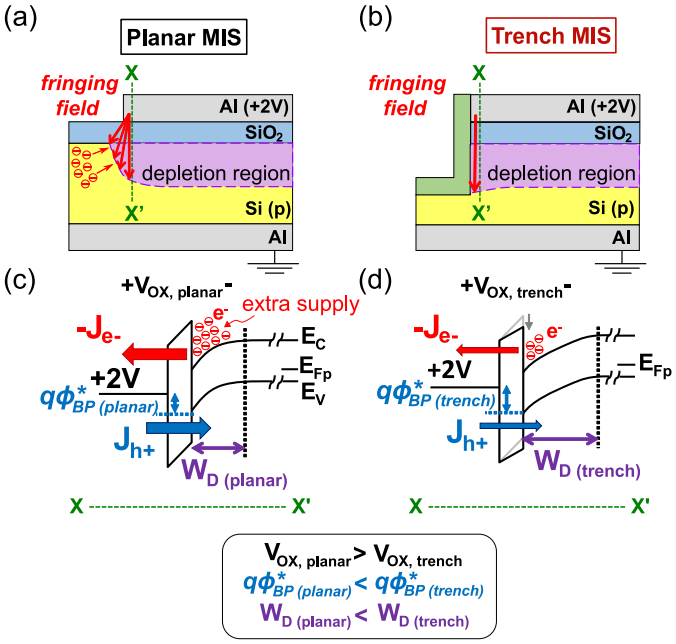

Fig. 4. Schematic cross sections of the (a) planar and (b) trench MIS TDs with fringing field distribution. Fringing field (red arrows). Range of the depletion region (purple region). For the planar MIS TDs, minority carriers (electrons) from the neighbor substrate can supply to the gate edge of the devices. Schematic band diagrams of the (c) planar and (d) trench devices at $V_G = +2$ V along the cutlines in (a) and (b).

in Fig. 4(a)], which causes the device under stronger inversion. On the contrary, for the case of trench MIS TDs, since a part of Si(p) substrate outside the gate edge is removed, the supply number of minority carriers from the Si(p) reduce accordingly [see Fig. 4(b)]. As a result, without enough minority carriers supplement, the number of inversion charges in trench device will not increase as V_G becomes larger. The gate bias equation of MIS TDs can be written as

$$V_G = V_{FB} + V_{\text{ox}} + \psi_s = V_{FB} - \frac{Q_d + Q_i}{C_{\text{ox}}} + \psi_s \quad (1)$$

where V_{FB} is the flat band voltage, V_{ox} is the oxide voltage drop, ψ_s is the surface potential of Si, Q_d is the depletion charge density per unit area, Q_i is the inversion charge density per unit area, and C_{ox} is the oxide capacitance per unit area. For the trench MIS TDs, according to (1), when V_G increases, Q_d and ψ_s will rise because of the almost fixed amount of Q_i, resulting in the enlarging band bending and the deep depletion phenomenon. On the other hand, for planar MIS TDs, because of more supply of Q_i, Q_i can keep increasing as V_G becomes bigger (under stronger inversion), leading to the less changed Q_d, ψ_s, and the shallower depletion region compared with it of trench devices.

Based on the above discussion, the equivalent V_{ox} of trench MIS TDs is smaller than that of the planar MIS TDs at the same positive V_G since more V_G of the trench device drops on ψ_s and causes deep depletion. From (1) and the same V_{FB}, the larger ψ_s means smaller V_{ox} in trench MIS TDs. Fig. 4(c) and (d), which show the schematic band diagrams of the two kinds of device at $V_G = +2$ V, illustrates the concept of equivalently smaller V_{ox} of trench devices. It is believed that this reduced V_{ox} accounts for the smaller reverse bias current in trench MIS TDs. The relation between V_{ox} and the reverse bias current will be explained in the following.

The steady-state reverse bias current of a planar MIS TD can be written as

$$I_{\text{steady}} = I_{e(T)} + I_{h(T)} \quad (2)$$

where $I_{e(T)}$ is the tunneling electron current and $I_{h(T)}$ is the tunneling hole current. Among (2), $I_{h(T)}$ can be expressed as [5], [6], [13]

$$I_{h(T)} = A^* A_{\text{eff}} P_t T^2 \exp\left(-\frac{q\phi^*_{Bp}}{k_B T}\right)\left[1 - \exp\left(-\frac{qV}{k_B T}\right)\right] \quad (3)$$

where A^* is the effective Richardson constant for holes, A_{eff} is the effective current flowing area, P_t is the tunneling probability, T is the temperature, q is the electron charge, ϕ^*_{Bp} is the hole-effective Schottky barrier height (SBH), and k_B is Boltzmann's constant. The hole-effective SBH ϕ^*_{Bp} is related to the oxide voltage (V_{ox}) [6], which can be written as

$$q\phi^*_{Bp} = q\chi_{\text{S}} - q\Phi_{\text{M}} + E_g - qV_{\text{ox}} \quad (4)$$

where χ_{S} is the electron affinity of the semiconductor, Φ_M is the metal work function, and E_g is the semiconductor bandgap.

From (3) and (4), the equivalently larger V_{ox} in planar MIS TDs would result in the decrease of hole-effective SBH ϕ^*_{Bp}, which further leads to larger $I_{h(T)}$ [see Fig. 4(c)]. Since $I_{e(T)}$ is also larger for bigger V_{ox}, it is explicable that planar MIS TDs have larger reverse bias current than trench MIS TDs [by (2)].

Readers may notice that the planar and trench devices have similar capacitance value and forward bias current level at $V_G = -2$ V, which does not reflect the influence of the removed substrate, as shown in Figs. 2 and 3. This is because at $V_G = -2$ V, when MIS TDs are under accumulation

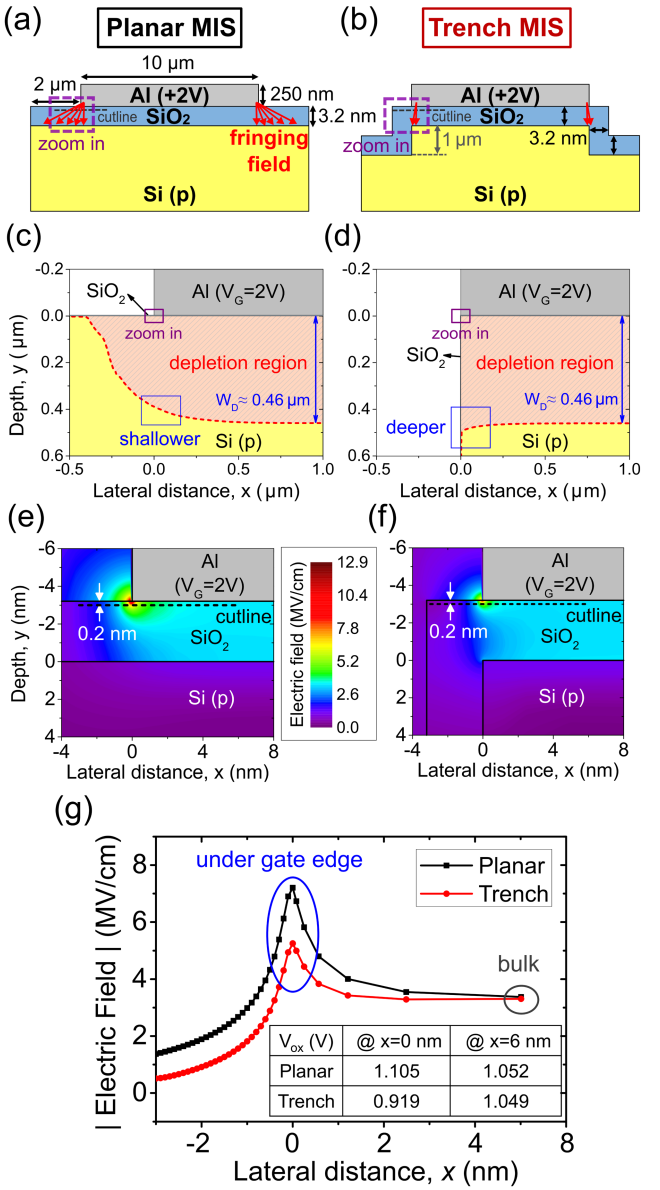

Fig. 5. (a) Structure parameters of the planar MIS TD and (b) trench MIS TD used in Silvaco TCAD simulation. The simulated depletion region of the (c) planar and (d) trench MIS TDs. The simulated total electric field in the (e) planar and (f) trench MIS TDs, confirming the smaller oxide field under the gate edge in trench devices. (g) Total electric field in SiO_2 along the cutlines in (e) and (f). The cutlines are located at 0.2 nm downward from the bottom of the Al gate. Simulated V_{ox} values (inset).

region, it is majority carriers (holes) that accumulate at the SiO_2/Si (p) interface of MIS TDs, not minority carriers. To be more specific, even a part of the substrate is removed, and the rest of the p-type Si substrate in trench devices can still offer enough holes for MIS TDs to maintain in accumulation condition. Therefore, the V_{ox} @ $V_G = -2$ V of the planar and trench devices is expected to be the same, which explains the similarity of capacitance and current properties of both kinds of devices at large negative bias (e.g., $V_G = -2$ V).

In Fig. 5, we use Silvaco TCAD simulation to verify the lower V_{ox} in trench devices. Fig. 5(a) and (b) shows the simulated device structures of the planar and trench MIS TDs, respectively. The difference between the depletion region of the planar and trench devices is demonstrated by the simulation results in Fig. 5(c) and (d). For trench device, the depletion region under the gate edge is indeed deeper than that of the planar MIS TD because of the insufficient minority carriers and smaller V_{ox}. In Fig. 5(e)–(g), we can see the difference in V_{ox} between the planar and trench devices by the electric field in the oxide layers. The expected larger V_{ox} can be verified by the stronger oxide electric field [see Fig. 5(e)] and the larger simulated V_{ox} values [see the inset in Fig. 5(g)] at the gate edge of planar MIS TD compared with trench MIS TD. However, it should be noted that despite the smaller edge V_{ox} in trench devices, the bulk V_{ox} and the bulk oxide electric field (V_{ox} and total oxide electric field @ $x = +6$ nm) in both devices are nearly the same [see Fig. 5(g)]. This is reasonable since the removed substrate only has a great impact on the supply of minority carriers to the edge part of MIS TDs. As to the bulk region of the trench device, it is too far away from the trench structure, so it remains almost unaffected.

B. Enhanced Transient Displacement Current in Trench MIS TDs

Back to Fig. 2, besides the lower reverse bias steady-state current, we also observe a larger transient current in trench devices at the low voltage region. To elaborate, the zero current voltage, where the current transition from negative to positive values or in reverse order happens, of trench devices is -0.25 V in the forward direction and $+0.21$ V in the backward direction when the sweeping rate (dV/dt) is 38 mV/s. For the forward sweeping direction, a negative zero current voltage means that there is a large positive displacement current that causes the total gate current to become positive even before V_G turns to positive voltage. Similarly, for the backward sweeping direction, a positive zero current voltage implies the existence of a negative displacement current. The fact that the magnitude of the zero current voltage becomes larger as the sweeping rate increases again corroborates this transient current behavior comes from displacement current because it is proportional to dV/dt.

For a deeper investigation of this transient behavior, we applied write and read memory operations to the devices. Fig. 6 shows the retention characteristics, whose measurement steps are shown in the inset of the figure, of the planar and trench devices. Note that 0 V read voltage condition is chosen to minimize the steady-state conduction current and the power consumption in the read operation. In Fig. 6, although both devices show negative transient displacement currents at read "-1" operations, the trench MIS TD exhibits apparently larger negative transient current at time $= 0^+$ s, which corresponds to our observation in the I–V curves of Fig. 2 in the backward direction. On the contrary, in read "0," both devices read steady-state currents ≈ 0 A.

Fig. 7(a) demonstrates the endurance characteristics of both devices, which also reflects the stronger read "-1" transient current of the trench device, as observed in Fig. 6. Though a decay of current window (CW) (will be explained later) of the trench device is observed in Fig. 7(b) before 600 cycles,

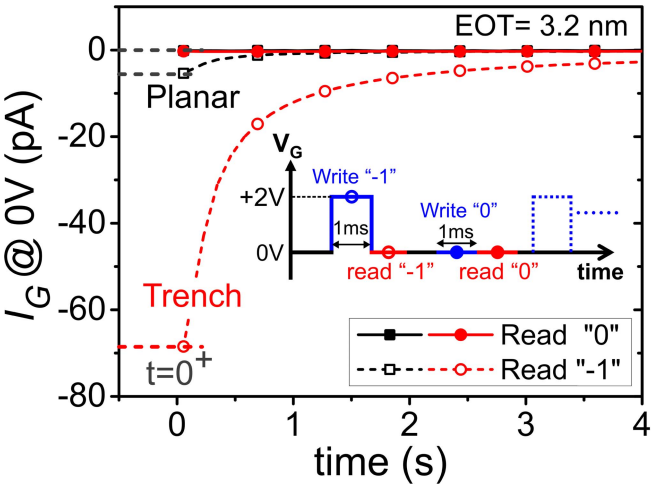

Fig. 6. Retention characteristics of the planar and trench MIS TDs. The inset shows the write and read voltage settings used in the retention measurements. Data of the planar device (black curves). Data of the trench device (red curves).

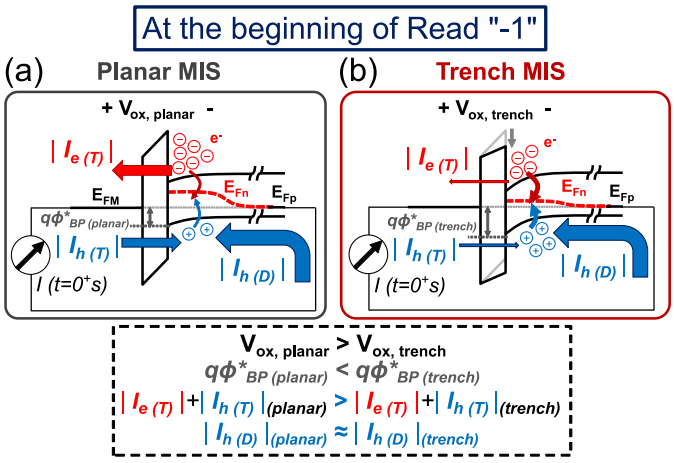

Fig. 8. Schematic band diagrams that illustrate the mechanism of the negative read "−1" current. (a) and (b) Schematic band diagrams of the planar and trench MIS TDs, respectively, at time = 0^+ s. The schematic band diagrams are along the cutlines in Fig. 4 at the gate edge.

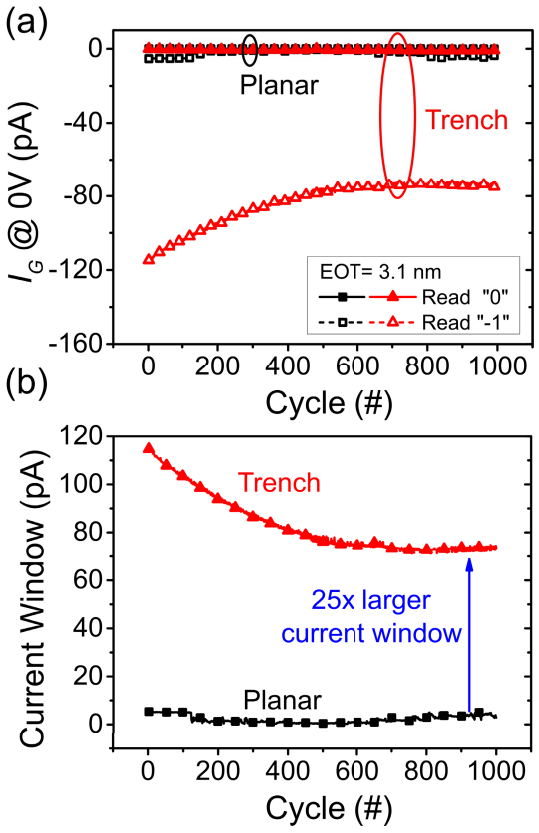

Fig. 7. (a) Endurance characteristics of the planar and trench MIS TDs. The endurance read current data is read at time = 0^+ s in each read program. (b) Extracted CW, which is defined as $I_{G,\text{read "0"}} - I_{G,\text{read "-1"}}$, from the endurance measurement in (a). The write and read voltage settings are the same as the retention measurement in Fig. 6.

it still maintains a 25 times larger CW than the planar device after the CW becomes stable.

Fig. 8 illustrates a possible mechanism to explain the larger negative transient current at read "−1" of the trench MIS TDs. Briefly speaking, when quickly switching from write "−1" ($V_G = +2$ V) to read "−1" ($V_G = 0$ V) operation, minority carriers (Q_{inv}) appealed by $V_G = +2$ V would become excess carriers ($Q_{\text{inv, excess}}$) at $V_G = 0$ V since there is no enough time for they to be recombined or disappear. This causes the non-equilibrium state of the MIS TDs at the beginning of read "−1." For the MIS TDs to return to the equilibrium state, $Q_{\text{inv, excess}}$ needs to be recombined or repelled, generating the transient current we observe. The total transient current consists of three current components [also illustrated in Fig. 8].

1) $Q_{\text{inv, excess}}$ tunnel through gate oxide, which contributes to the positive electron tunneling current, $I_{e(T)}$.
2) Holes from the gate tunnel through gate oxide and then recombine with $Q_{\text{inv, excess}}$, which contributes to positive hole tunneling current, $I_{h(T)}$.
3) Holes from the back gate inject into the Si(p) substrate and then recombine with $Q_{\text{inv, excess}}$, which contributes to the negative hole displacement current, $I_{h(D)}$.

Based on the above description, the read "−1" transient current can be written as

$$I_{G,\ \text{read "−1"}}(t) = |I_{e(T)}(t)| + |I_{h(T)}(t)| - |I_{h(D)}(t)|. \quad (5)$$

For planar devices, we can observe a small negative read "−1" current at t = 0^+ s in Fig. 6. By (5), we can infer that the $|I_{h(D)}|$ current in planar devices is a little bigger than the $|I_{e(T)}|+|I_{h(T)}|$ current, as shown in Fig. 8(a). On the contrary, for trench devices, the enhanced negative read "−1" current implies the much bigger $|I_{h(D)}|$ component than the $|I_{e(T)}| + |I_{h(T)}|$ component [see Fig. 8(b)]. This is because the trench devices have equivalently smaller V_{ox}, which gives rise to smaller gate tunneling current, that is, smaller $|I_{e(T)}|+|I_{h(T)}|$, based on the discussion in Section III-A. If we assume the $|I_{h(D)}|$ components for both the planar and trench devices are the same, according to (5), the larger negative transient current in the trench MIS TD can be deduced, which is consistent with our observation in Fig. 6.

Note that in the above discussion, we mainly focus on the current that flows close to the gate edge and the V_{ox} at the

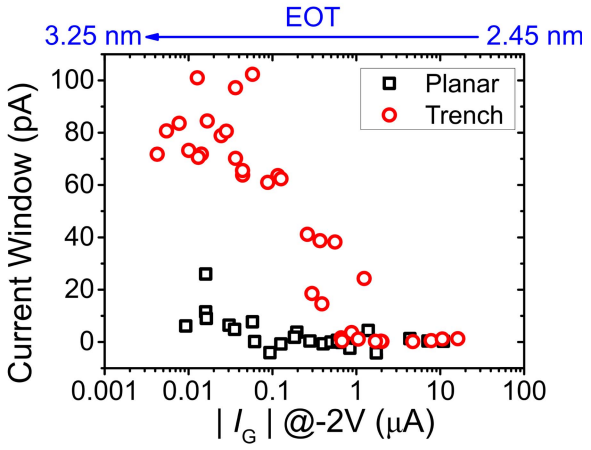

Fig. 9. CW of MIS TDs with different EOT. We use the gate current at forward bias (−2 V) to represent the EOT. The thicker the EOT, the smaller the $|I_G|$@ −2 V becomes. Different $|I_G|$@ −2 V values correspond to different EOT values of the devices.

gate edge to explain the transient current difference between the planar and trench devices [like in Fig. 8]. It is not only because the overall current of MIS TDs is edge-dominated at the reverse bias region [14], but also because bulk V_{ox} and bulk electric field are expected to be the same in two kinds of MIS TDs [see Fig. 5]. As a result, the transient current that flows through the bulk region should be the same in these devices. Regarding the read "0" state, there is no $Q_{inv,\ excess}$ because the voltage conditions of write "0" and read "0" are all 0 V. Hence, both planar and trench MIS TDs show zero transient currents in read "0" state [see Figs. 6 and 7].

Back to Fig. 7(a), the decay of the transient current as the cycle increases might result from the increase in the interface trap density (D_{it}) at SiO_2/Si(p) interface and at trench sidewall as the number of operation cycles rises. The increased D_{it} would recombine some of the $Q_{inv,\ excess}$ and lead to the decrease in transient current and CW.

To investigate the effect of different oxide thicknesses on the transient current behavior, the CWs of devices with various EOTs were measured and plotted in Fig. 9. Note that we use the forward bias current ($|I_G|$@ −2 V) to represent the EOT of the devices. When the EOT becomes thicker, the $|I_G|$@ −2 V would decrease [14]. Regarding the CW, it was extracted from the retention characteristics [like Fig. 6] at time $= 0^+$ s of the devices. Fig. 9 shows that though trench devices exhibit better CW at large EOT, the CW will degrade and ultimately equal to the CW of the planar devices as the EOT getting thinner. It is because when the EOT reduces, the tunneling probability (P_t) will increase since the oxide tunneling barrier will reduce. As a result, the $|I_{e(T)}| + |I_{h(T)}|$ current would become larger. If $|I_{h(D)}|$ current component is unchanged, according to (5), the $I_{G,\text{read "}-1\text{"}}$ and the CW would degrade as the EOT becomes thinner. However, this is not to say the CW of the trench MIS TDs would infinitely increase as EOT getting thicker. We expect that the CW would eventually decay when the EOT becomes too large because of the reduction of C_{ox}. This might lead to the decrease of $Q_{inv,\ excess}$ and further give rise to smaller transient current and CW. More detailed investigation of CW–EOT relation would be part of our future work. To sum up, the trench MIS TDs exhibit better CW than the planar MIS TDs when EOT $\geq$ 2.8 nm.

IV. Conclusion

In this article, we proposed a new structure of MIS TDs, trench MIS TDs. Compared to traditional planar MIS TDs, trench devices demonstrate lower reverse bias steady-state current and enhanced transient current behavior (about 25 times larger CW in the endurance measurement). Based on the high-frequency C–V measurements, the above different properties between the trench and planar devices are believed to result from the insufficient minority carriers (electrons) and the lower equivalent V_{ox} in the trench MIS TDs. In the end, the CW and EOT relation was investigated to show that the trench devices have superior CW than the planar devices at a wide range of EOTs.

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