Enhanced Memory Properties in MIS TD by Forming Trench Structure at the Gate edge

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***Abstract* — A new type of MIS TD memory with trench structure is proposed. The memory properties of MIS TD with trench structure are investigated by current-voltage and memory endurance measurement. It is found that the trench MIS TDs exhibit better memory properties, e.g., larger current difference between reset and set states, compared with conventional planar structure MIS TDs. With the improved memory properties, trench MIS TD may find its use in embedded memory.**

***Index Terms* —metal-insulator-semiconductor (MIS) tunnel diode (TD), trench structure, volatile memory, embedded memory.**

I. Introduction

Embedded capacitor-less memories [1, 2] have become more and more important for the application of internet of things (IoT). As a result, embedded memory with small area, low power, low cost and CMOS compatible are highly desired. Among these memories, conventional planar metal-insulator-semiconductor (MIS) tunnel diode (TD) memory have been reported with clear two-states current by applying long time positive and negative stresses to the gate region [3]. In this work, a new type of MIS TD memory with trench structure is proposed, and is found with enhanced memory properties compared with conventional planar MIS TD.

II. Experimental

Boron-doped p-type (100)-oriented silicon wafers with a resistivity of 1–10 Ω·cm were used as the substrate. After standard Radio Corporation of America (RCA) clean, ultra-thin SiO_2 with various thickness was grown by anodic oxidation in deionized water under room temperature. Rapid thermal annealing (RTA) was then performed in N_2 ambient at 950 °C for 15 s. Later, 200 nm thick aluminum layer was deposited by thermal evaporation, followed by photolithography and wet etching to define the aluminum gate area of the devices. Note that the photoresist (PR) layer was kept after wet etching. Wafers were then divided into two groups of processes: conventional planar MIS (denoted by planar MIS) and MIS with trench structure at the edge of the devices gate metal (denoted by trench MIS). For the planar MIS process, the PR was then removed. As for the trench MIS process, the PR was used as the reactive ion etch (RIE) mask. By applying Si etch RIE recipe, Si trench structure was created at the edge of the PR. A layer of Al_2O_3 was formed by thermal evaporation of aluminum, followed by nitric acid oxidation [4] in order to protect the exposed Si substrate from reacting with oxygen after RIE process. After that, the PR of the trench MIS wafers was then lift-off. Finally, the native oxide on the backside of both groups of wafers was removed by buffered oxide etchant, and then 200 nm thick aluminum was deposited as back electrode. **Fig. 1** shows the schematics of two types of devices.

III. Results and discussion

Fig. 2 shows the current-voltage characteristics of the planar MIS TD and trench MIS TD. After applying reset (-1.5V for 120s then -1.75V for 20s) stress to the gate, the current was measured by sweeping V_G from -0.5V~ +0.5V (solid symbol and solid line). Then, set stress (+1V for 20 s) voltage was applied to the gate, followed by the current measured by sweeping V_G from +0.5V~ -0.5V (open symbol and dash line). It is worth noting that the current of trench MIS becomes smaller after applying reset negative stress. On the contrary, the current level increases after applying set positive voltage stress. The phenomenon of current level change induced by reset and set stress in trench MIS samples was confirmed by measuring lots of trench MIS TDs. Compared with trench MIS, planar MIS shows little current level changes after stress. The results of **Fig. 2** imply that the memory properties, e.g., the two states current, of trench MIS structure are stronger than planar MIS structure.

To further investigate the memory characteristics, endurance measurement with various stress conditions was performed on another pair of planar and trench MIS TDs. **Fig. 3 (a)** demonstrates the endurance measurement steps. Between each stress condition, only set positive stress conditions were modified (+1V 10s / +1V 1s / +0.5V 0.1s). The measured endurance results are shown in **Fig. 3(b)**. Notice that the current differences between reset and set state of the trench MIS under three stress conditions (>250pA) are all larger than the current differences of the planar MIS (<50pA). Furthermore, the current can be set to four different states (denoted “0”, “1”, “2”, “3”) in trench MIS, which is not observed in the planar MIS. All these outcomes are consistent with the implication of **Fig. 2**, which the trench MIS TDs have better memory properties than the planar MIS TDs.

To explain why the trench MIS TDs have better memory properties, a possible mechanism is proposed and exhibited in **Fig. 4**. Compared with planar MIS TDs, MIS TDs with trench structure provide extra charge traps at the trench sidewall. According to the former research [4], the reverse bias current of MIS TDs with ultra-thin oxide is dominated by the current flowing through device edges, which is results from the strong fringing field at the gate metal edge. When “reset negative stress” is applied, electrons are emitted from gate and then trapped in the electron traps at the SiO_2 and trench sidewall. Because of the repulsive Coulomb force caused by large amount of trapped electrons in the trench sidewall, less

electrons are attracted by the gate fringing field and then tunnel through oxide, which results in smaller read "0" current. On the other hand, "set positive stress" evacuates the trapped electrons. With the decreased repulsive Coulomb force, larger current can be read. In summary, extra charge traps at the trench sidewall contribute to the better memory properties of trench MIS TDs.

IV. Conclusion

In this work, a new structure of MIS TD is proposed. With trench structure at the edge of the gate metal, trench MIS TD shows better memory properties than conventional planar MIS TD. Furthermore, the enhanced memory properties of trench MIS TD can be explained by a preliminary electron traps mechanism. With the advantages of low cost, simple structure , low power and CMOS process compatible, trench MIS TD may find its possible use in the future.

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References

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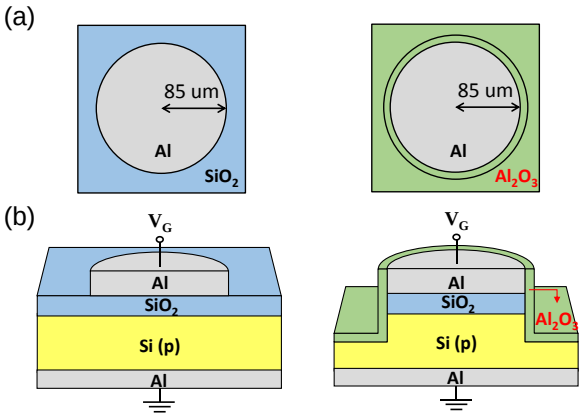

Fig. 1. Schematics of (a) top views and (b) cross sections of the conventional planar MIS TD (left) and the trench MIS TD (right).

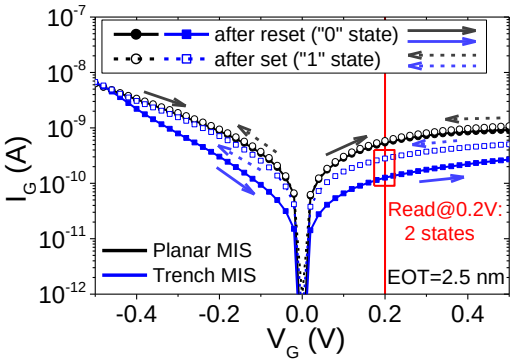

Fig. 2. Current-voltage characteristics of the devices. Reset stress ("0" state): -1.5V for 120s, then -1.75V for 20s. Set stress ("1" state): +1V for 20s.

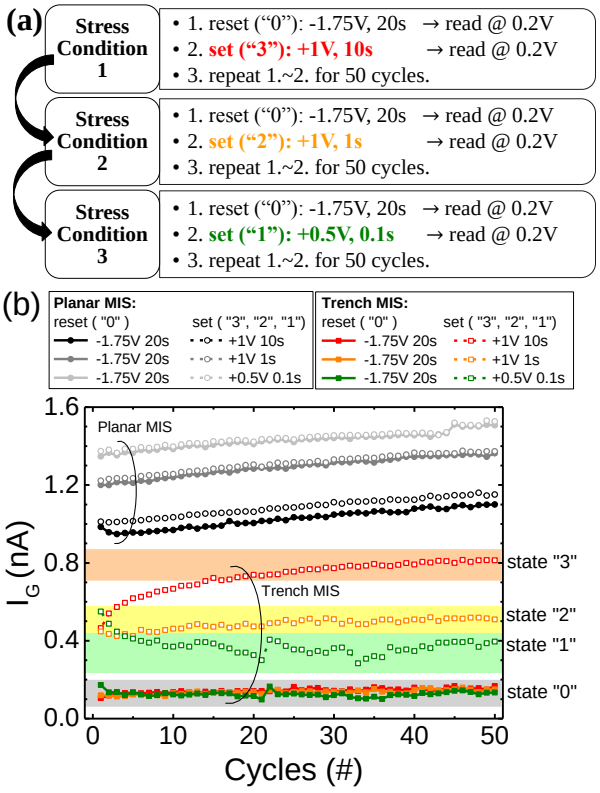

Fig. 3. (a) Measurement steps of endurance test under different stress conditions. (b) Endurance test of planar and trench MIS. Stress condition 1: (black, red), 2: (gray, orange), 3: (light gray, green).

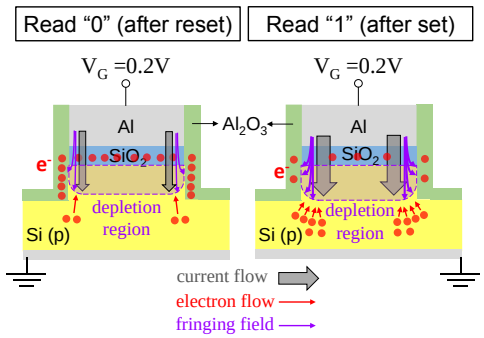

Fig. 4. The schematic diagrams of the proposed electron trapping mechanisms. Left: the read process after reset (-1.5V 120s then -1.75V 20s). Right: the read process after set (+1V 20s).