具閘極邊界溝槽結構之金氧半穿隧二極體之暫態電流強化行為

Enhanced Transient Current Behavior in MIS(p) Tunnel Diode with Gate Edge Trench Structure

Presenter: Jian-Yu Lin (林建宇)

Advisor : Dr. Jenn-Gwo Hwu (胡振國 博士)

Graduate Institute of Electronics Engineering
National Taiwan University

NTUEE
C-V LAB

Outline

- ***Introduction***
- ***Experimental***
- ***<u>Part I.</u>*** ***I–V and C–V Characteristics of Trench MIS TDs***
- ***<u>Part II.</u>*** ***Transient Current Behavior of Trench MIS TDs***
- ***<u>Part III.</u>*** ***Influence of EOT on Transient Current Behavior of MIS TDs***
- ***Conclusion and Future Work***

Outline

- ***Introduction***
- ***Experimental***
- ***Part I.*** ***I–V and C–V Characteristics of Trench MIS TDs***
- ***Part II.*** ***Transient Current Behavior of Trench MIS TDs***
- ***Part III.*** ***Influence of EOT on Transient Current Behavior of MIS TDs***
- ***Conclusion and Future Work***

Outline

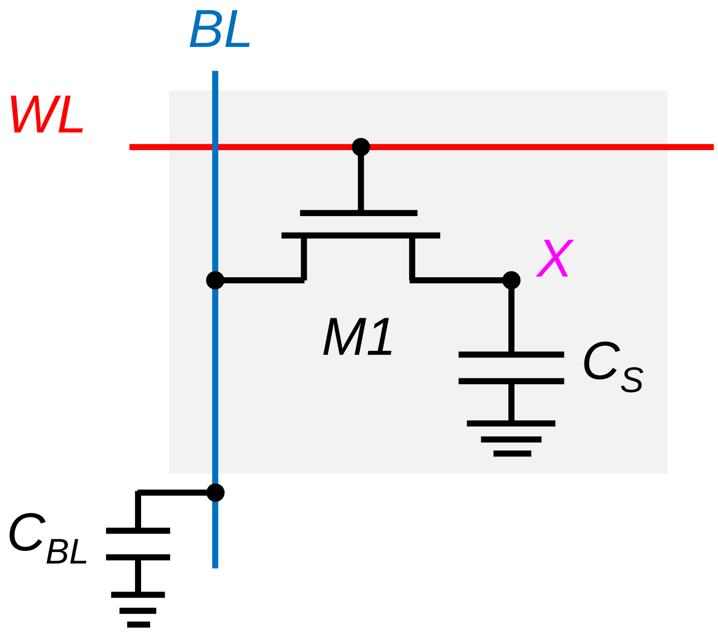
- ***Introduction***
  - **Motivation**
  - **Background of MIS TDs**
    - ***I–V*** **Characteristics**
    - **Deep Depletion Phenomenon**
    - **d_{ox}-Dependency of *I–V* Curves**

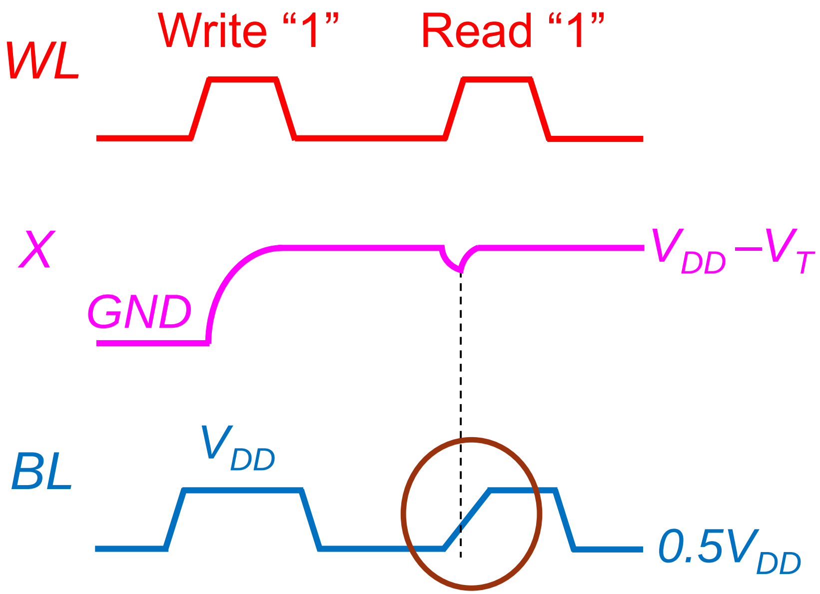
Outline

- ***Introduction***
  - **➢Motivation**
  - **➢Background of MIS TDs**
    - ***I–V* Characteristics**
    - **Deep Depletion Phenomenon**
    - **d_{ox}-Dependency of *I–V* Curves**

Motivation

- **Transient behavior in electronic devices is important.**
  - **represent potential for memory applications.**



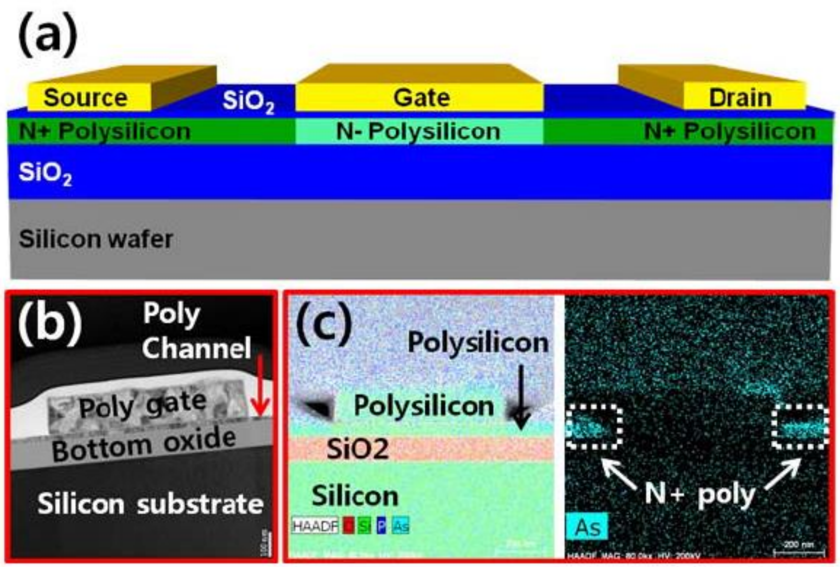


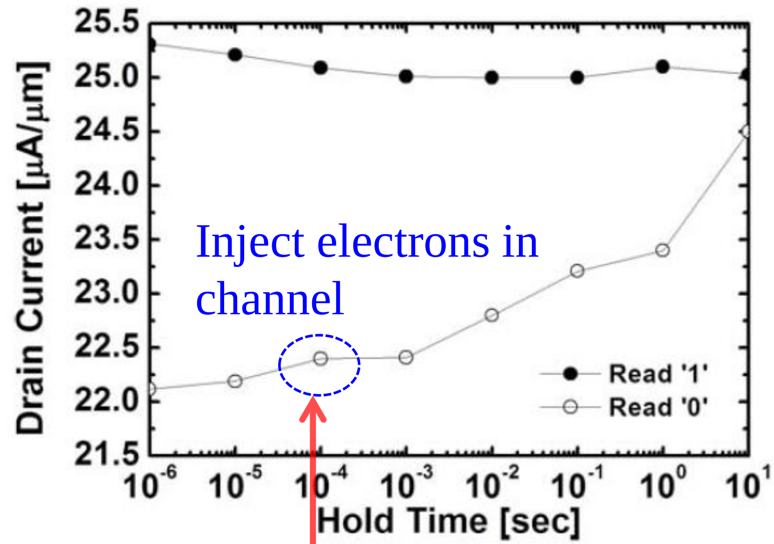
1T-1C DRAM:

- **memory states can be read by transient voltage behavior caused by charges in capacitance.**

Motivation (cont.)

NMOS





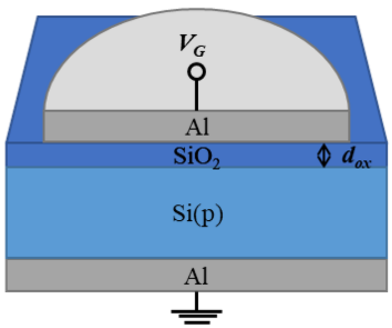
Capacitor-less DRAM (or 1T-DRAM):

- **Most of the devices are build on SOI.**
- **Memory states can be read by transient current behavior.**

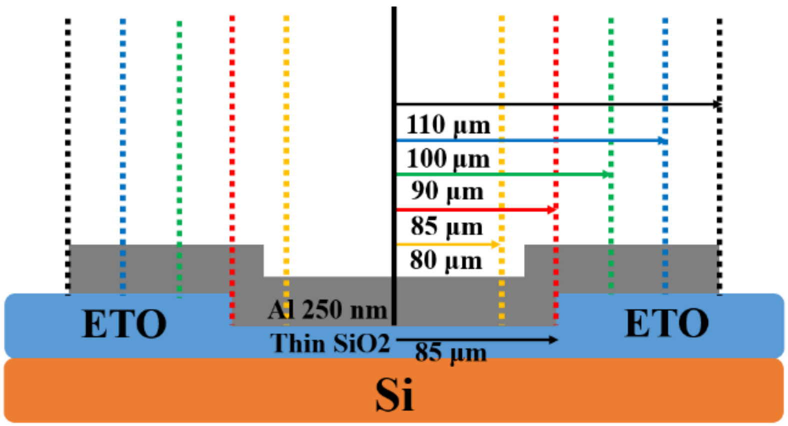
J. H. Seo et al., "Fabrication and Characterization of a Thin-Body Poly-Si 1T DRAM With Charge-Trap Effect," in IEEE Electron Device Letters, vol. 40, no. 4, pp. 566-569, April 2019, doi: 10.1109/LED.2019.2901003.

Transient Current Behavior in MIS TDs

Metal-insulator-semiconductor (MIS) tunnel diodes (TDs) also show transient current behavior by special structure design.

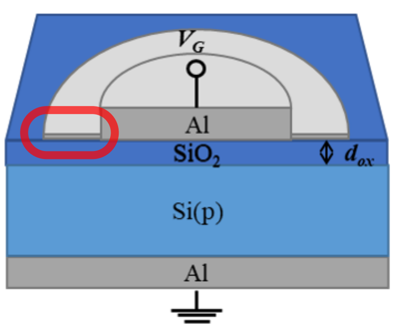


Normal Structure MIS TD



ETO MIS
(Edge-Thickened Oxide) MIS [2]

Ultrathin metal

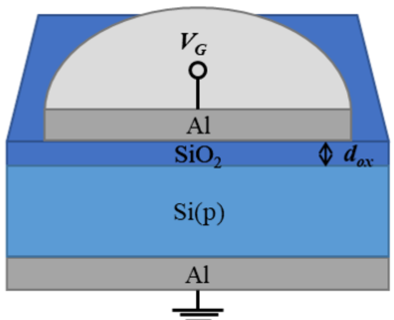


UTMSG MIS
(ultrathin metal surrounded gate) MIS [1]

[1] C.F.Cheng, et al., ECS Journal of Solid State Science and Technology, Vol.8, No.12, December, PP. N214-N219, doi: 10.1149/2.0191912jss.
[2] Y.-C. Yang, et al., ECS Journal of Solid State Science and Technology, vol. 9, no. 10, p. 103006, 2020/11/03 2020, doi: 10.1149/2162-8777/abc576.

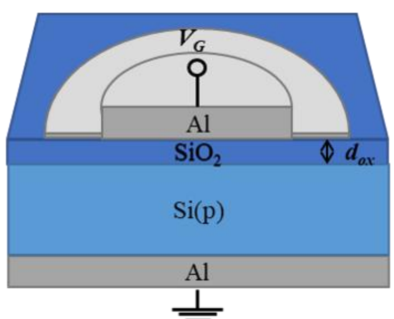
Transient Behavior in UTMSG MIS

Normal structure (control group)

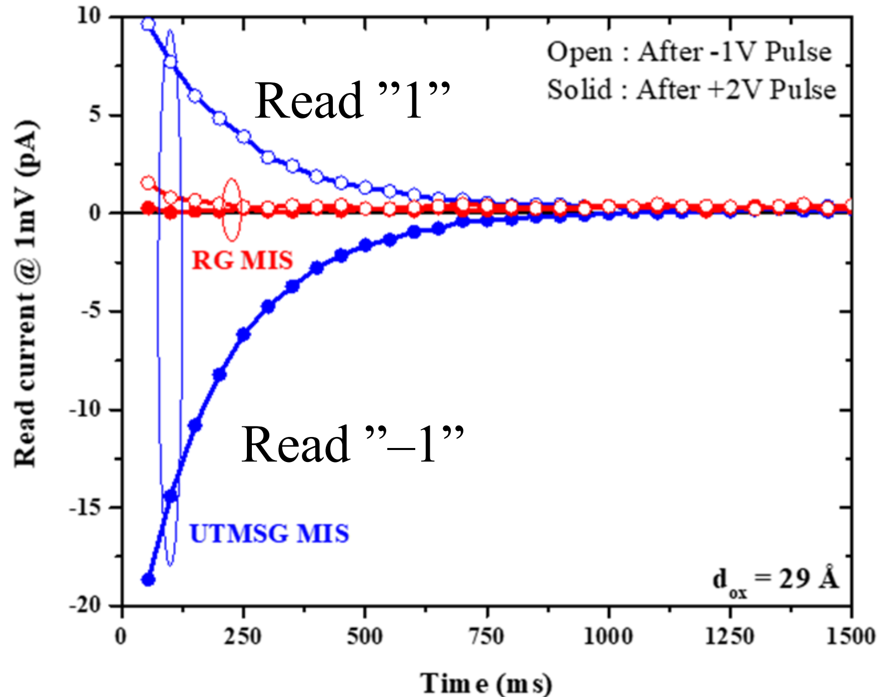


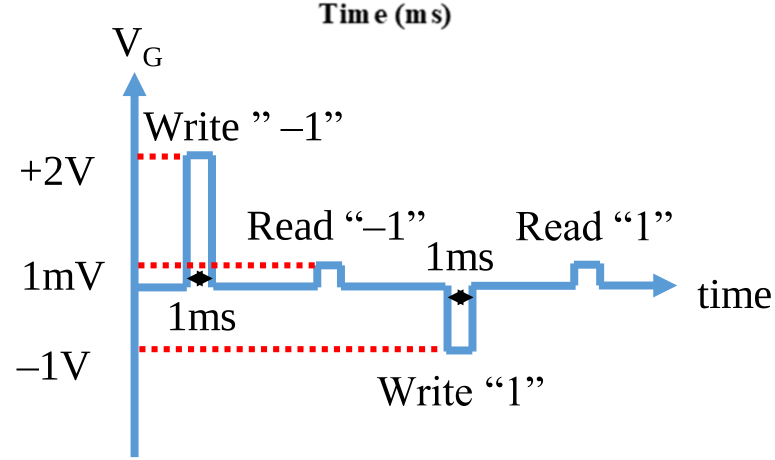
RG MIS
(regular gate) MIS

Special structure



UTMSG MIS
(ultrathin metal surrounded gate) MIS

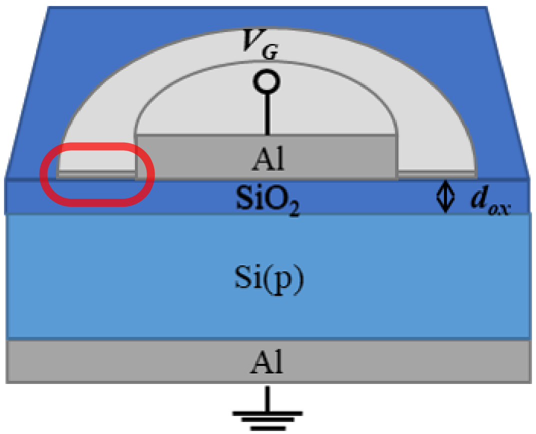




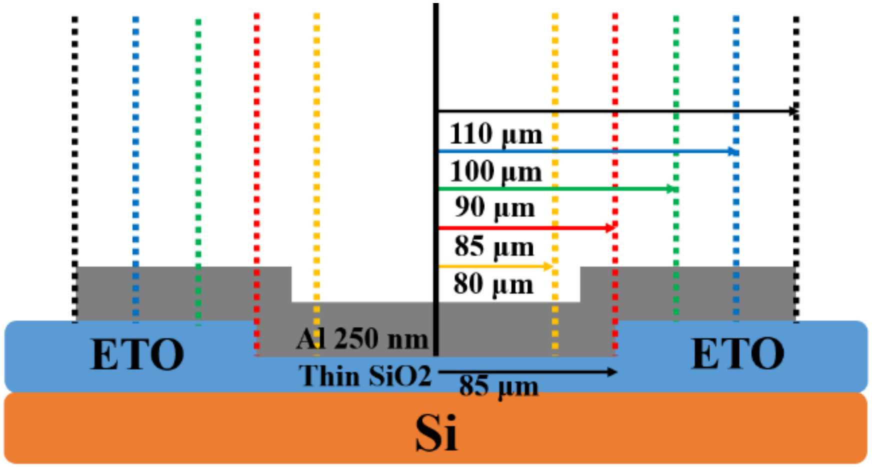
C.F.Cheng, et al., ECS Journal of Solid State Science and Technology, Vol.8, No.12, December, PP. N214-N219, doi: 10.1149/2.0191912jss.

Problems in Previous Works

Ultrathin metal



UTMSG MIS [1]



ETO MIS [2]

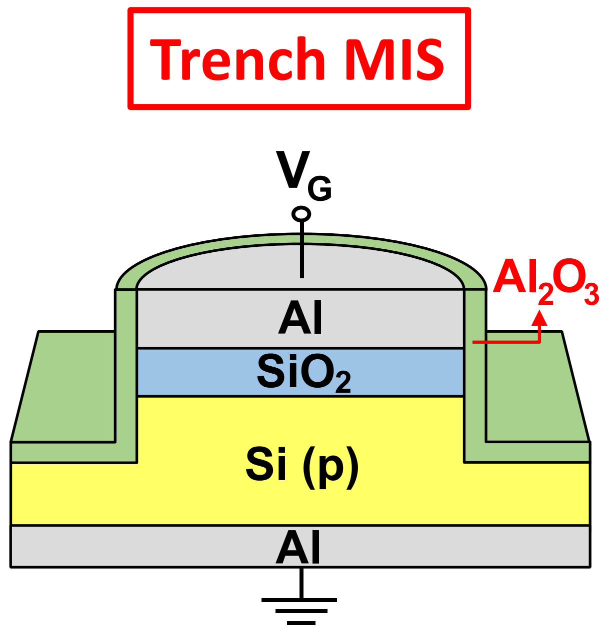
- Normal structure MIS TDs use **one mask process** to fabricate.
- However, **UTMSG** and **ETO** structure in the previous works need **two masks** photolithography process.

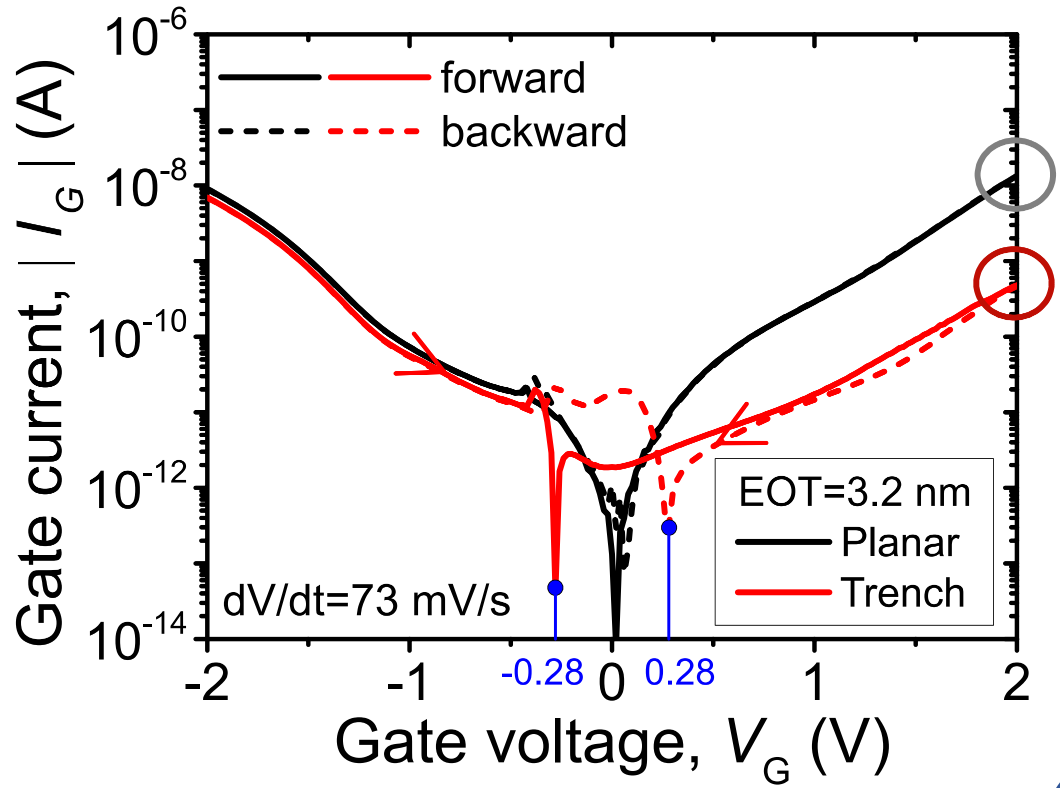
✵ **Fabrication cost ↑.**

[1] C.F.Cheng, et al., ECS Journal of Solid State Science and Technology, Vol.8, No.12, December, PP. N214-N219, doi: 10.1149/2.0191912jss.
[2] Y.-C. Yang, et al., ECS Journal of Solid State Science and Technology, vol. 9, no. 10, p. 103006, 2020/11/03 2020, doi: 10.1149/2162-8777/abc576.

In this Thesis

- A new type of MIS TDs, **trench structure MIS TDs (Trench MIS)**, is proposed.
- Only need **one mask** photolithography process.
- Trench MIS demonstrate **stronger transient current behavior** compared with normal structure MIS TDs (Planar MIS).

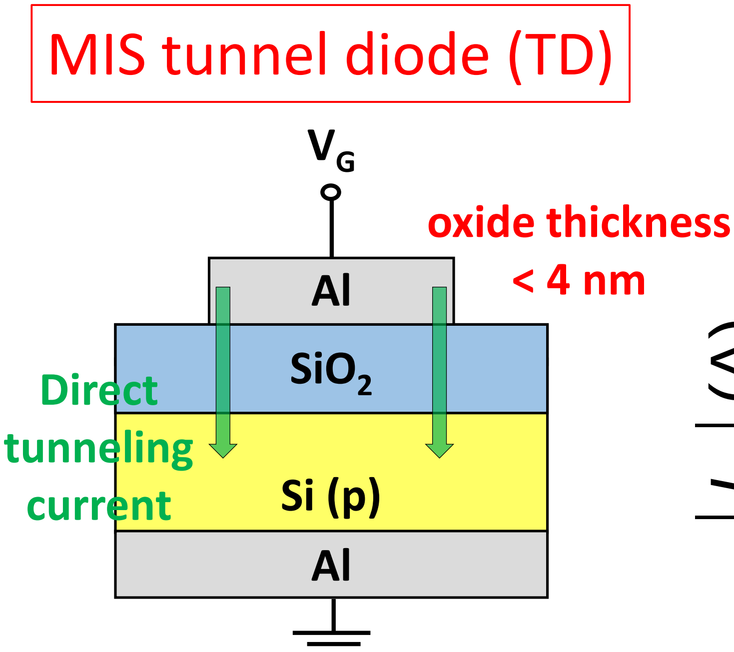


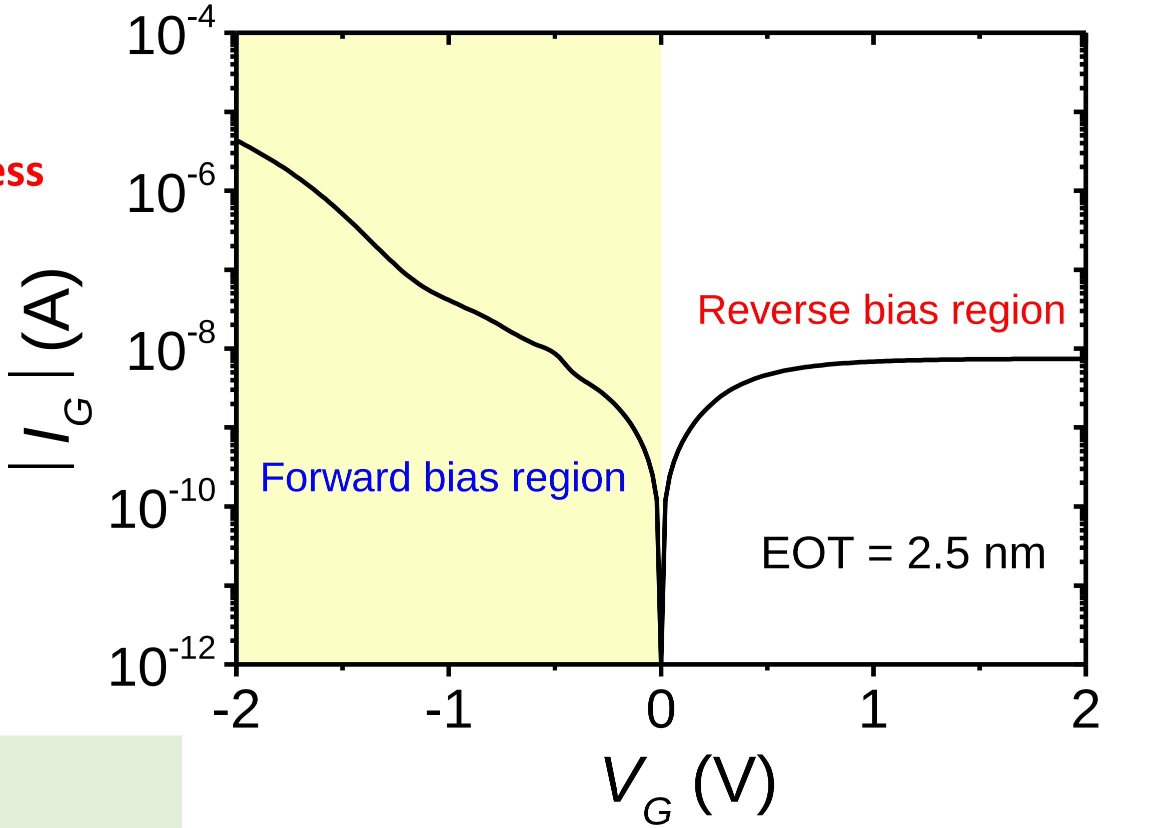


Outline

- ***Introduction***
  - **Motivation**
  - **Background of MIS TDs**
    - ***I–V* Characteristics**
    - **Deep Depletion Phenomenon**
    - **d_{ox}-Dependency of *I–V* Curves**

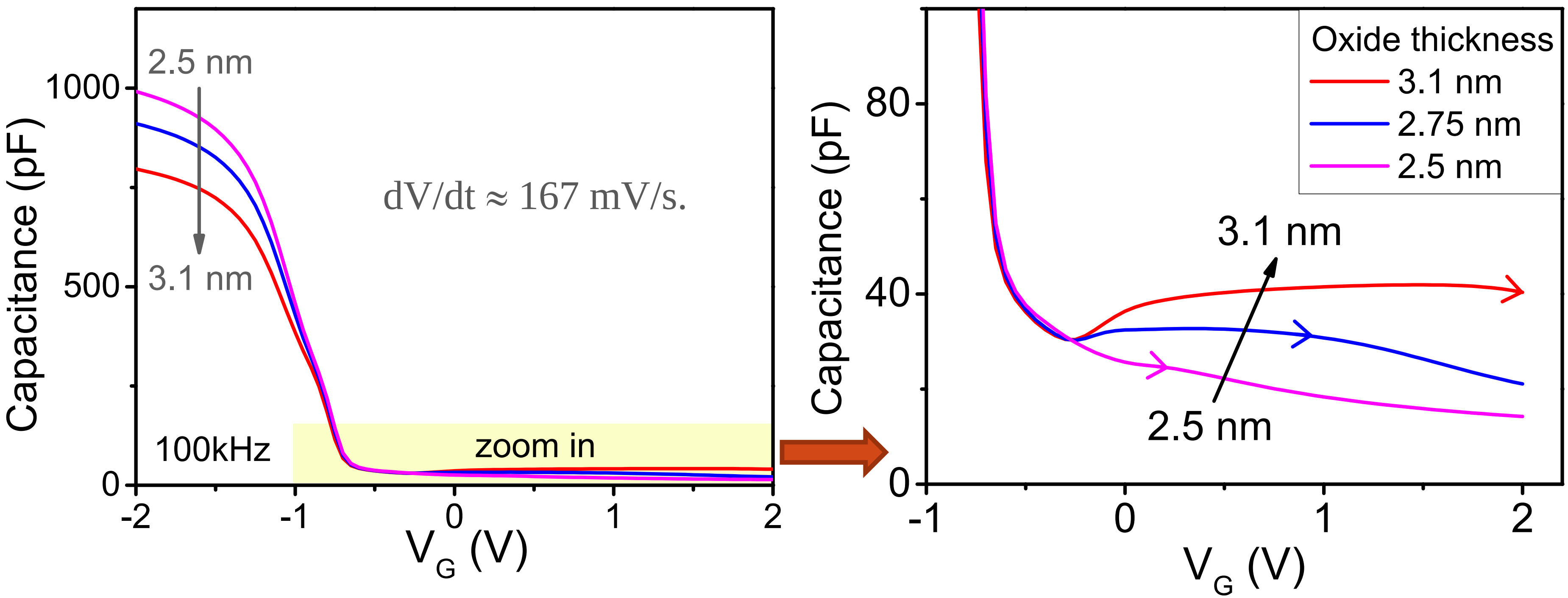
I–V Characteristics of MIS TDs





- Diode-like I–V curve.
- $V_G < 0$: forward bias region.
- $V_G > 0$: reverse bias region.

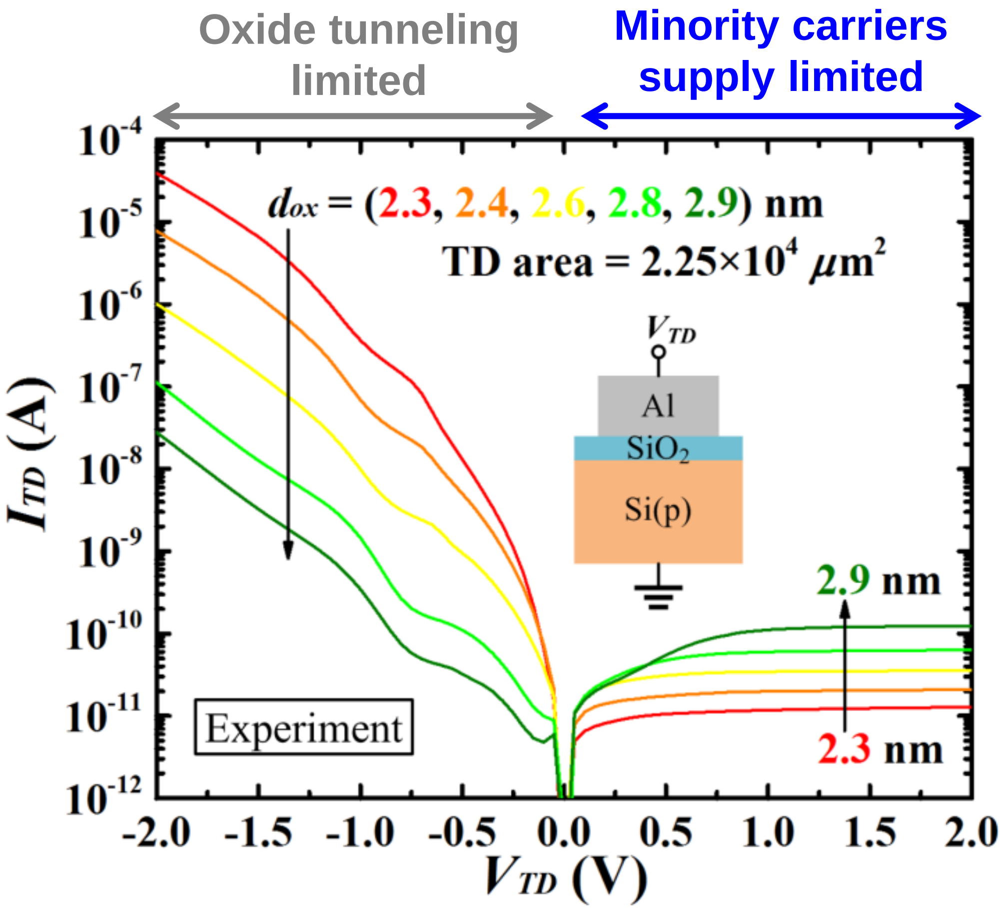
Deep Depletion Phenomenon in MIS TDs

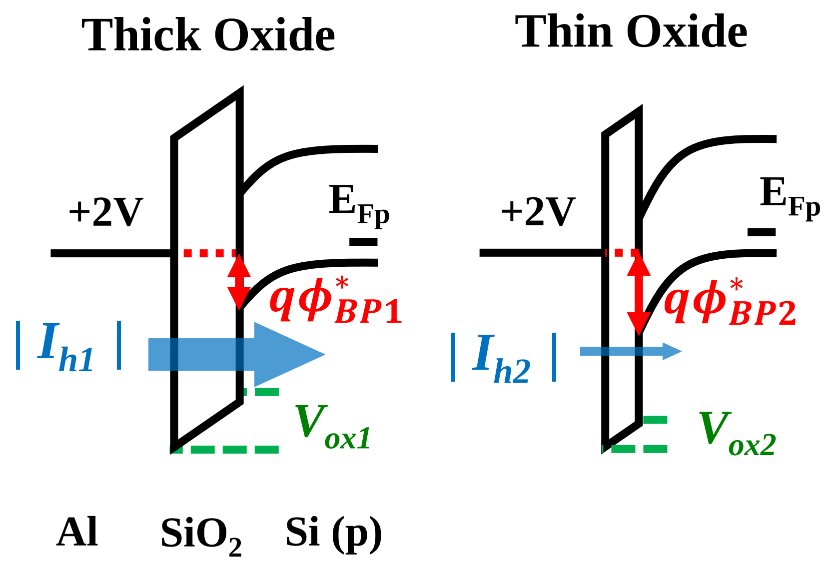


- **Steady-state deep depletion.**
- **High tunneling rate**.
- insufficient inversion carriers (Q_i).
- deeper depletion region.

$$V_G \uparrow = V_{FB} + V_{ox} + \psi_s$$
$$= V_{FB} - \frac{Q_d \uparrow + Q_i}{C_{ox}} + \psi_s \uparrow$$

d_{ox}-Dependency of *I–V* Curves





$$V_{ox1} > V_{ox2}$$
$$q\phi^*_{BP1} < q\phi^*_{BP2}$$
$$|I_{h1}| > |I_{h2}|$$

$$q\phi^*_{Bp} = q\chi_S - q\Phi_M + E_g - qV_{ox}$$

$$I_h = A^* A_{eff} P_t T^2 exp\left(-\frac{q\phi^*_{Bp}}{k_B T}\right)\left[1 - exp\left(-\frac{qV_{TD}}{k_B T}\right)\right]$$

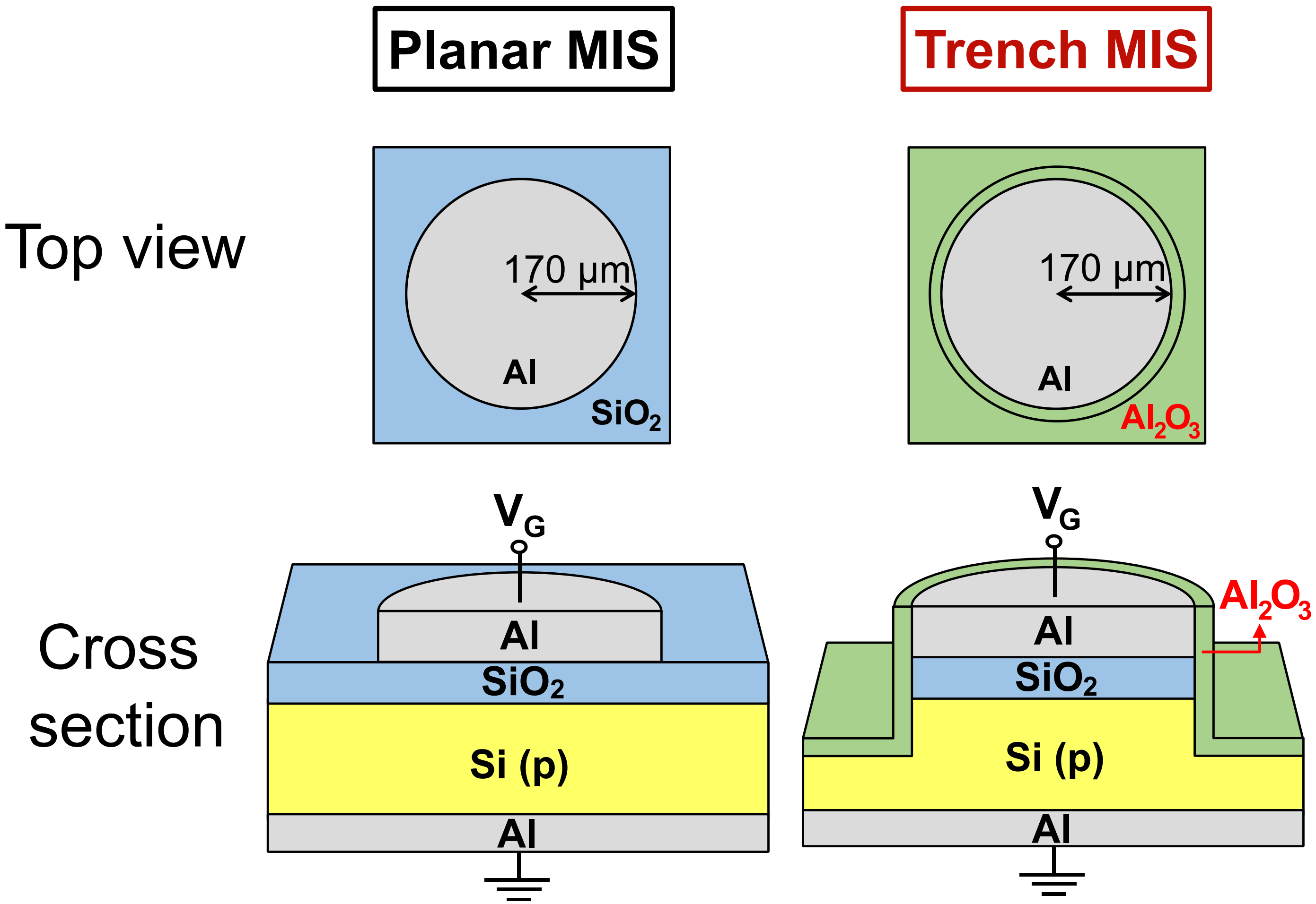
d_{ox} ↑, V_{ox} ↑ , $q\phi^*_{BP}$ ↓, and $|I_h|$ ↑.

C. Liao, W. Kao, and J. Hwu, IEEE Journal of the Electron Devices Society, vol. 4, no. 6, pp. 424-429, 2016, doi: 10.1109/JEDS.2016.2591956.

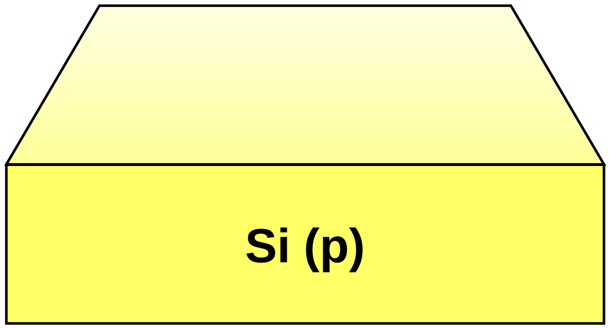
Outline

- *Introduction*
- ***Experimental***
- *Part I.* *I–V and C–V Characteristics of Trench MIS TDs*
- *Part II.* *Transient Current Behavior of Trench MIS TDs*
- *Part III.* *Influence of EOT on Transient Current Behavior of MIS TDs*
- *Conclusion and Future Work*

Device Structure

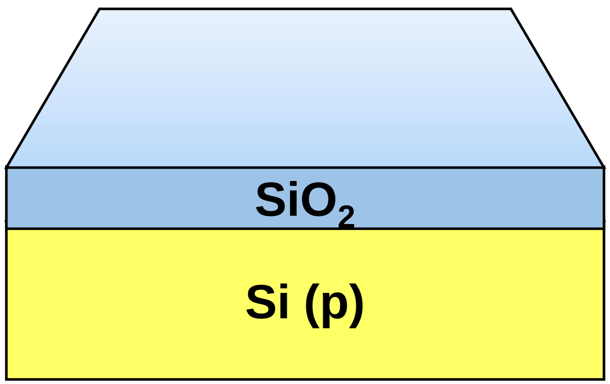


Device Fabrication (1/2)



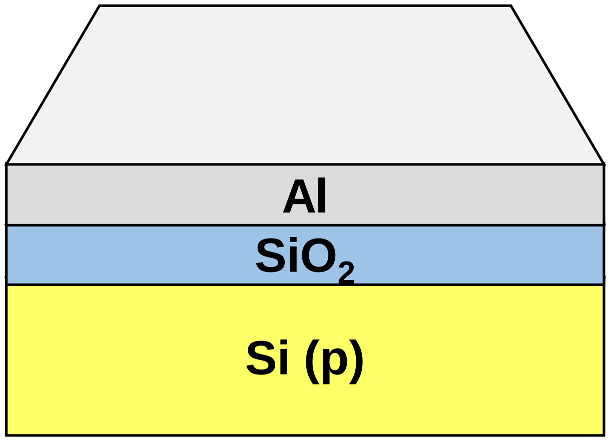
- Radio Corporation of America (RCA) clean
- Ultra-thin oxide grown by anodic oxidation
- RTA in N_2 at 950 ^{0}C for 15 s
- Thermal evaporate 250nm Al as top electrode
- Photolithography
- Al wet etching
- ✵ Si substrate etching by RIE

Device Fabrication (1/2)



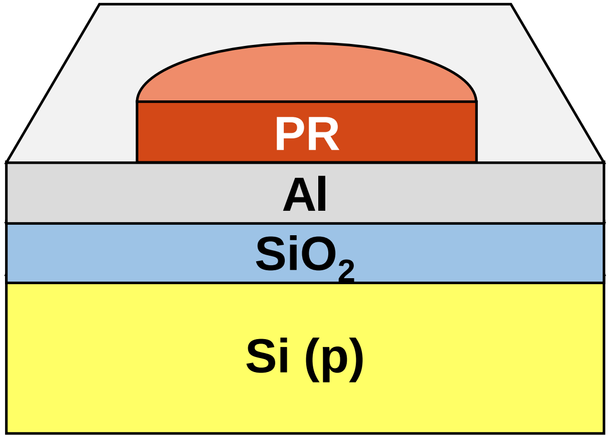
- Radio Corporation of America (RCA) clean
- Ultra-thin oxide grown by anodic oxidation
- RTA in N_2 at 950 ^oC for 15 s
- Thermal evaporate 250nm Al as top electrode
- Photolithography
- Al wet etching
- ✵ Si substrate etching by RIE

Device Fabrication (1/2)



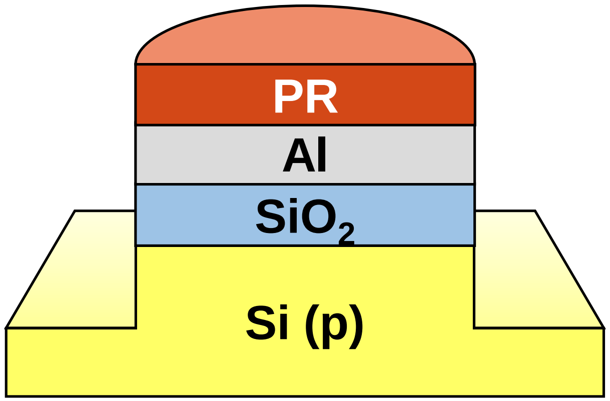
- Radio Corporation of America (RCA) clean
- Ultra-thin oxide grown by anodic oxidation
- RTA in N_2 at 950 ^{0}C for 15 s
- Thermal evaporate 250nm Al as top electrode
- Photolithography
- Al wet etching
- ✵ Si substrate etching by RIE

Device Fabrication (1/2)



- Radio Corporation of America (RCA) clean
- Ultra-thin oxide grown by anodic oxidation
- RTA in N_2 at 950 ^{o}C for 15 s
- Thermal evaporate 250nm Al as top electrode
- Photolithography
- Al wet etching
- ✵ Si substrate etching by RIE

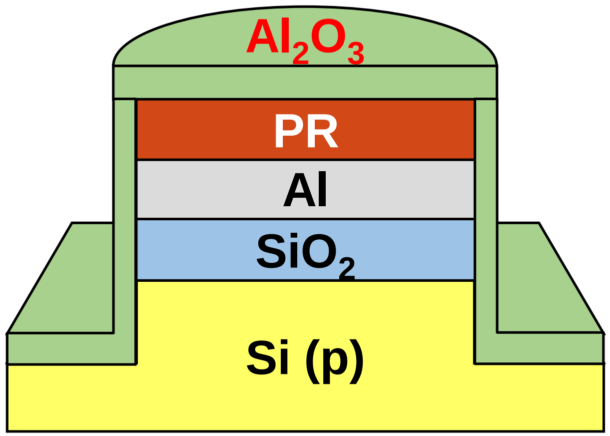
Device Fabrication (1/2)



✵ Trench MIS only process

- Radio Corporation of America (RCA) clean
- Ultra-thin oxide grown by anodic oxidation
- RTA in N_2 at 950 ^{0}C for 15 s
- Thermal evaporate 250nm Al as top electrode
- Photolithography
- Al wet etching
- ✵ Si substrate etching by RIE

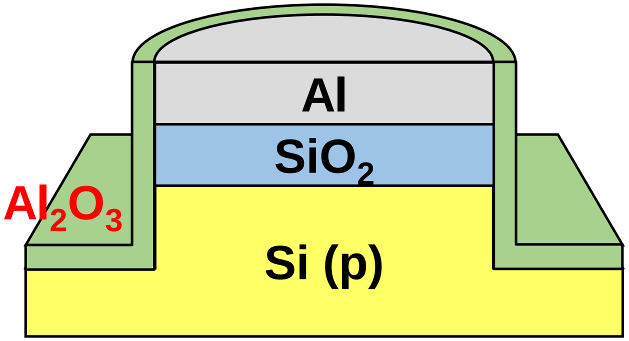
Device Fabrication (2/2)



Al_2O_3 layer:
protect Si substrate from being exposed to air.

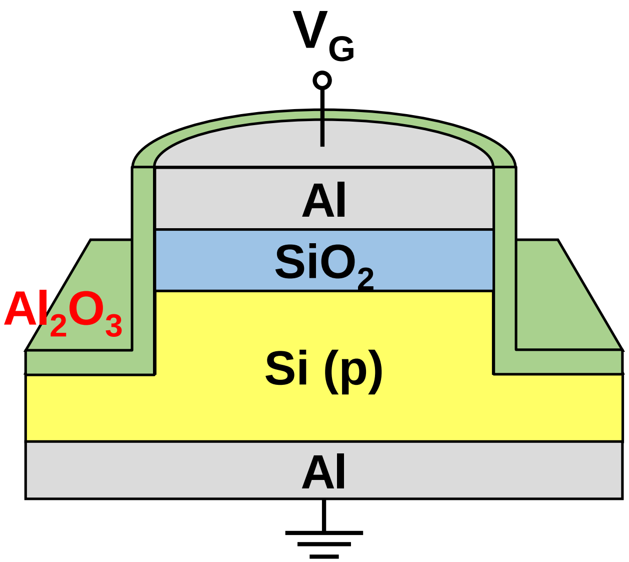
- ✵ Remove native oxide by BOE
- ✵ Deposit Al_2O_3 by *in-situ* oxidation of dc sputtering Al target in Ar/O_2 ambient
- Lift-off photoresist (PR)
- ✵ Furnace annealing in N_2 at 200 ^oC for 10 minutes
- Backside native oxide removal
- 200 nm Al back electrode deposition

Device Fabrication (2/2)



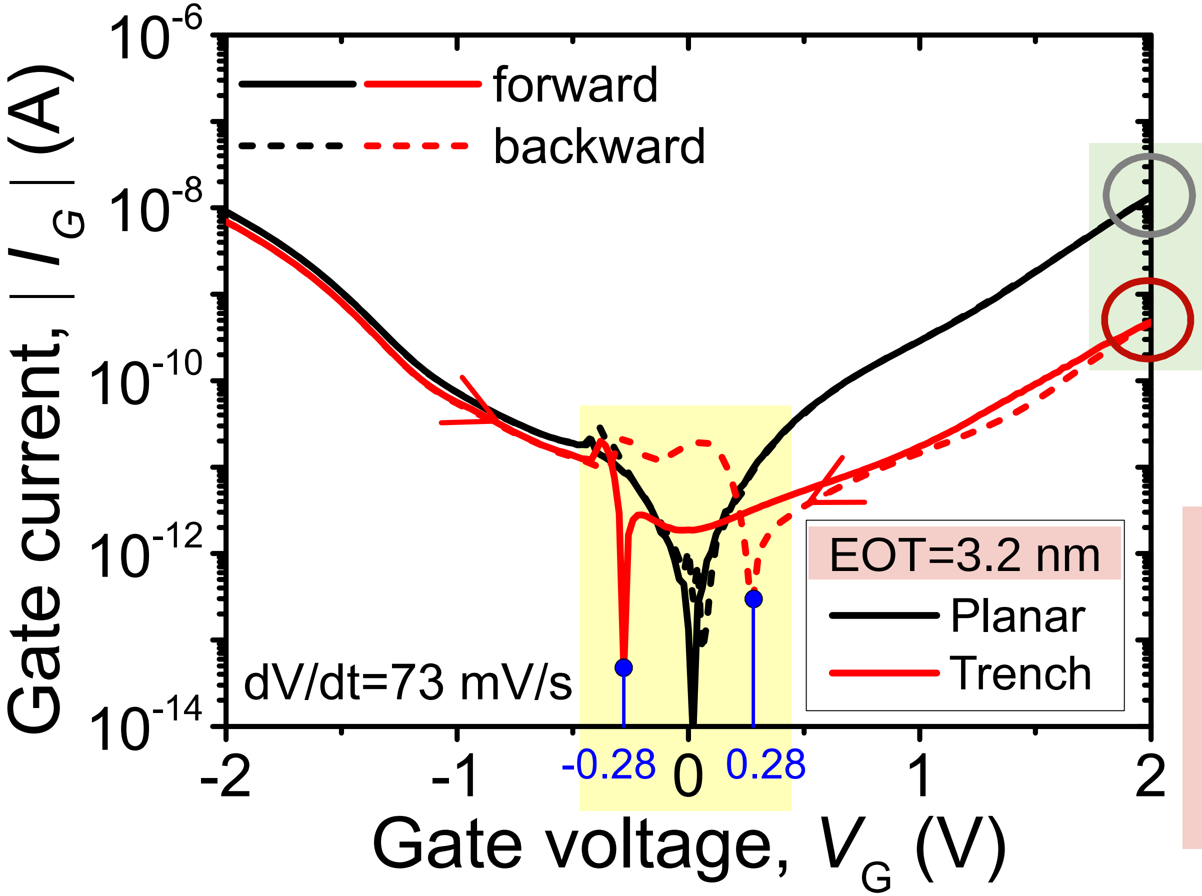
- ✵ Remove native oxide by BOE
- ✵ Deposit Al_2O_3 by *in-situ* oxidation of dc sputtering Al target in Ar/O_2 ambient
- Lift-off photoresist (PR)
- ✵ Furnace annealing in N_2 at 200 ^oC for 10 minutes
- Backside native oxide removal
- 200 nm Al back electrode deposition

Device Fabrication (2/2)



- ✵ Remove native oxide by BOE
- ✵ Deposit Al_2O_3 by *in-situ* oxidation of dc sputtering Al target in Ar/O_2 ambient
- Lift-off photoresist (PR)
- ✵ Furnace annealing in N_2 at 200 ^oC for 10 minutes
- Backside native oxide removal
- 200 nm Al back electrode deposition

Organization of this Thesis



1. **Lower steady-state reverse bias current *(Part I)***

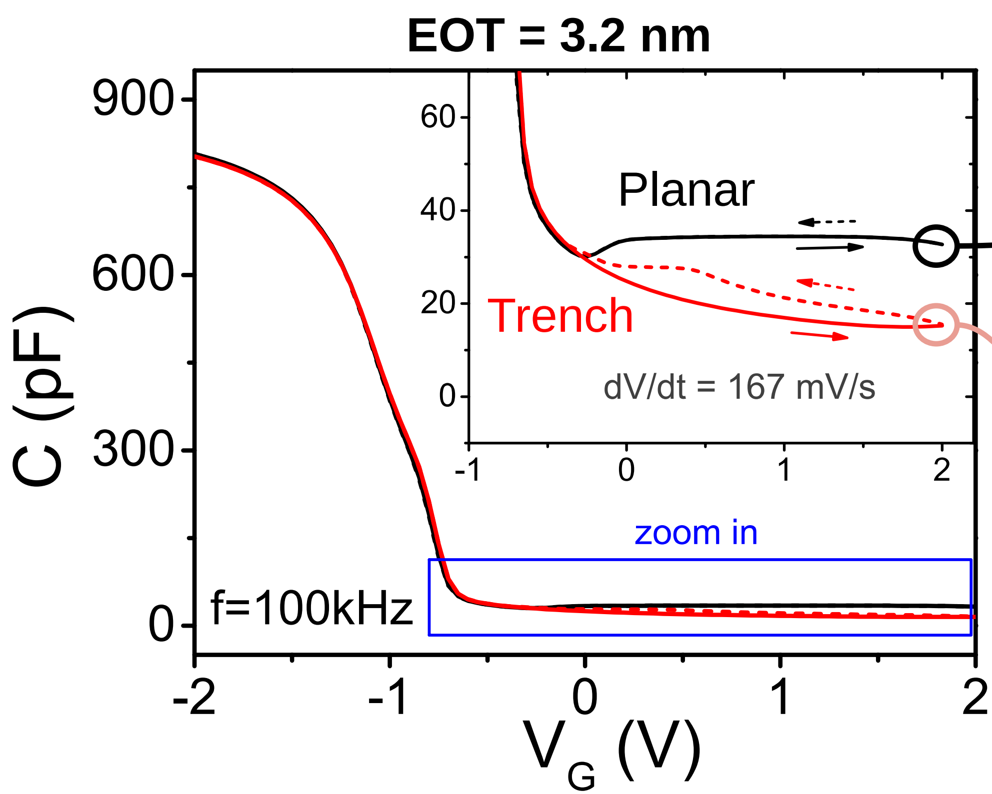
2. **Enhanced transient displacement current *(Part II)***

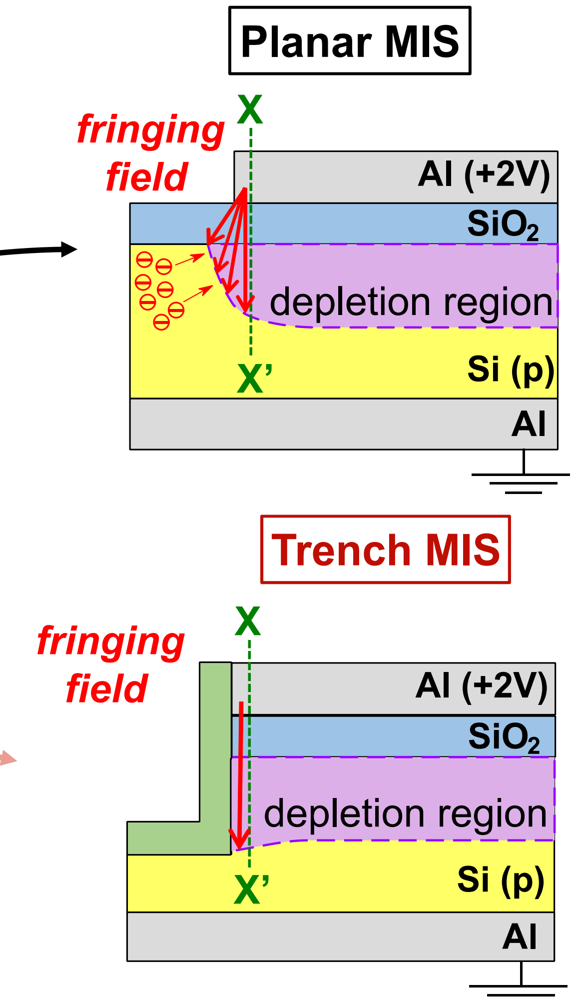
3. **Influence of equivalent oxide thickness (EOT) on transient current *(Part III)***

Outline

- *Introduction*
- *Experimental*
- ***Part I.*** ***I–V and C–V Characteristics of Trench MIS TDs***
- ***Part II.*** ***Transient Current Behavior of Trench MIS TDs***
- ***Part III.*** ***Influence of EOT on Transient Current Behavior of MIS TDs***
- *Conclusion and Future Work*

Reason for the Lower Reverse Bias Current

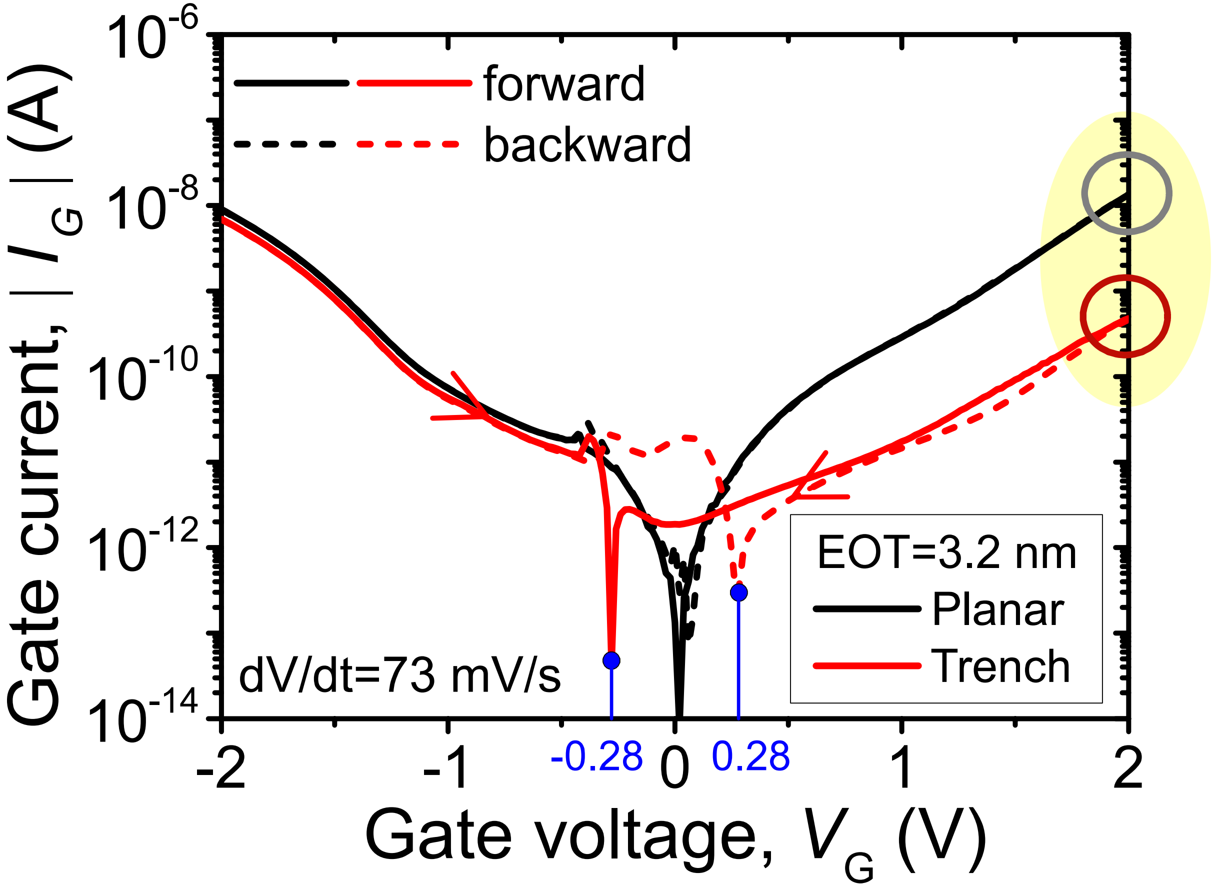




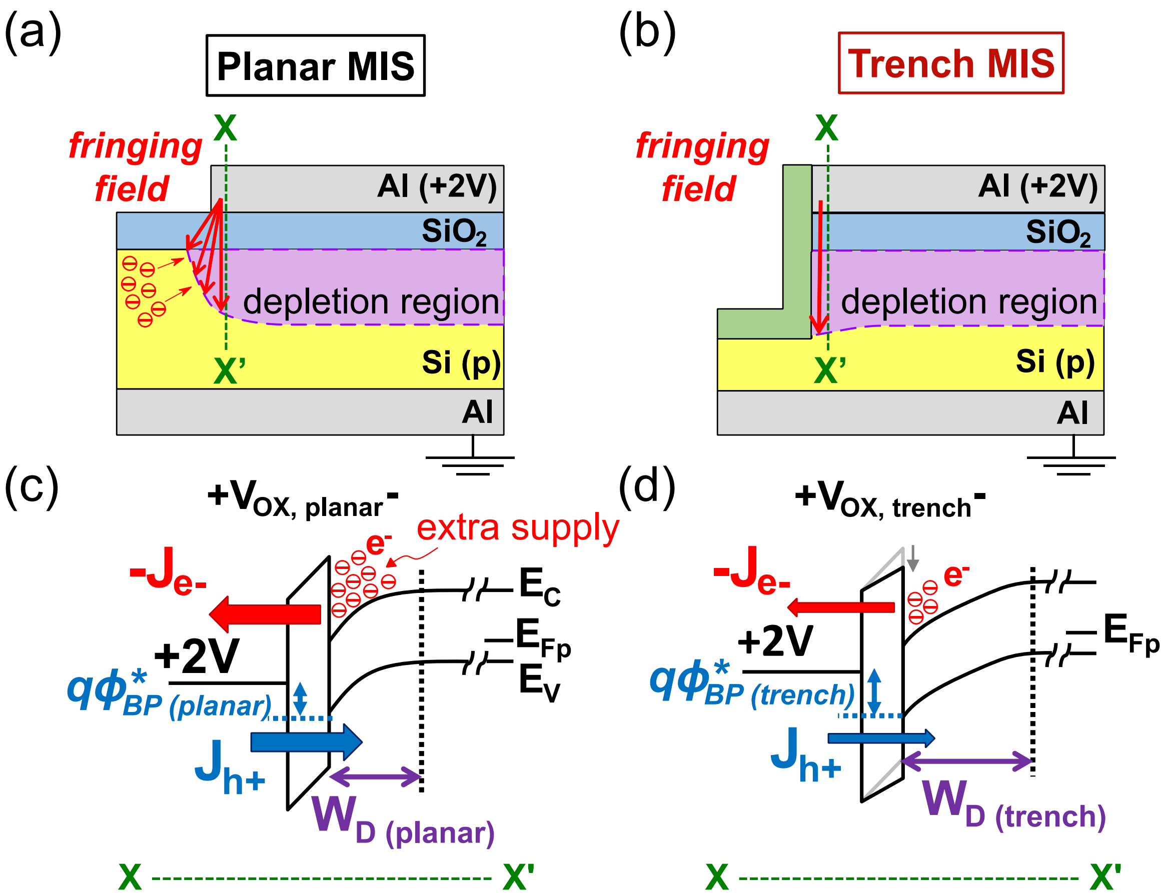
- **Planar:** **sufficient supply of e⁻** from the neutral region in substrate → inversion signal.
- **Trench:** **insufficient supply of e⁻** → **deep depletion.**

$$V_G\uparrow = V_{FB} - \frac{Q_d\uparrow + Q_i\downarrow}{C_{ox}} + \psi_s\uparrow$$

Lower Reverse Bias Current



Equivalently Smaller V_{ox} in Trench Devices



- Trench devices do **not have sufficient electrons.**
  - ➢ **deeper depletion region.**
  - ➢ **equivalently smaller V_{ox}.**
  - ➢ **Smaller reverse bias current (e.g. I_G @ +2V).**

$$V_G = V_{FB} + V_{ox} + \psi_s$$
$$= V_{FB} - \frac{Q_d + Q_i}{C_{ox}} + \psi_s$$

$V_{OX,\ planar} > V_{OX,\ trench}$

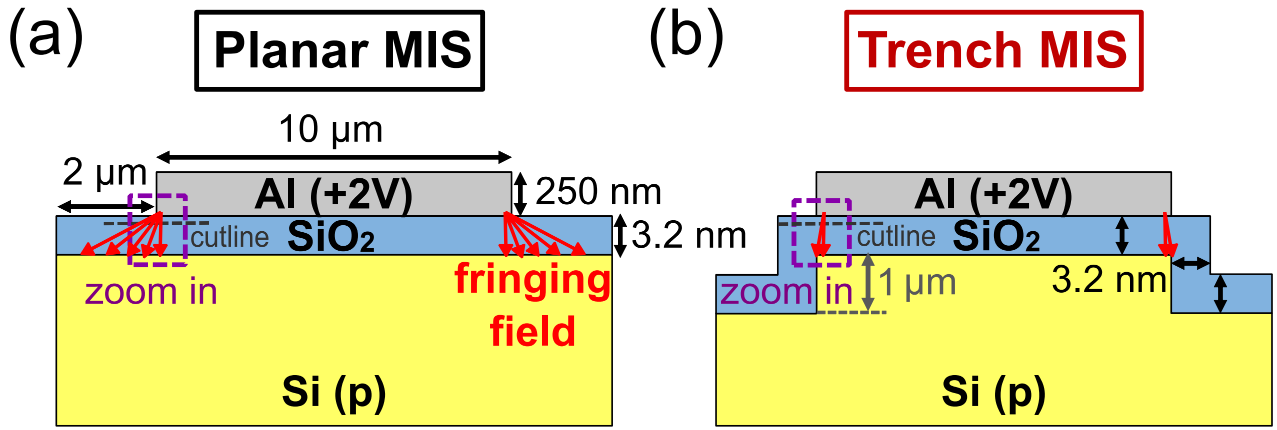
$q\phi^*_{BP\ (planar)} < q\phi^*_{BP\ (trench)}$

$W_{D\ (planar)} < W_{D\ (trench)}$

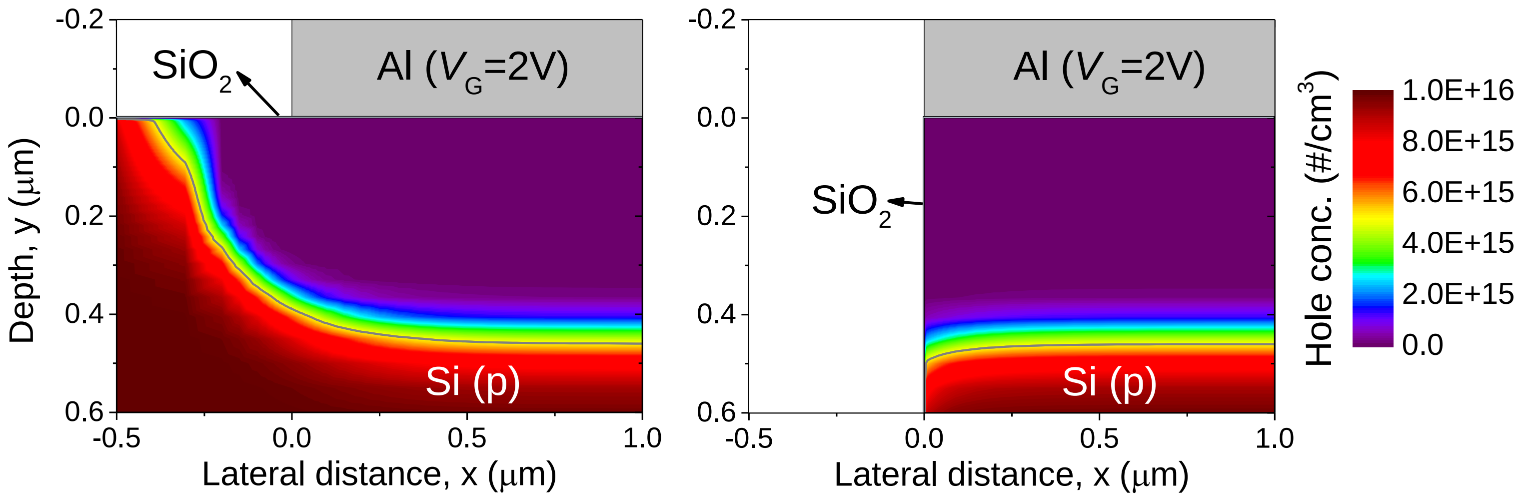
J_{e-}, $J_{h+} \propto V_{ox}$

Steady-State TCAD Simulation (1/3)

Device structure



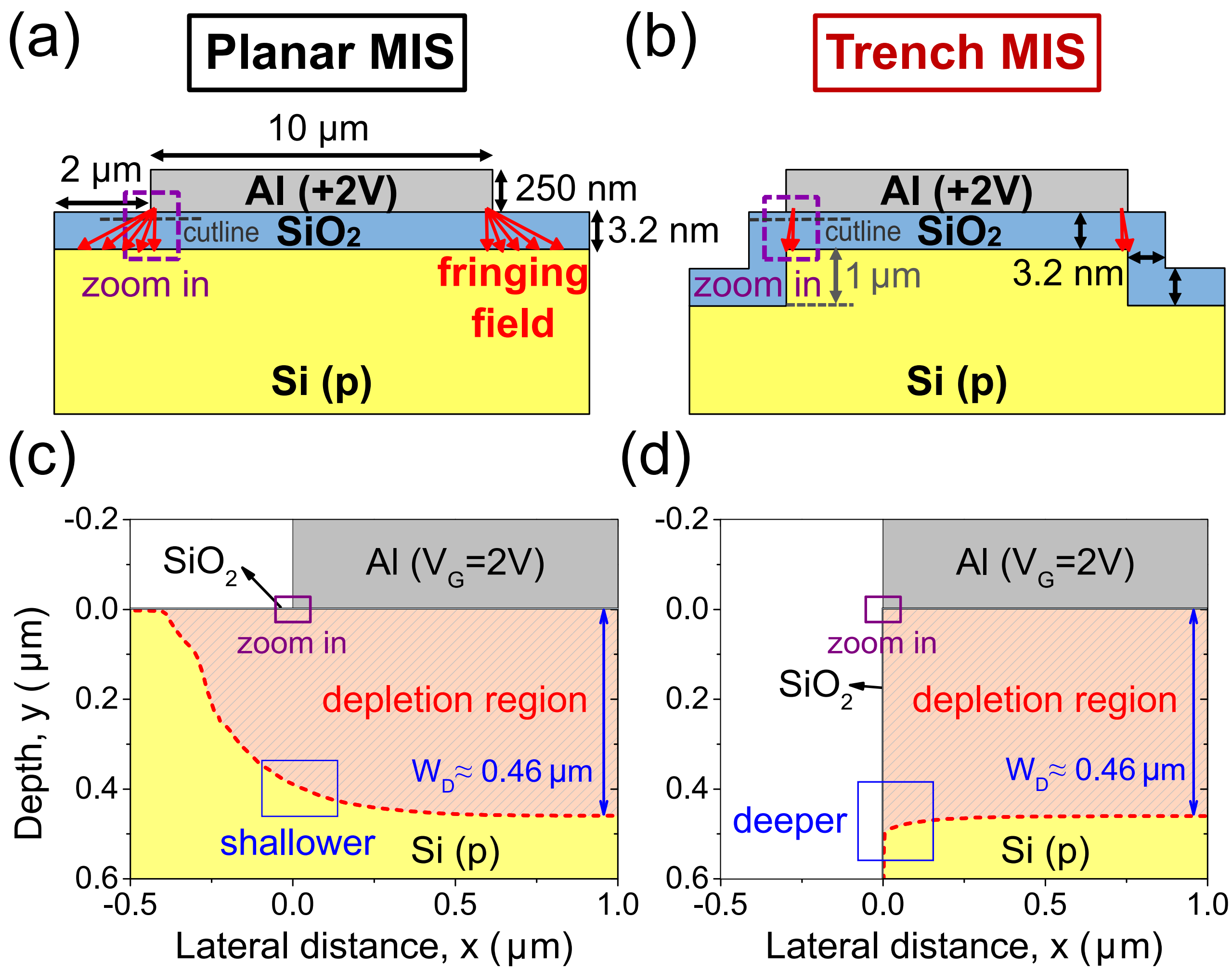
Simulated hole concentration



Steady-State TCAD Simulation (2/3)

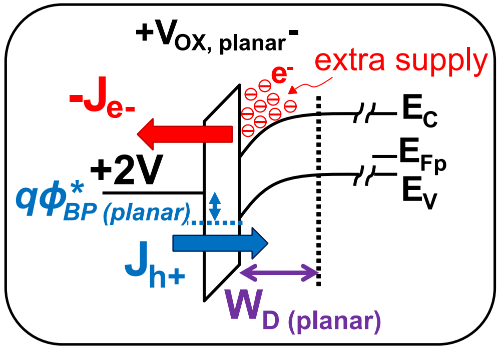
Device structure

Simulated depletion region

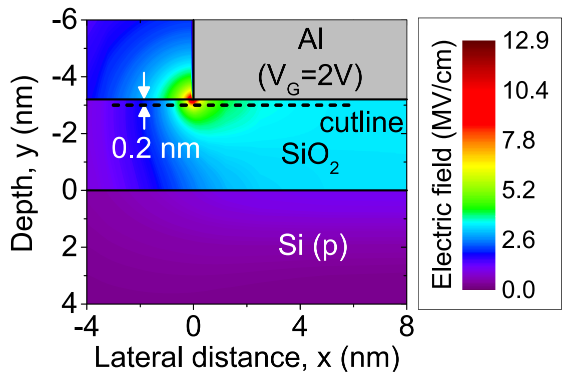


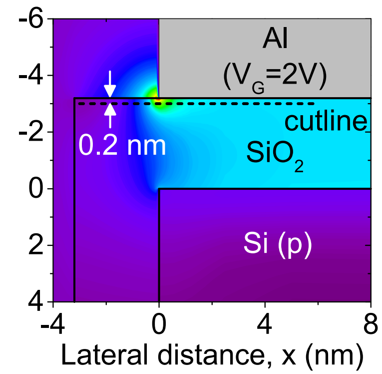
Steady-State TCAD Simulation (3/3)

Planar

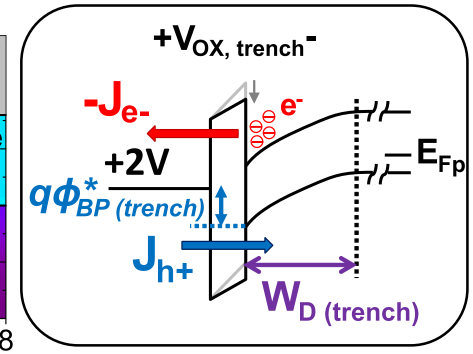


Contour plot of total electric field



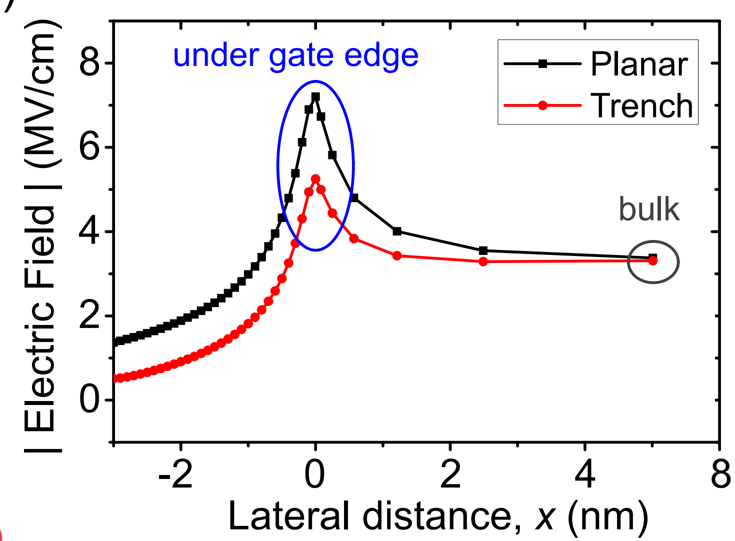


Trench



Total electric field in the oxide layer

(g)



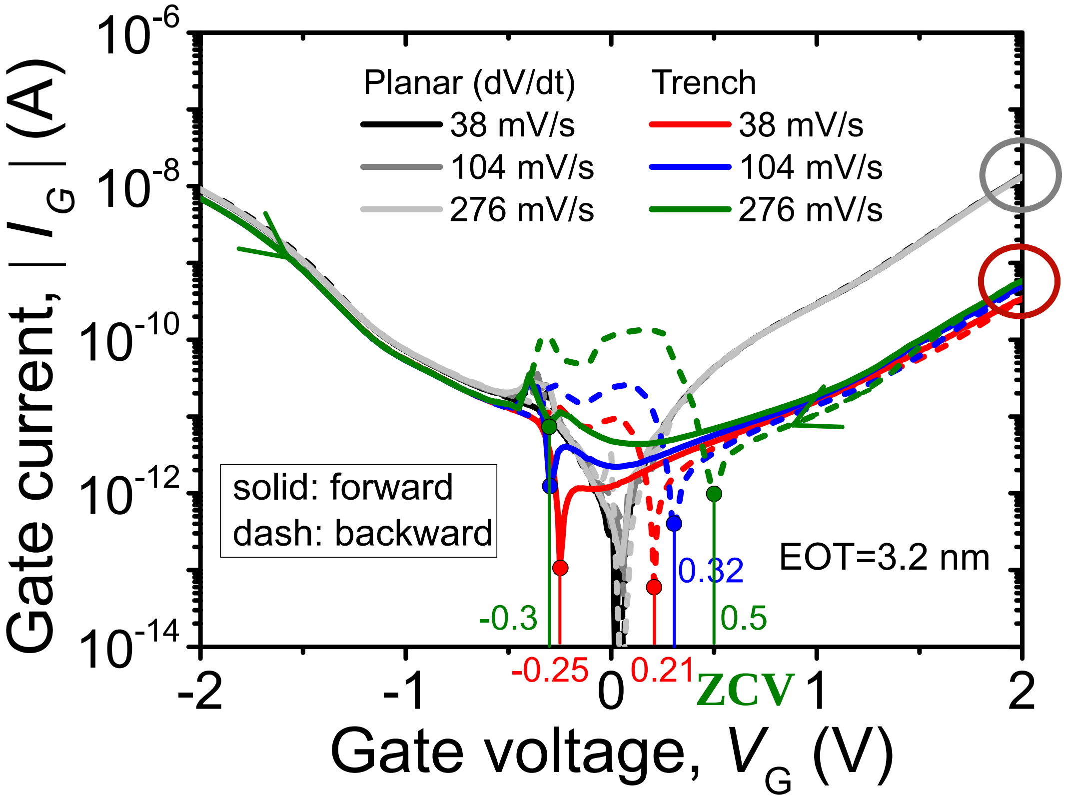
V_{ox} (V)	@ x=0 nm	@ x=6 nm
Planar	1.105	1.052
Trench	0.919	1.049

- Trench devices have **smaller edge V_{ox}.**
- However, **the bulk V_{ox} of two devices are close** since trench structure only influence the V_{ox} close to edge.

Outline

- *Introduction*
- *Experimental*
- ***Part I.*** *I–V and C–V Characteristics of Trench MIS TDs*
- ***Part II.*** ***Transient Current Behavior of Trench MIS TDs***
- ***Part III.*** *Influence of EOT on Transient Current Behavior of MIS TDs*
- *Conclusion and Future Work*

I–V Curves with Different Sweeping Rates



$$I_G = I_{cond} + I_{disp}$$

$$I_{disp} \propto \frac{dV_G}{dt}$$

Zero current voltage (ZCV): the voltage where current transits from – to + or + to – .

$V_G\ (-2 \sim +2V)$: $I_{disp} > 0$

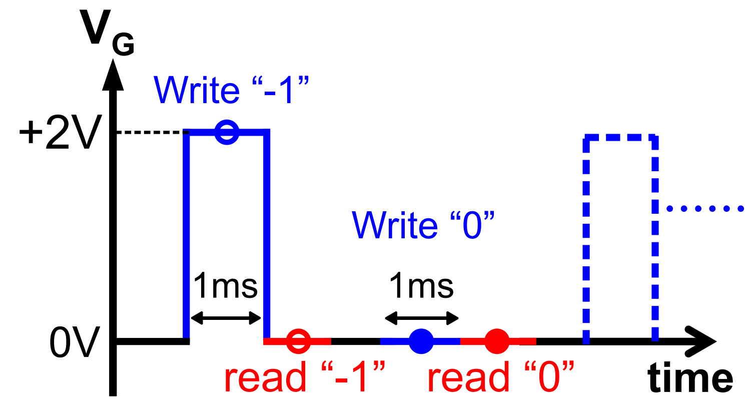
$V_G\ (+2 \sim -2V)$: $I_{disp} < 0$

- Trench devices have **stronger transient current**.
- The enhanced transient current comes from **displacement current (I_{disp})**:
  1) Hysteresis of *I–V* curves.
  2) Zero Current Voltage (ZCV) ≠ 0 V.

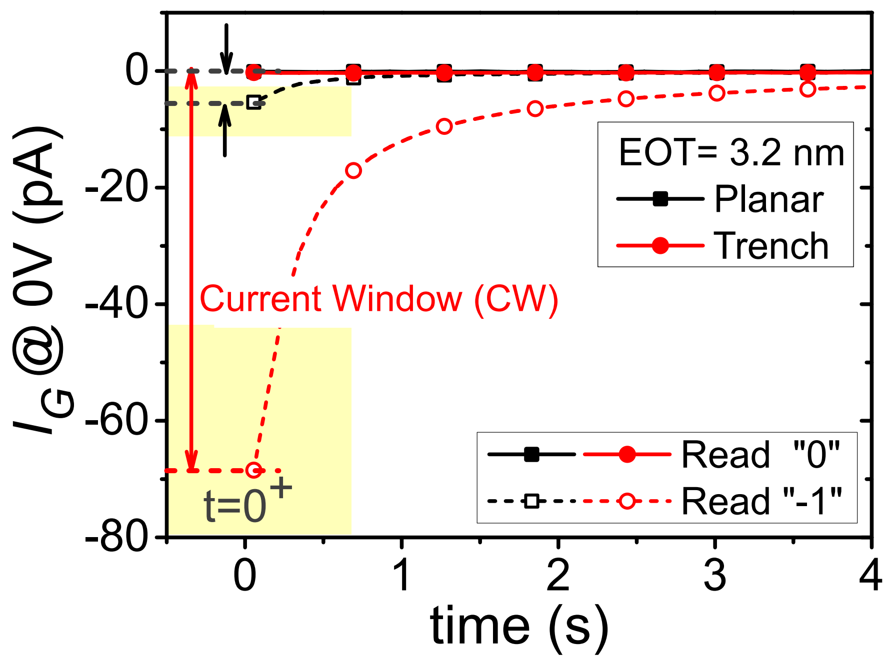
$\propto \frac{dV_G}{dt}$

Memory Measurements

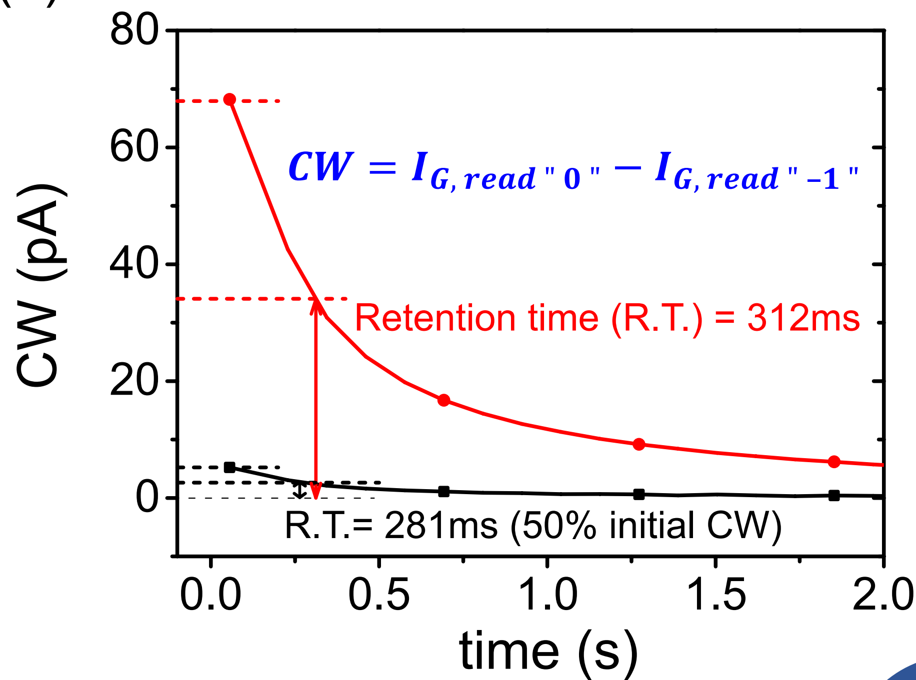
- Memory measurements are applied.
- **Write –1** to **read –1** → dV/dt ≪ 0.
- **Write 0** to **read 0** → dV/dt =0.



(a) **Memory Retention Property**



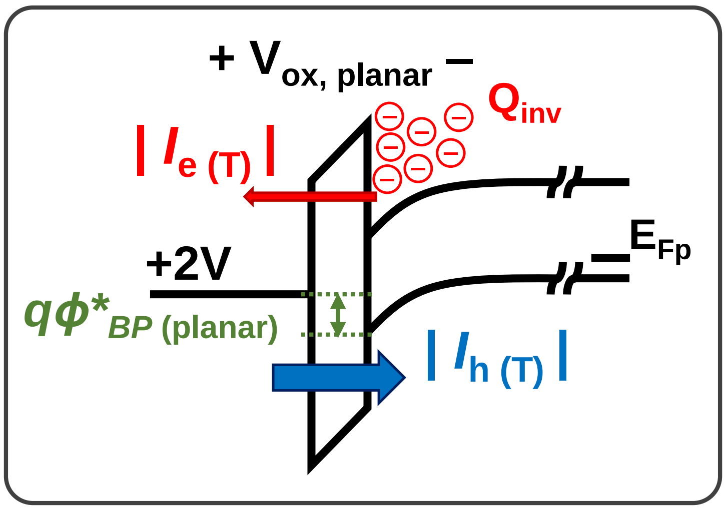
(b)



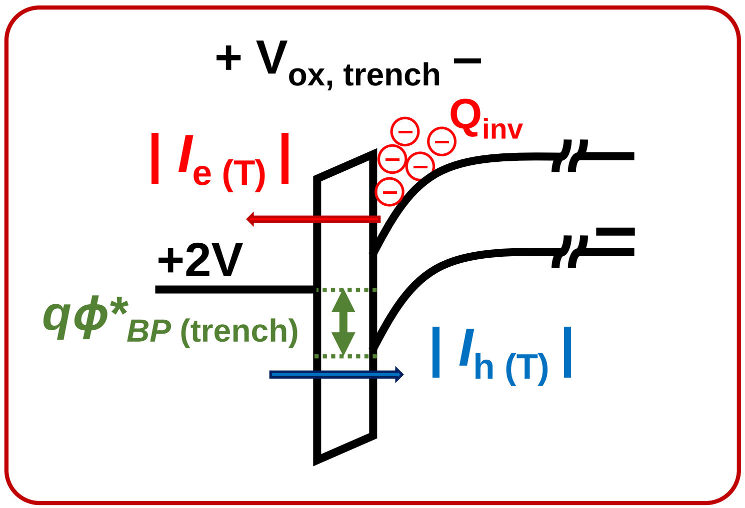
Reason for the Negative Transient Current: Thermal Equilibrium Model

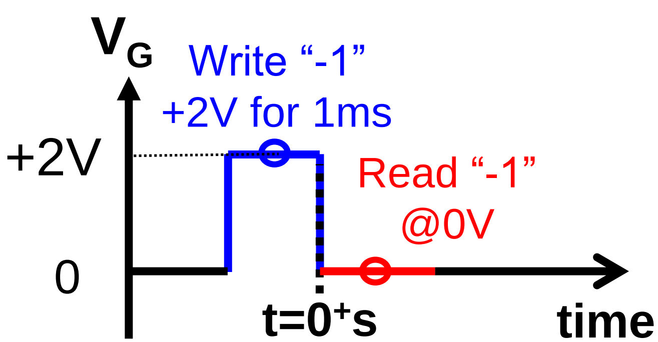
1. Write “-1” (+2V, steady-state)

Planar MIS



Trench MIS





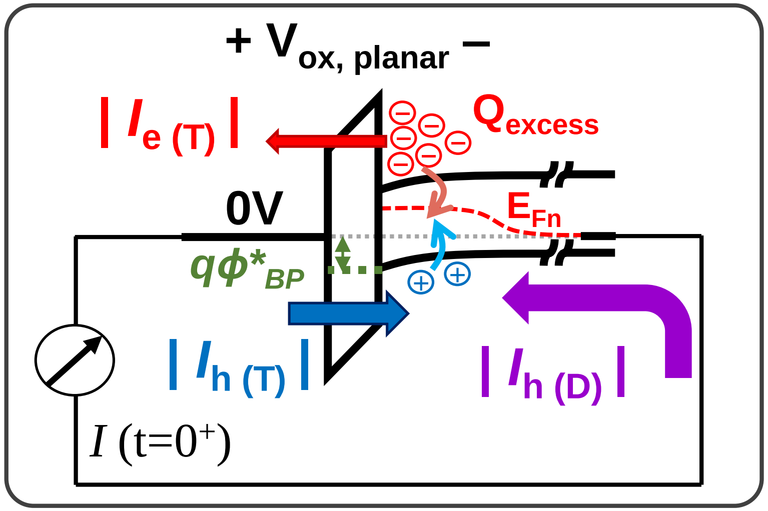
carrier flow

- At write “-1” (+2V, 1ms), many **inversion carriers accumulate** at SiO_2 / Si(p) interface.
- Planar devices have more electrons.

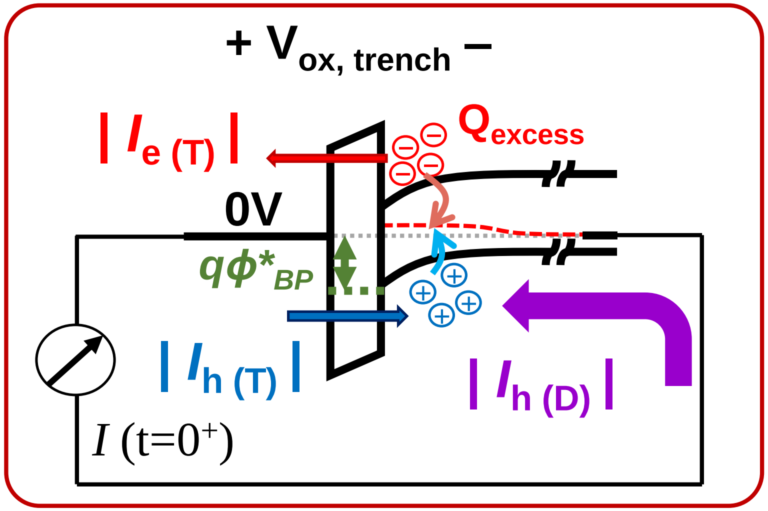
Reason for the Negative Transient Current: Thermal Equilibrium Model

2. Read "-1" @ t=0⁺s (non-equilibrium)

Planar MIS



Trench MIS



$$Q_{excess}(\text{"}-1\text{" } state) \approx Q_{inv}(@+2\ V) - Q_{inv}(@\ 0\ V)$$

e: electron
h: hole
T: tunneling
D: displacement

(1) Q_{excess} tunnel through gate oxide, $I_{e(T)}$.

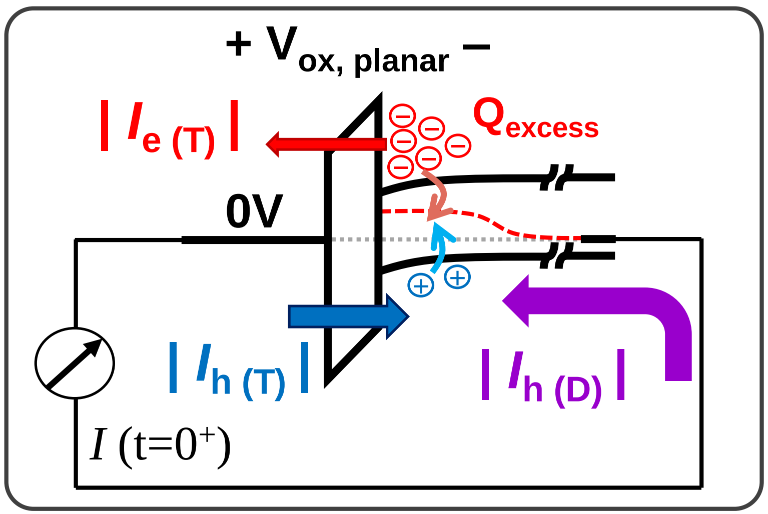
(2) Holes from gate electrode tunnel through gate oxide, $I_{h(T)}$.

(3) Hole from back gate electrode inject into the Si(p) substrate, $I_{h(D)}$.

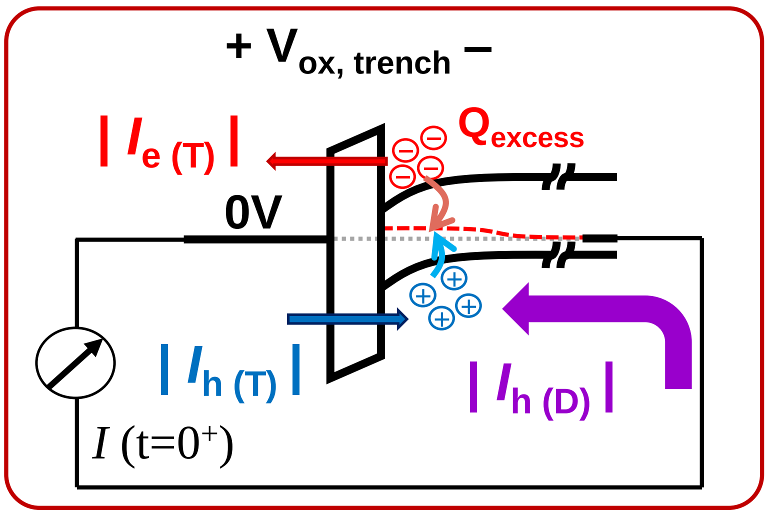
Reason for the Negative Transient Current: Thermal Equilibrium Model

2. Read "-1" @ t=0⁺s (non-equilibrium)

Planar MIS



Trench MIS



$V_{ox,\ planar} > V_{ox,\ trench}$

$|I_{e\ (T)}| + |I_{h\ (T)}|_{(planar)} \gg |I_{e\ (T)}| + |I_{h\ (T)}|_{(trench)}$

$|I_{h\ (D)}|_{(planar)} \approx |I_{h\ (D)}|_{(trench)}$

$$I_{G,\,read\,"-1"}(t) = \cancel{|I_{e(T)}(t)|} + \cancel{|I_{h(T)}(t)|} - |I_{h(D)}(t)|$$

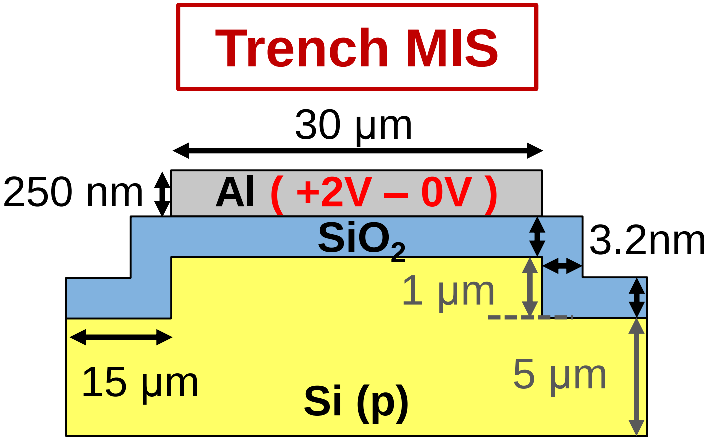
Trench devices: stronger transient current

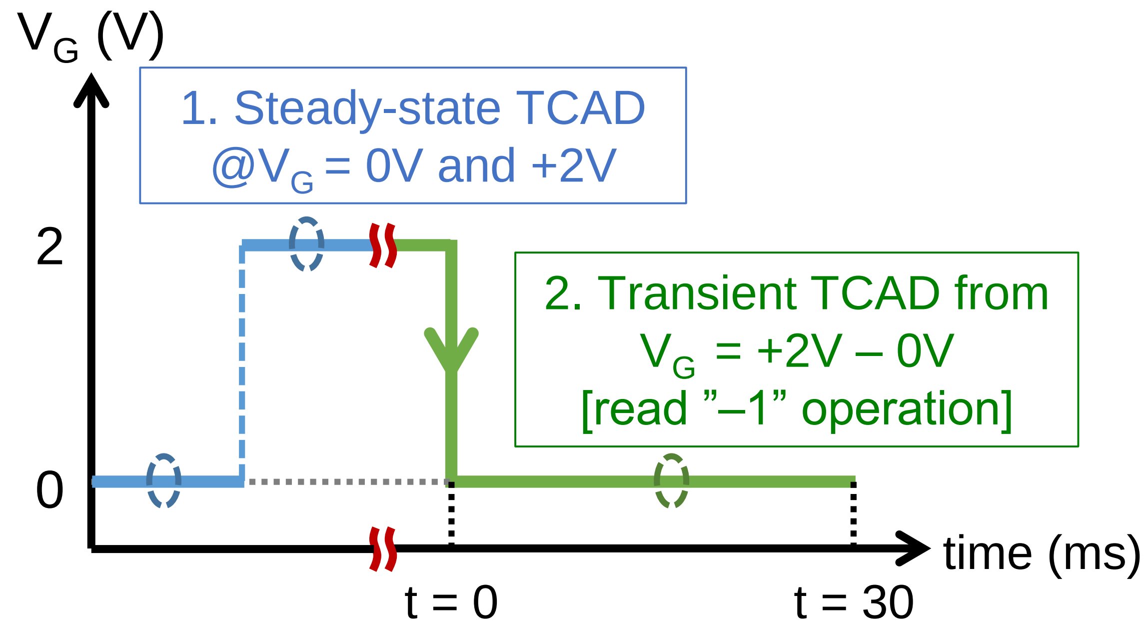
$$I_{G,\,read\,"-1"}(t = 0^+) \ll 0$$

| Transient current | ∝ | Q_{excess} |

Verification of Thermal Equilibrium Model

- **Transient TCAD Simulation**

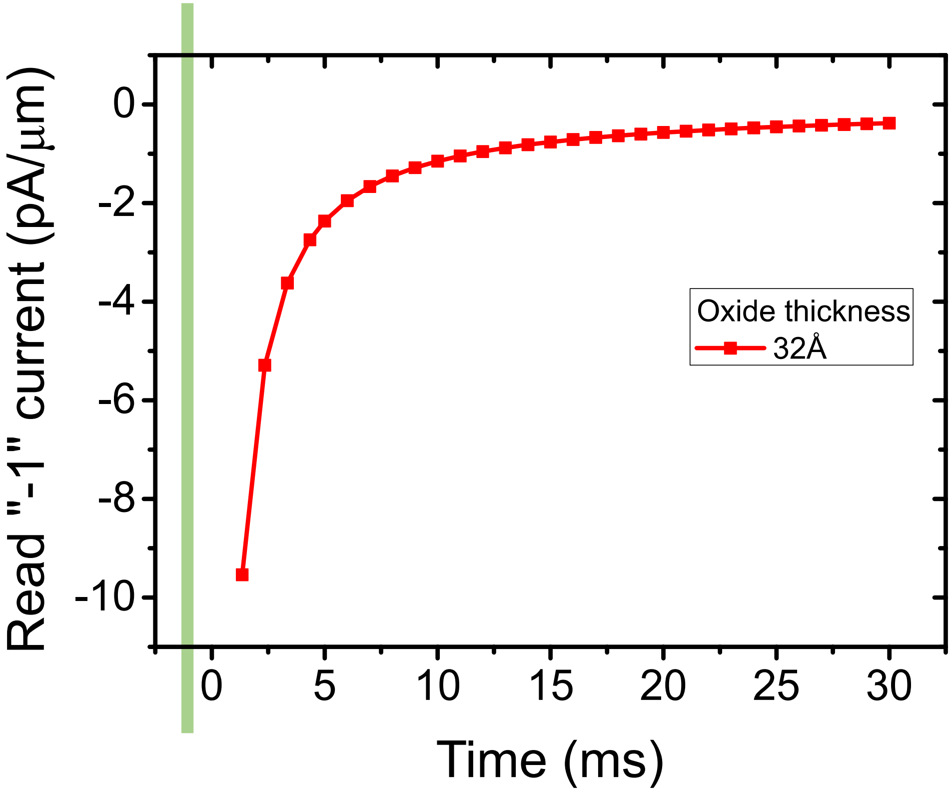




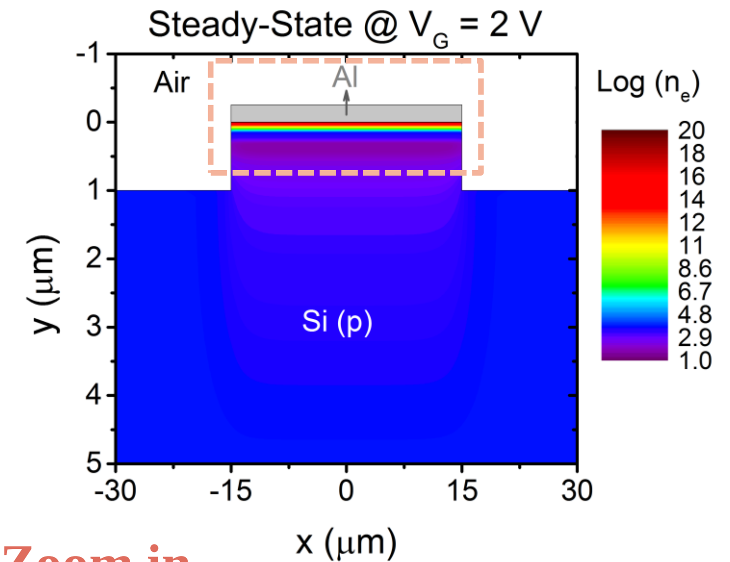
- Write "–1" (+2 V) and read "–1" (0 V) operations were simulated.
- If the proposed model is right, **transient TCAD simulation** should show:
  - **negative read "–1" transient current.**
  - and it is related to **recombination of excess carriers.**

Verification of Thermal Equilibrium Model

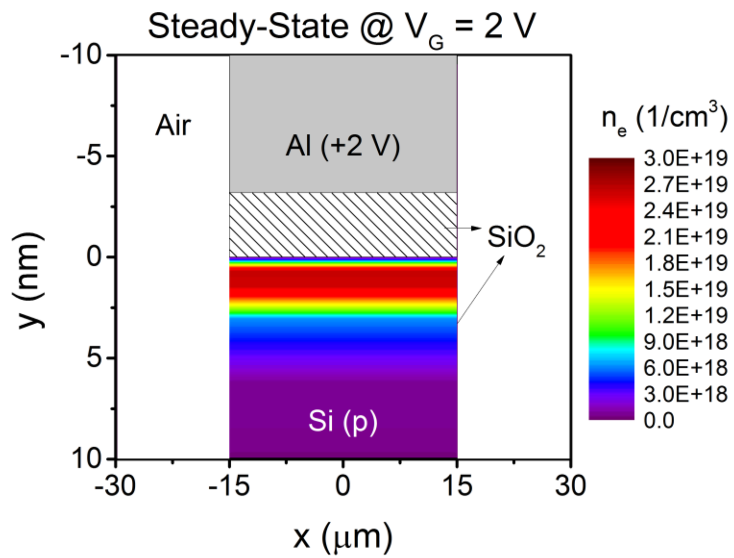
Write "–1"
t < 0 (V_G = +2 V)



Electron concentration (n_e)



Zoom in

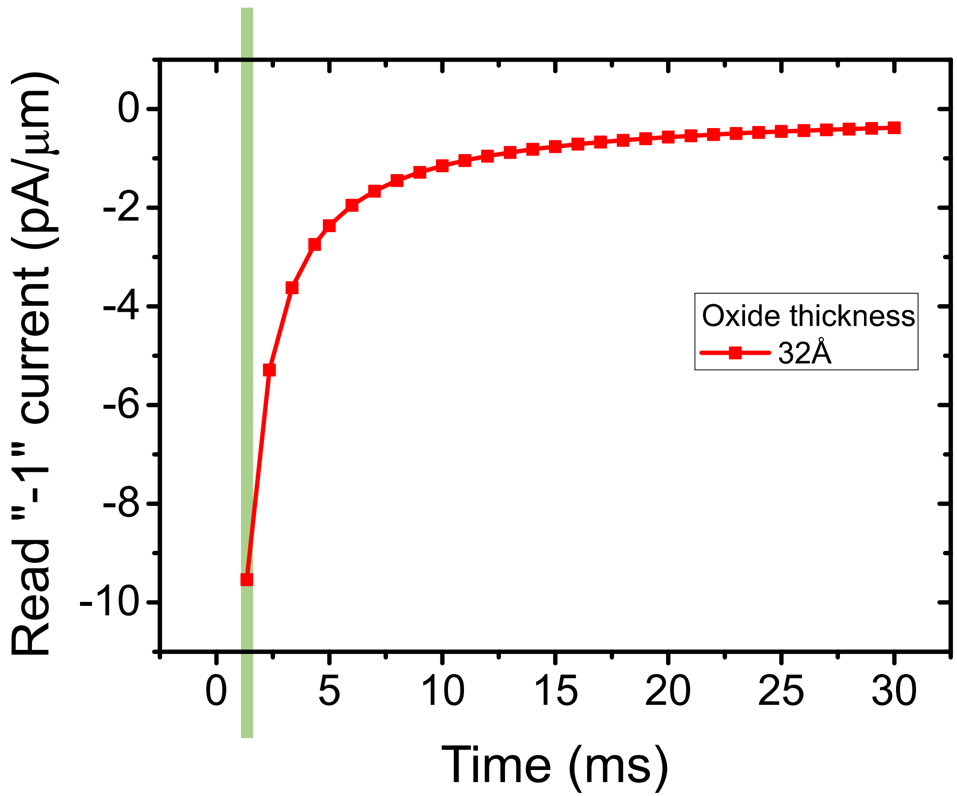


- Steady-state solution @ 2 V was solved first. [write "–1"]

Verification of Thermal Equilibrium Model

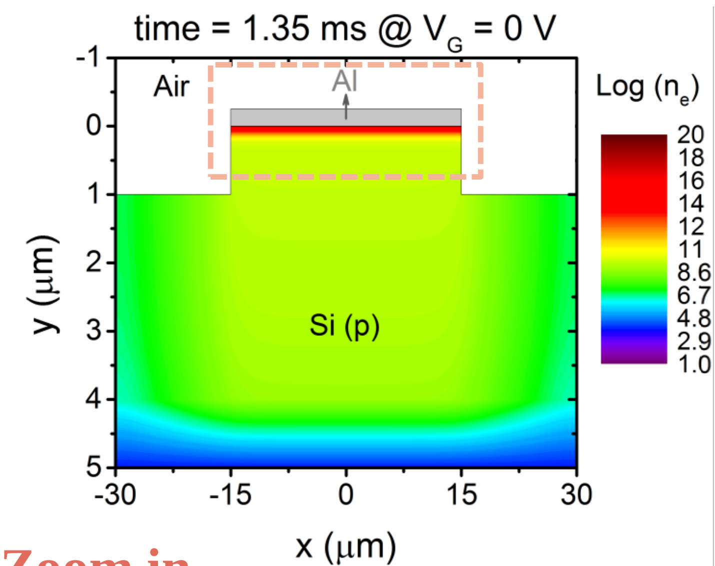
Read “–1”

t = 1.35 ms (V_G = 0 V)

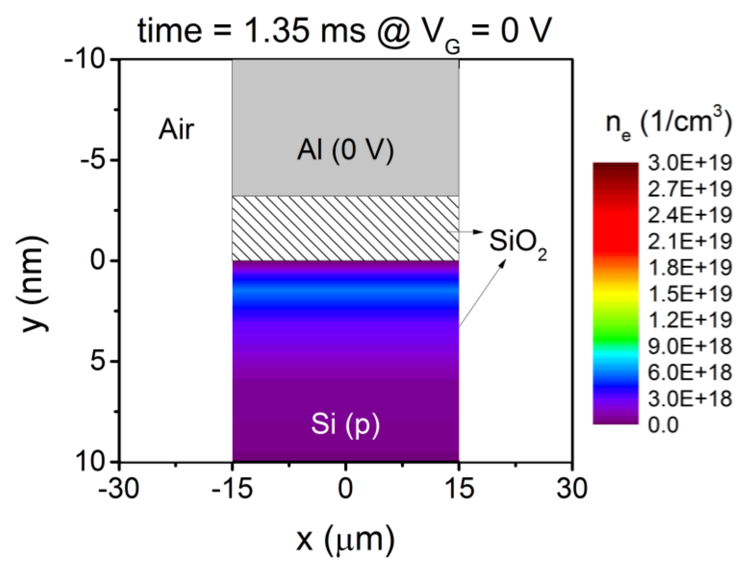


- There are **excess carriers** at the beginning of read “–1”.

Electron concentration (n_e)



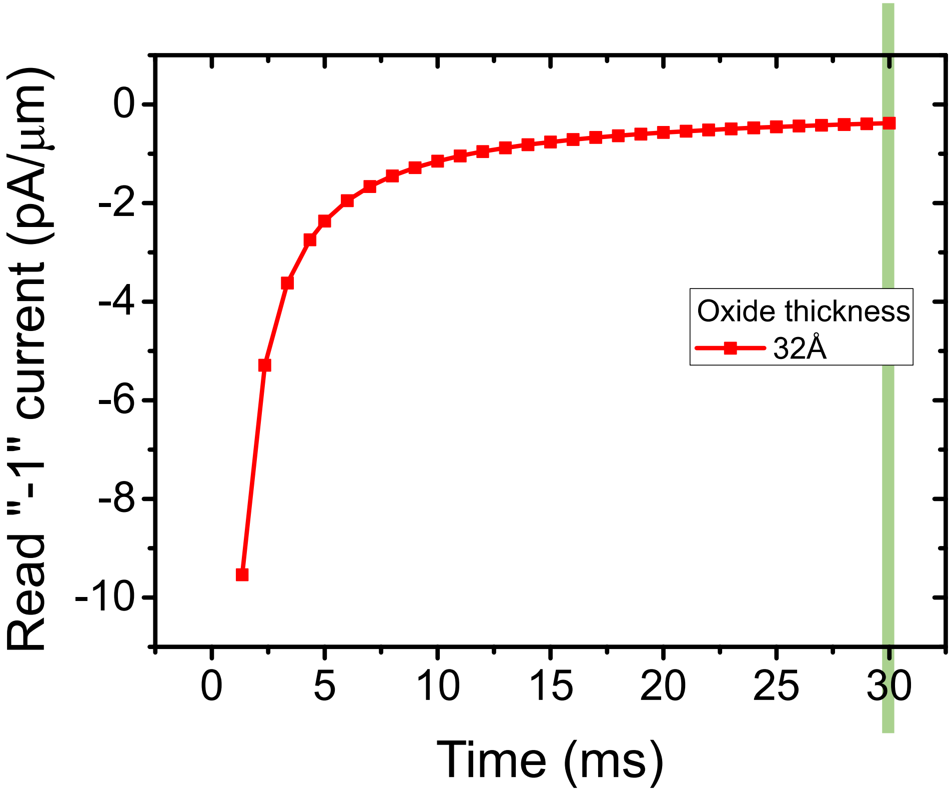
Zoom in



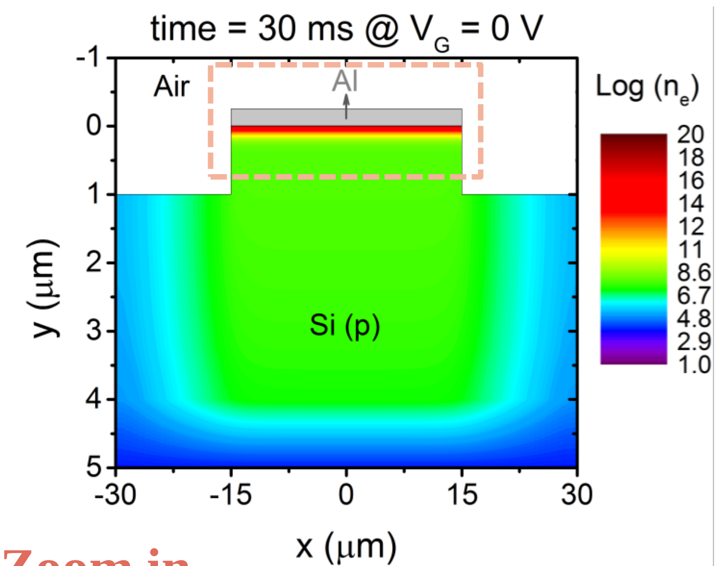
SILVACO

Verification of Thermal Equilibrium Model

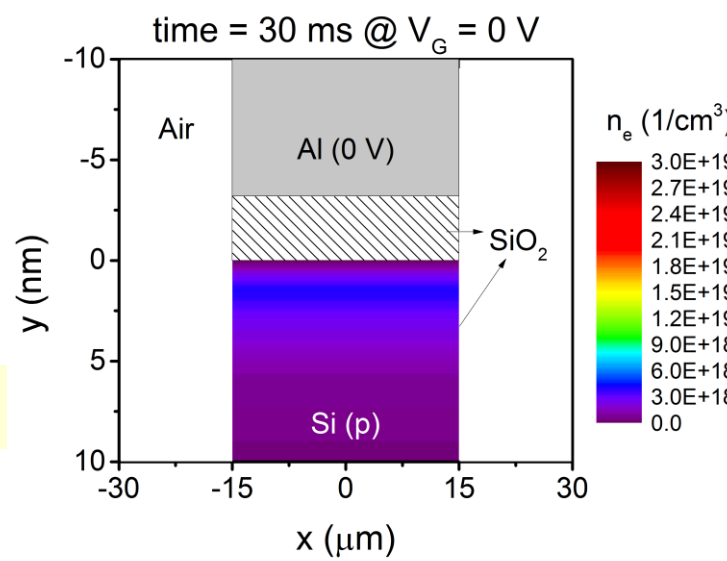
Read "–1"
t = 30 ms (V_G = 0 V)



Electron concentration (n_e)

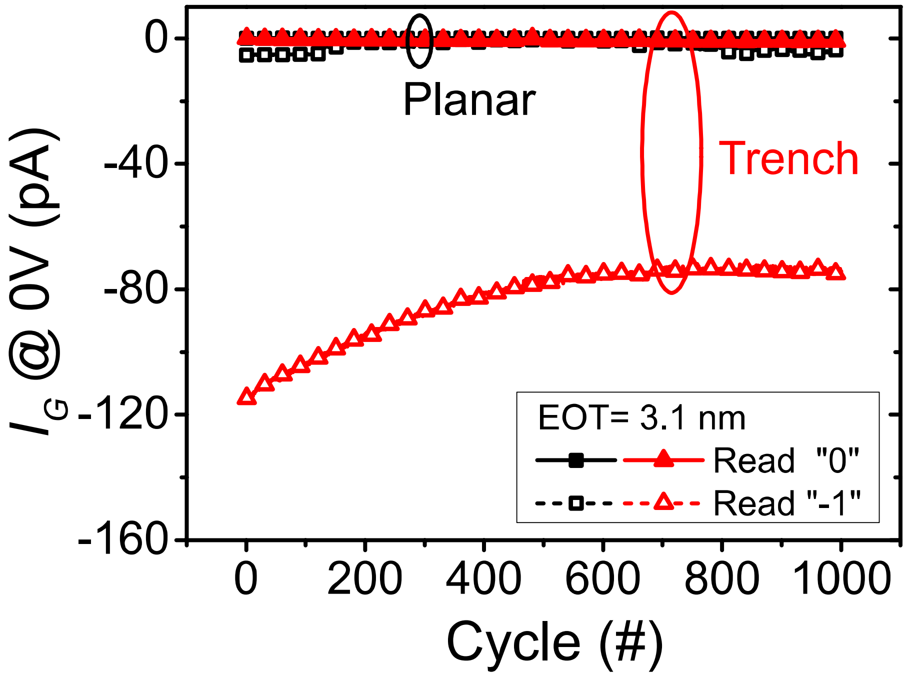


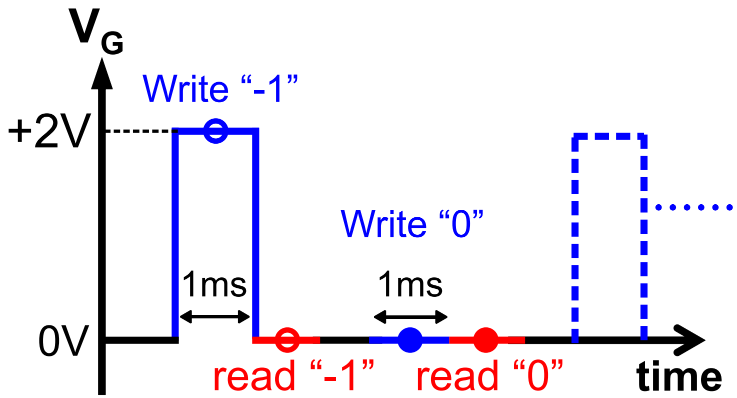
Zoom in



- Excess carriers are gradually recombined.

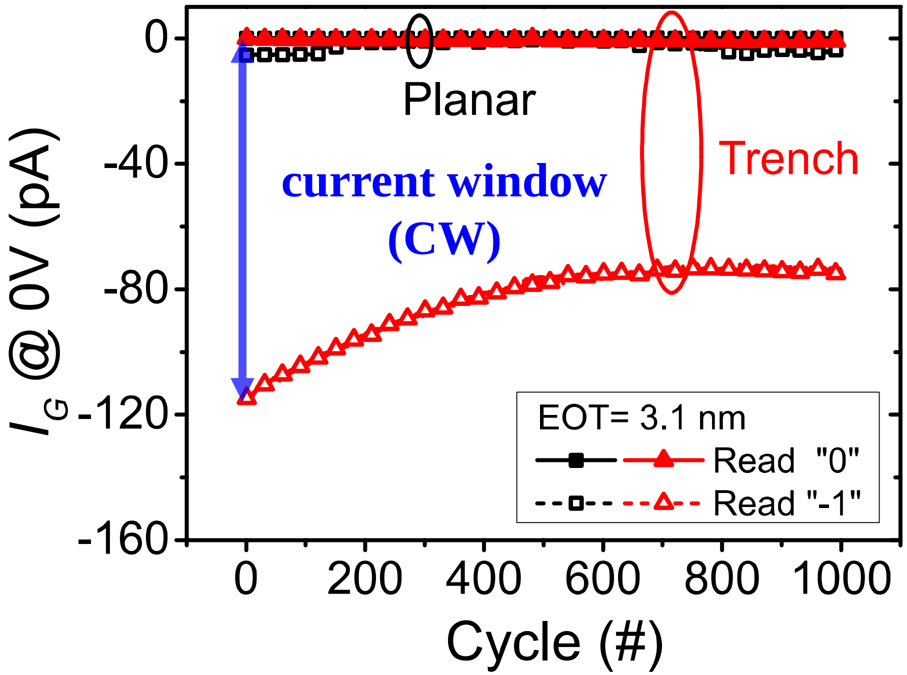
Memory Endurance Characteristics

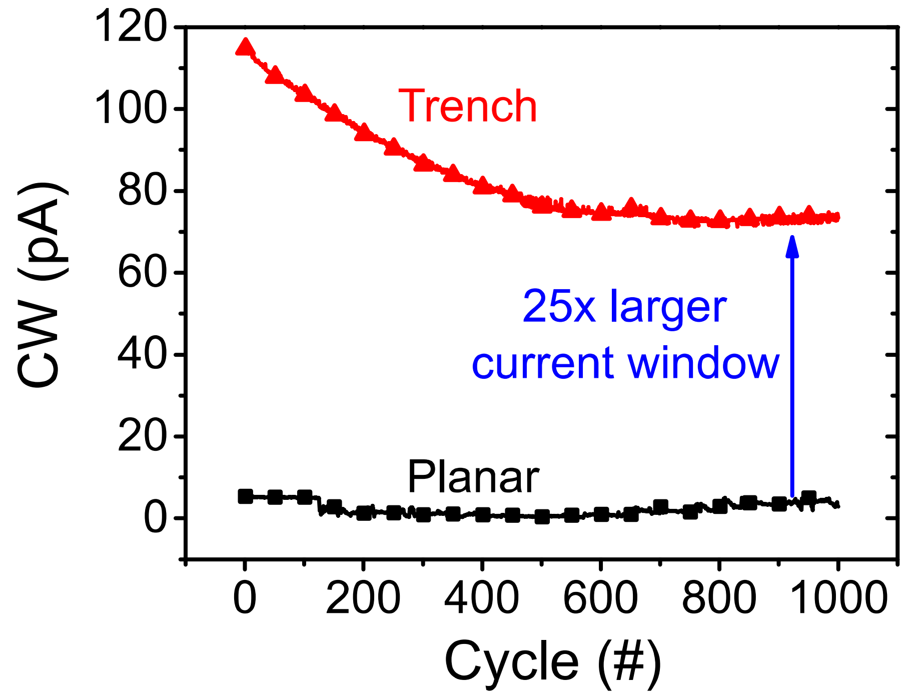




$$I_{G,read\,"-1"}(t) = |I_{e(T)}(t)| + |I_{h(T)}(t)| - |I_{h(D)}(t)|$$

Memory Endurance Characteristics





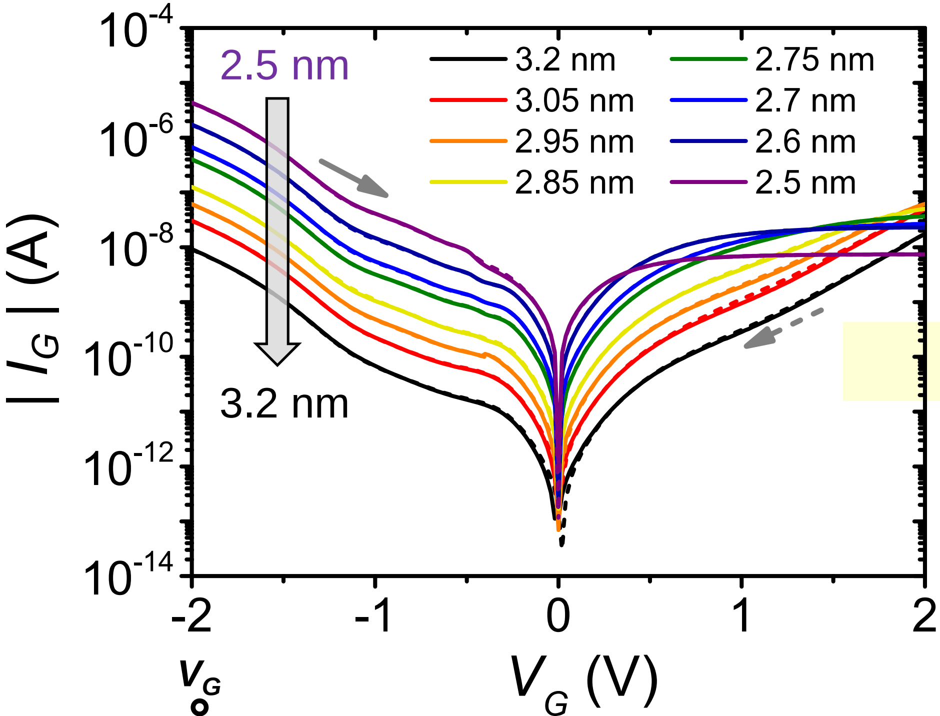
$$I_{G,read\,"-1"}(t) = |I_{e(T)}(t)| + |I_{h(T)}(t)| - |I_{h(D)}(t)|$$

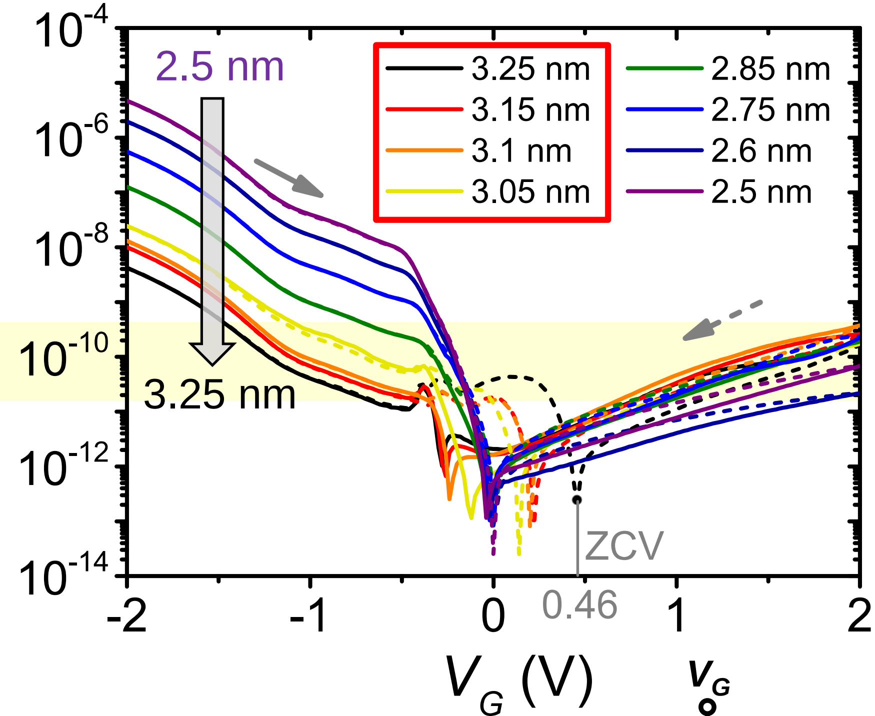
- **Trench MIS has 25 times larger CW** (73.4 pA) than the planar device (2.9 pA).
- The decay of CW as the cycle increases:
  - ➢ interface trap density (D_{it}) at SiO_2 / Si(p) interface and at trench sidewall ↑.
  - ➢ Q_{excess} ↓, CW ↓.

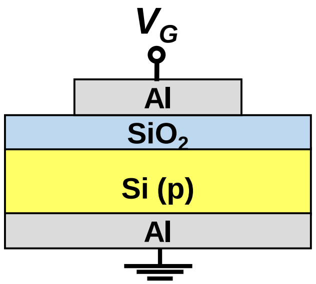
Outline

- *Introduction*
- *Experimental*
- ***Part I.** I–V and C–V Characteristics of Trench MIS TDs*
- ***Part II.** Transient Current Behavior of Trench MIS TDs*
- ***Part III.** Influence of EOT on Transient Current Behavior of MIS TDs*
- *Conclusion and Future Work*

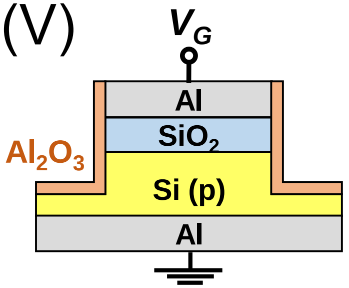
I–V Curves with Different EOTs



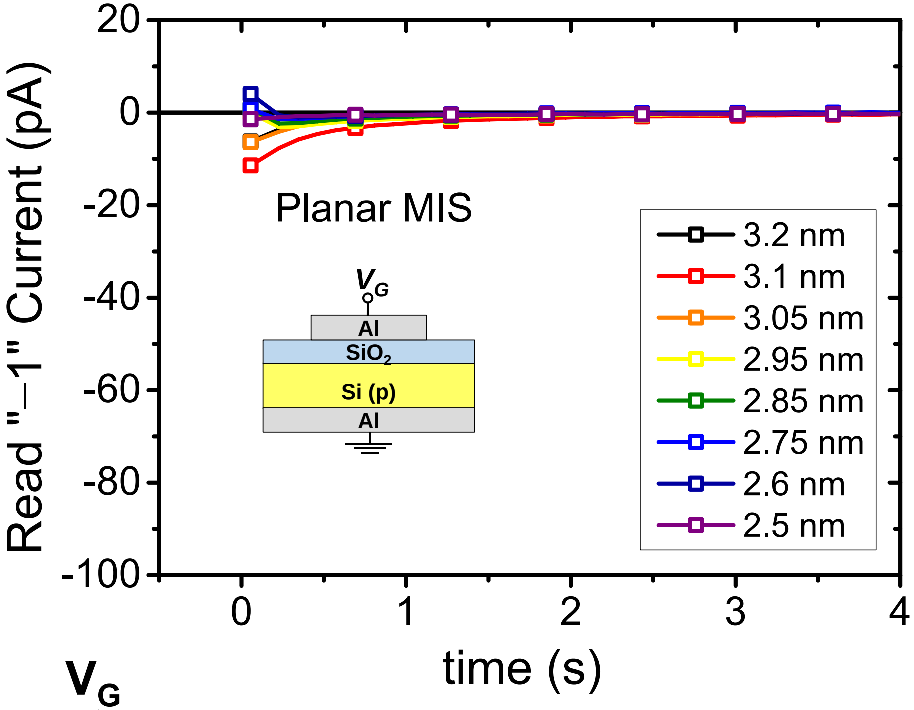


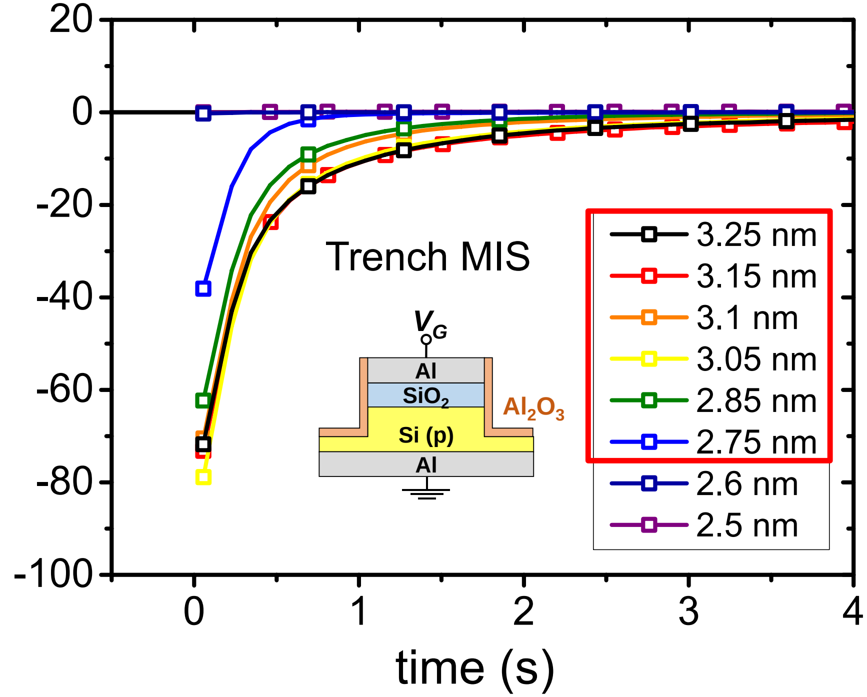


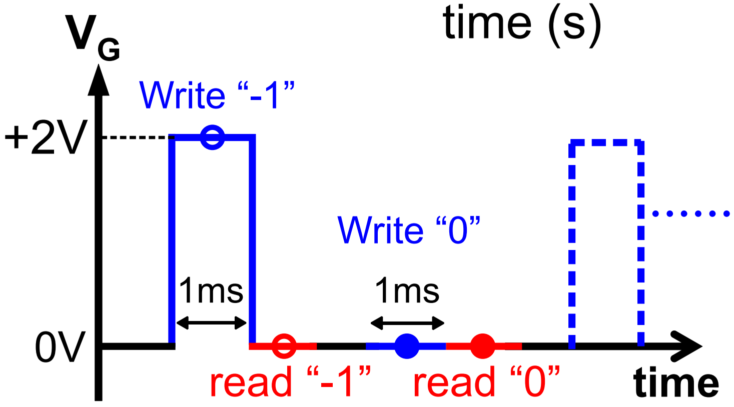
- Trench MIS TDs:
  - ➢ **Smaller reverse bias current** at all EOTs.
  - ➢ **Strong transient current at thicker EOTs (3.25–3.05 nm).**



Read “–1” Current with Different EOTs

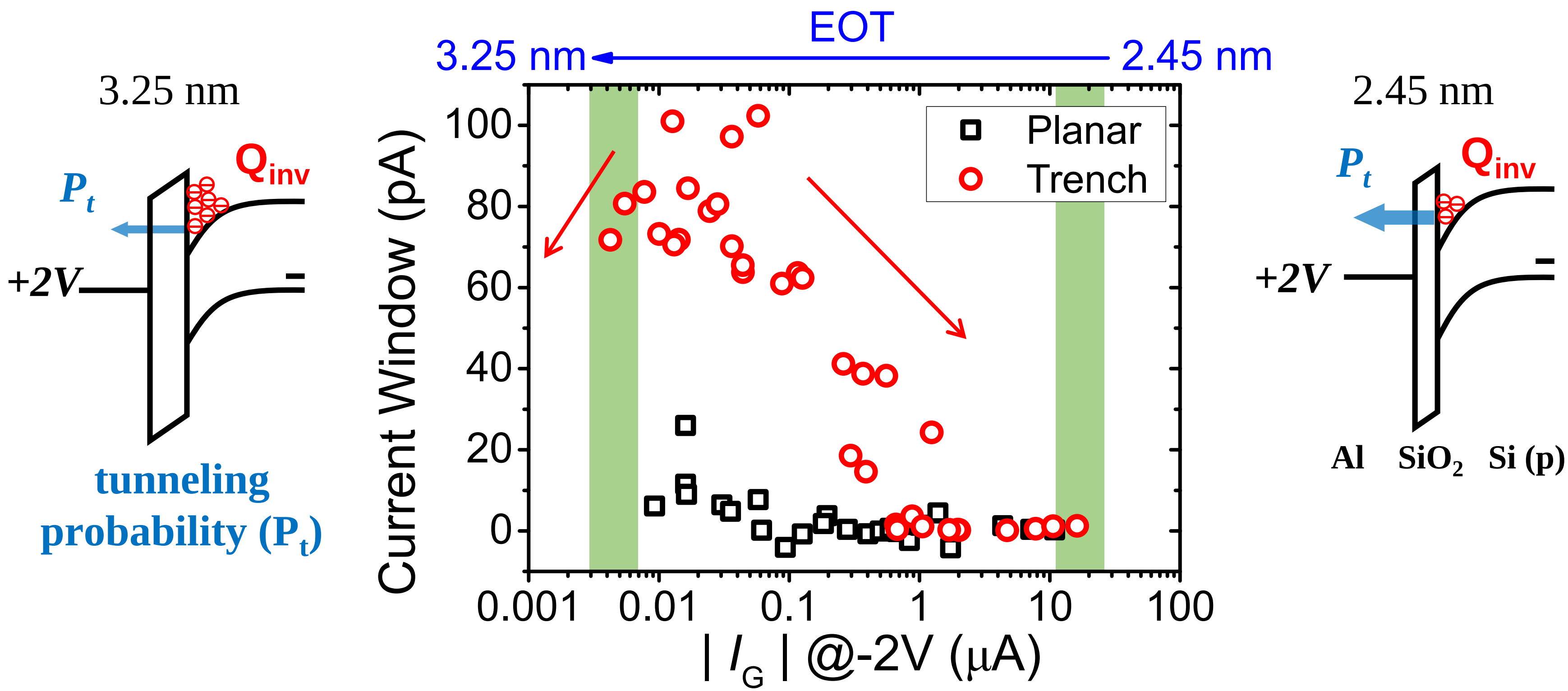






- Read “0” current are not shown for simplicity since they are all close to zero.
- Trench devices show **enhanced transient current only when EOTs are thick enough (≥ 2.75 nm).**

Current Window with Different EOTs



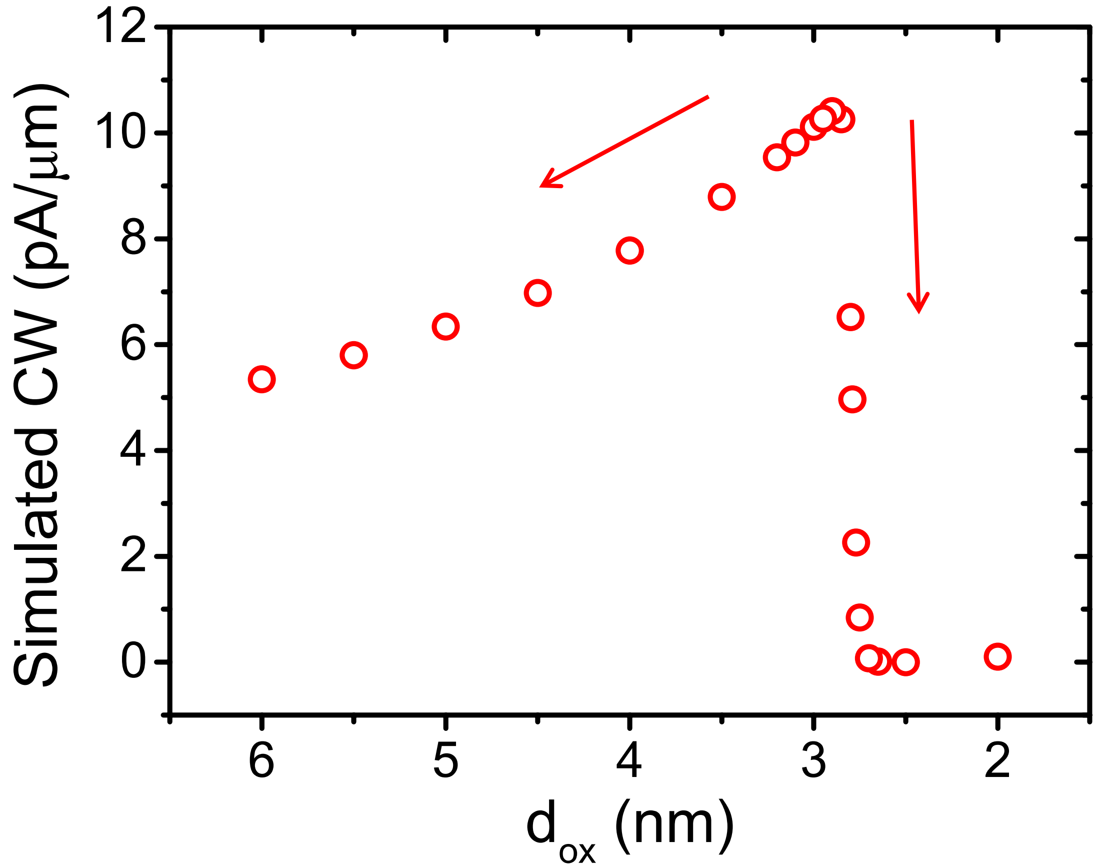
$$CW = I_{G,read\,"0"} - I_{G,read\,"-1"} \approx -I_{G,read\,"-1"}$$

- CW is related to the number of excess carriers (Q_{excess}) .
- $Q_{excess} \propto Q_{inv}$ @+2V.

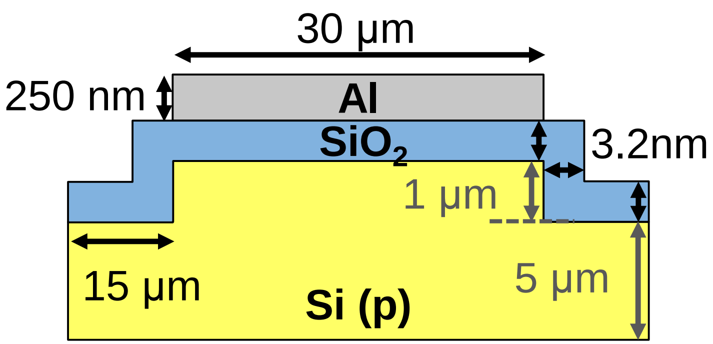
➢ EOT ↓, P_t ↑, Q_{inv} @+2V ↓, $\mathbf{Q_{excess}}$ ↓, CW ↓.

➢ EOT ↑, C_{ox} ↓, Q_{inv} @+2V ↓, $\mathbf{Q_{excess}}$ ↓, CW ↓.

Simulated CW under Various EOTs

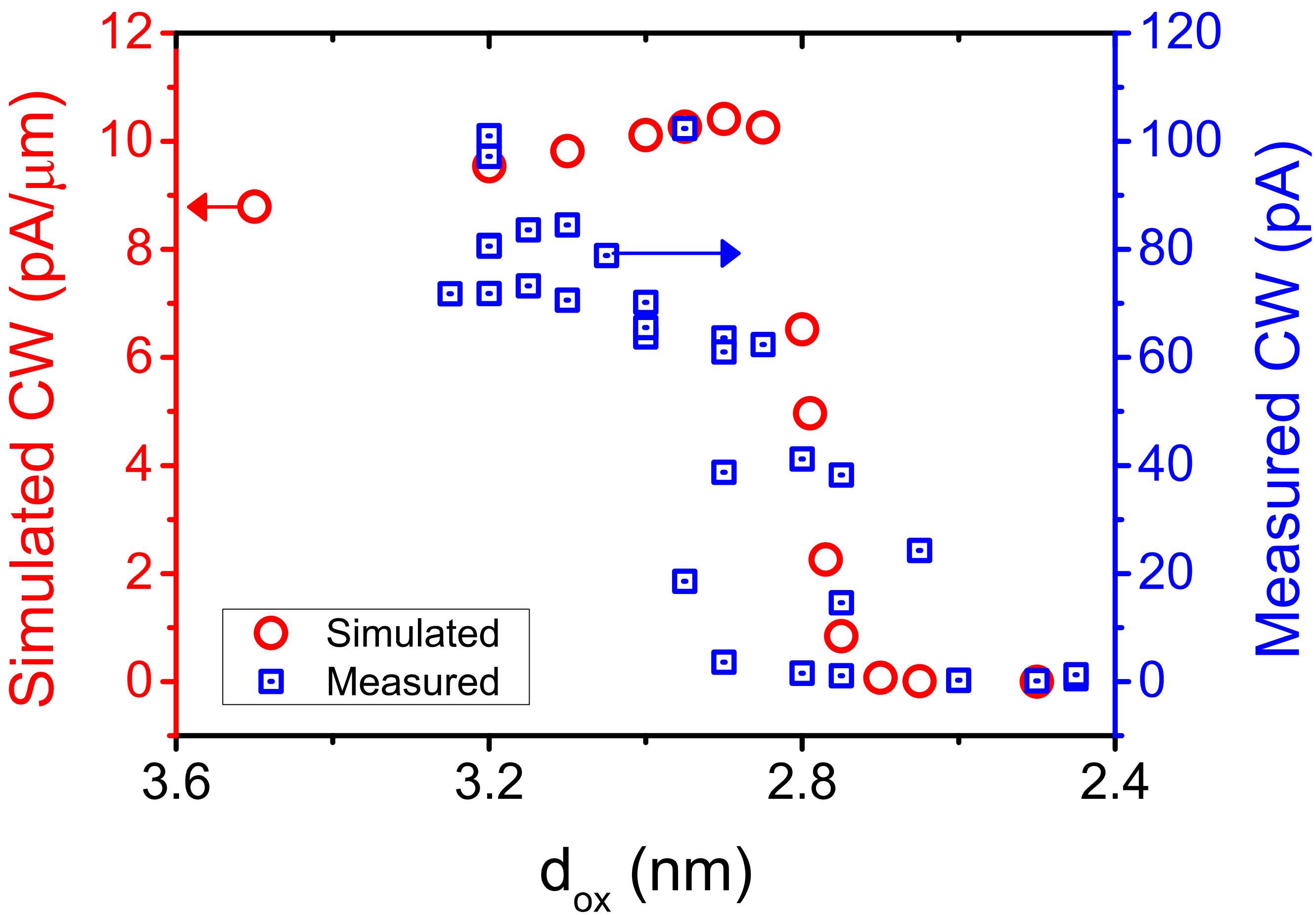


Trench MIS



<u>Transient TCAD simulation</u> shows the **maximum CW** at specific oxide range because of the **maximum Q_{excess}**.

Simulated CW under Various EOTs



● **Simulation data** is similar to the trend of **experimental results.**

Outline

- *Introduction*
- *Experimental*
- *Part I.* *I–V and C–V Characteristics of Trench MIS TDs*
- *Part II.* *Transient Current Behavior of Trench MIS TDs*
- *Part III.* *Influence of EOT on Transient Current Behavior of MIS TDs*
- ***Conclusion and Future Work***

Conclusion

- The thesis propose a new structure of MIS TDs: **Trench MIS TDs.**

- Different from conventional Planar MIS TDs, Trench devices have:

  1) Lower reverse bias current (because of insufficient e^- supply).

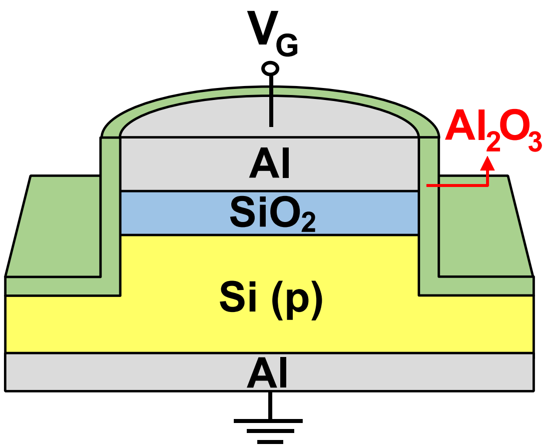
  2) Enhanced transient current behavior at thicker EOTs ($\geq$ 2.75 nm).

- Utilizing the **stronger transient current behavior (e.g. 25x larger CW),** Trench MIS TDs may find their use in **memory applications.**

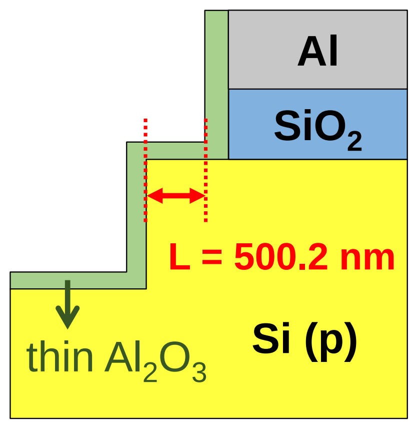
Suggestions for Future Work

1. **Study of distance between gate edge and trench edge.**

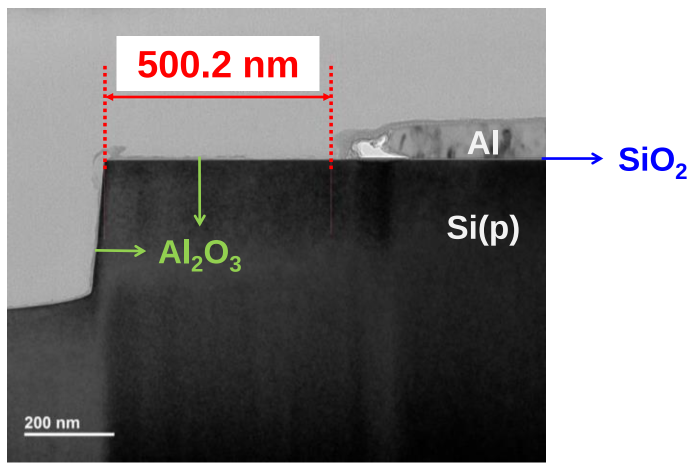
Ideal case



(a)

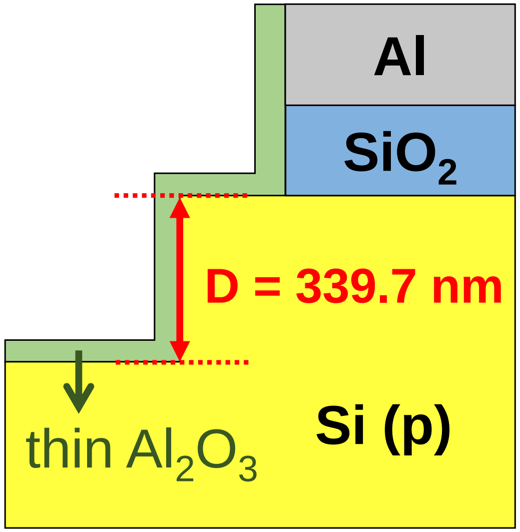


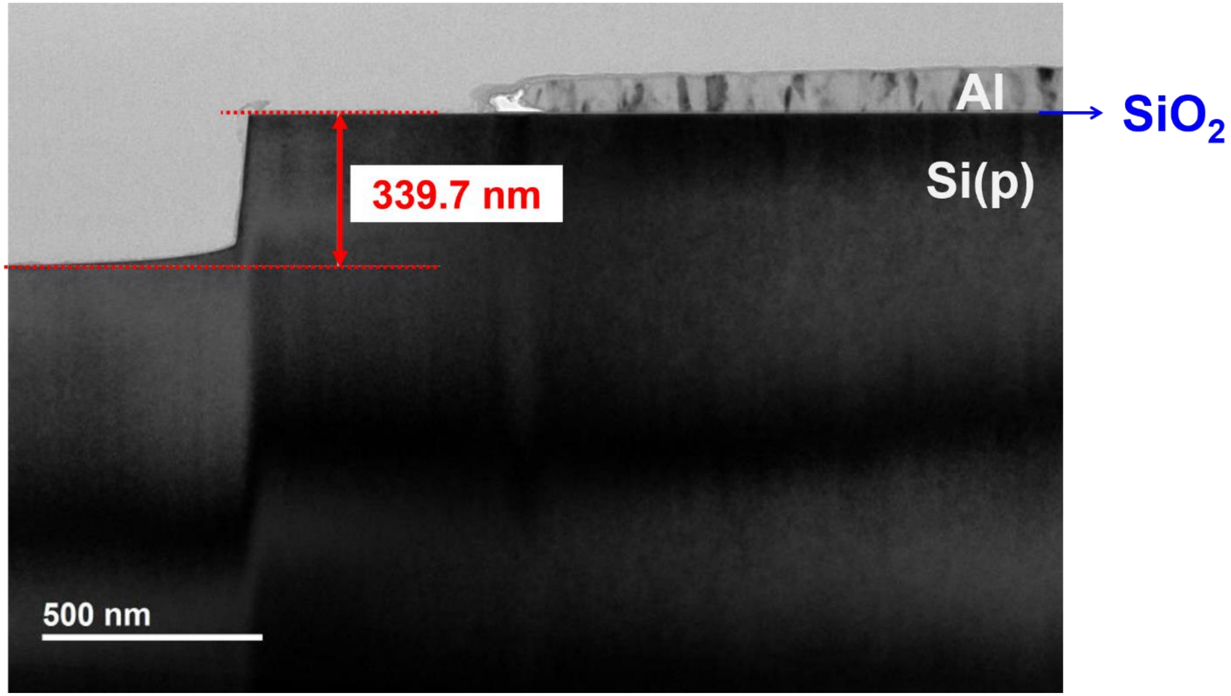
(b)



Suggestions for Future Work

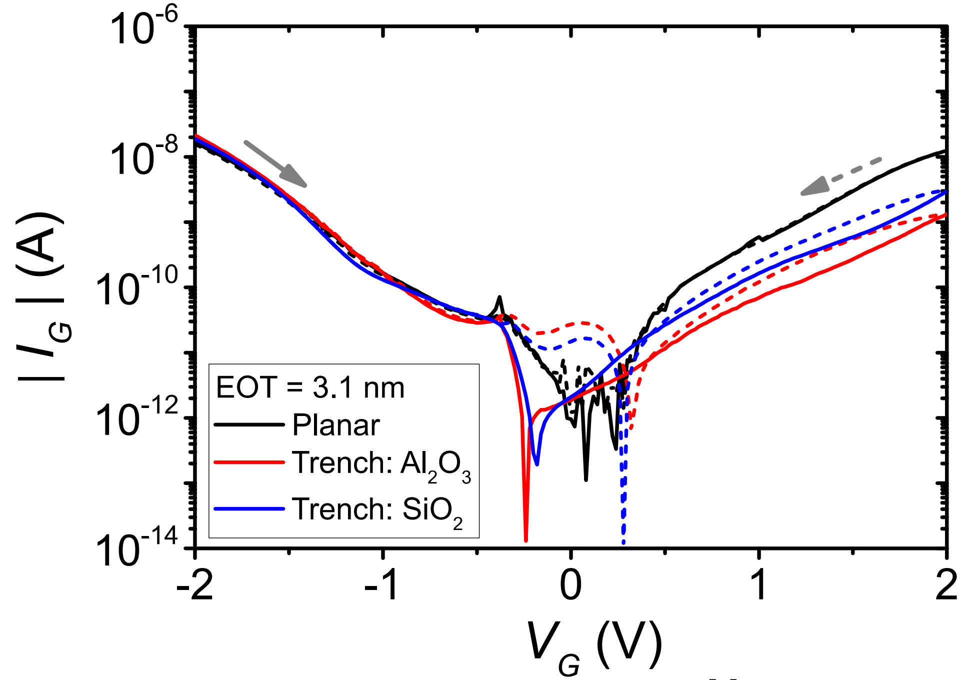
2. The depth of trench structure.

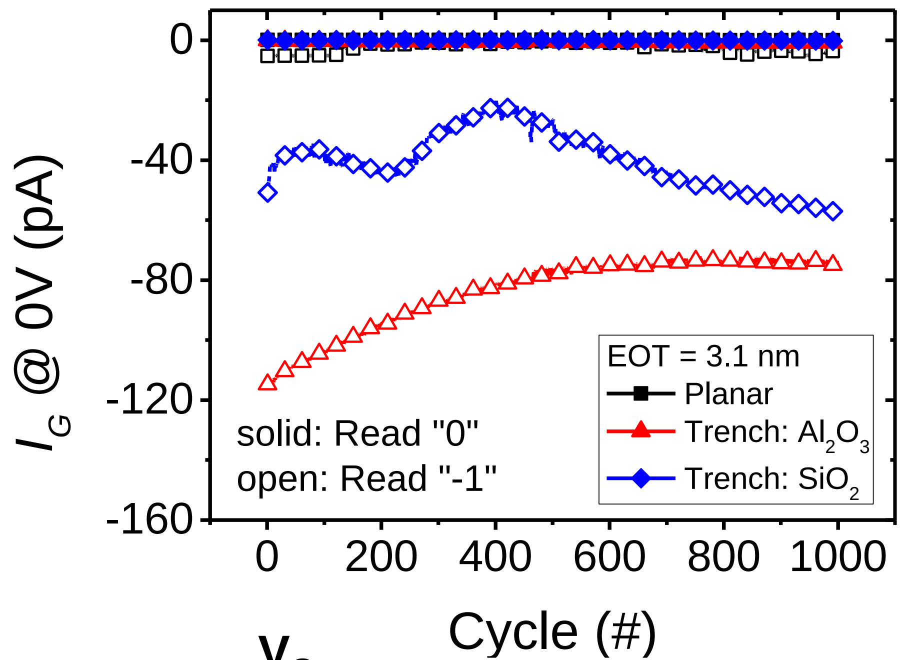


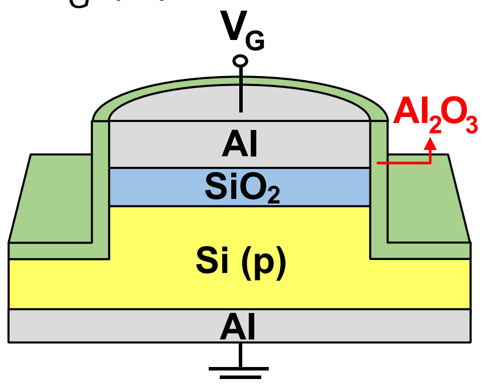


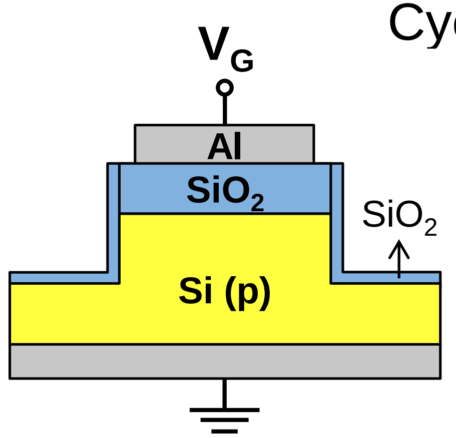
Suggestions for Future Work

3. Different sidewall materials.









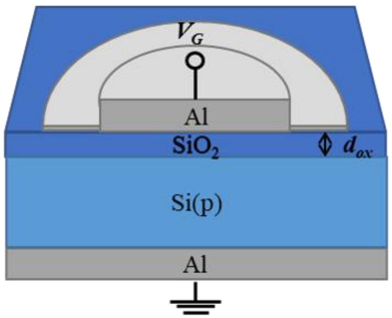
Thank you for listening!

Presenter: Jian-Yu Lin (林建宇)

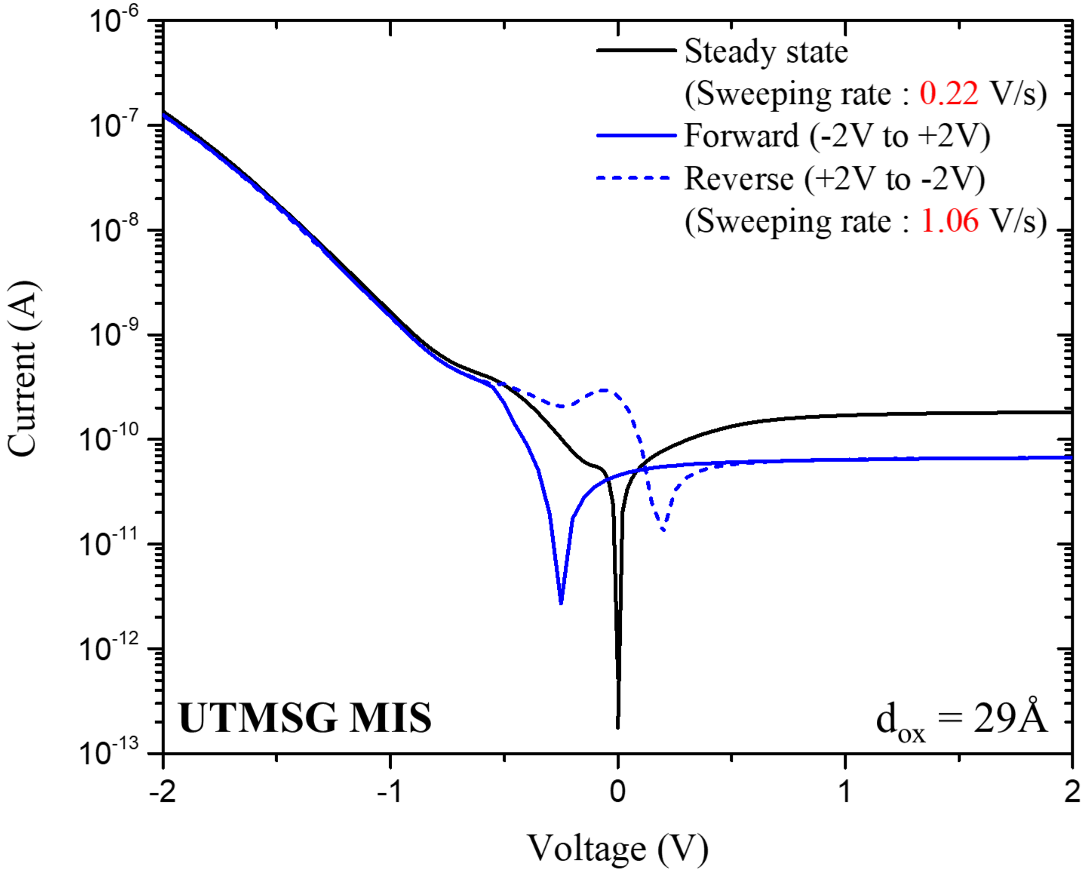
Backup

UTMSG MIS

Special structure

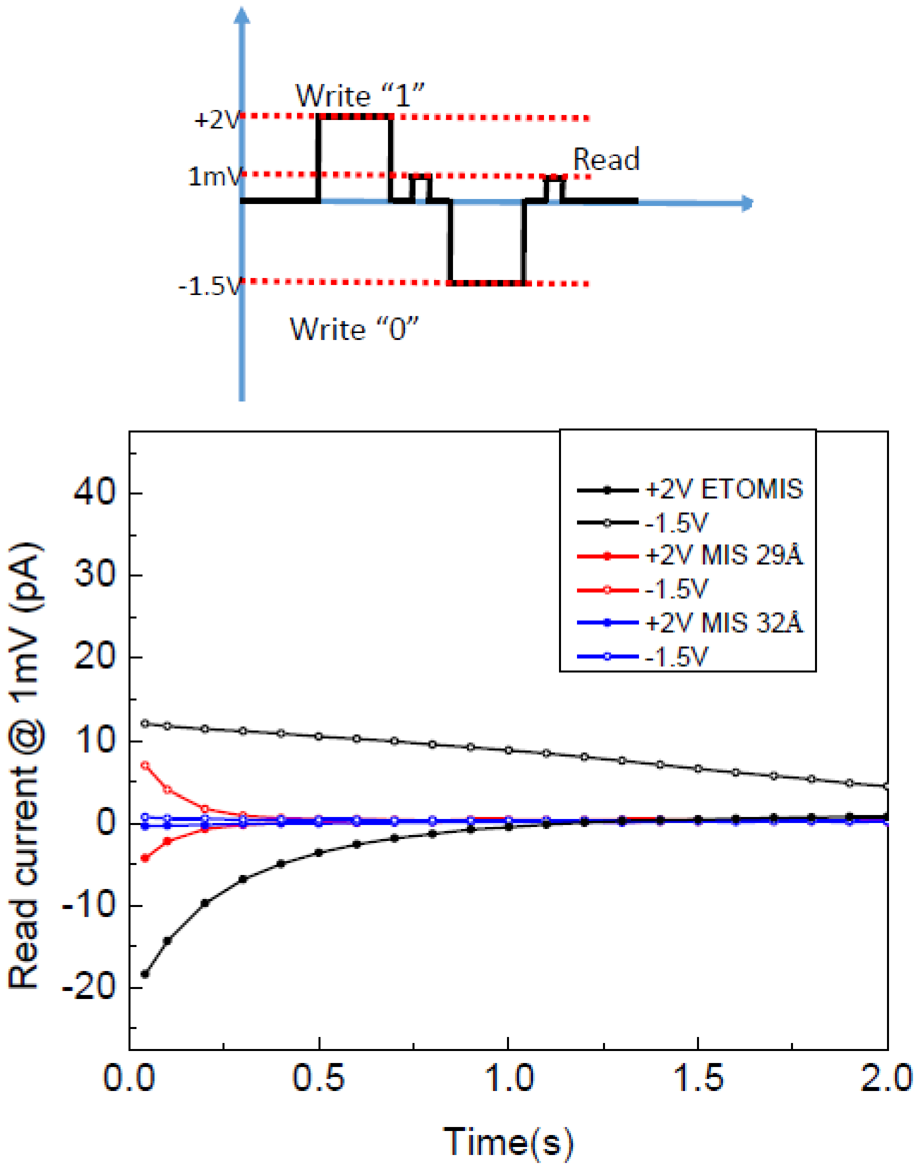


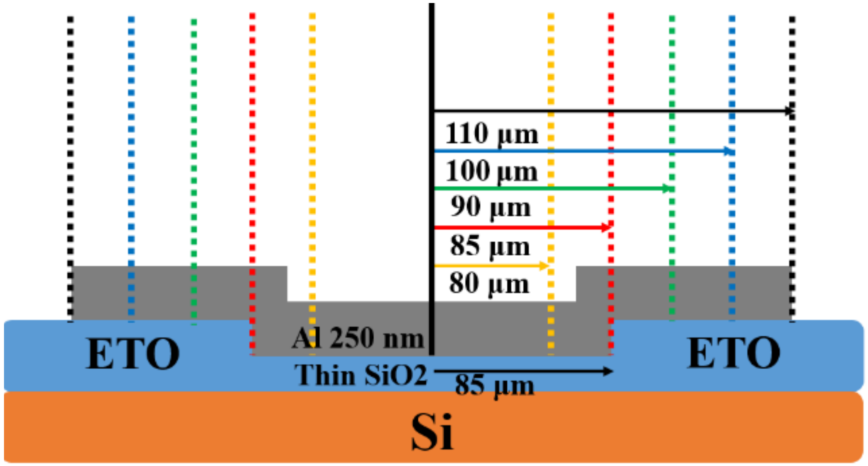
UTMSG MIS
(ultrathin metal surrounded gate) MIS



C.F.Cheng, et al., ECS Journal of Solid State Science and Technology, Vol.8, No.12, December, PP. N214-N219, doi: 10.1149/2.0191912jss.

Edge-Thickened Oxide (ETO) MIS

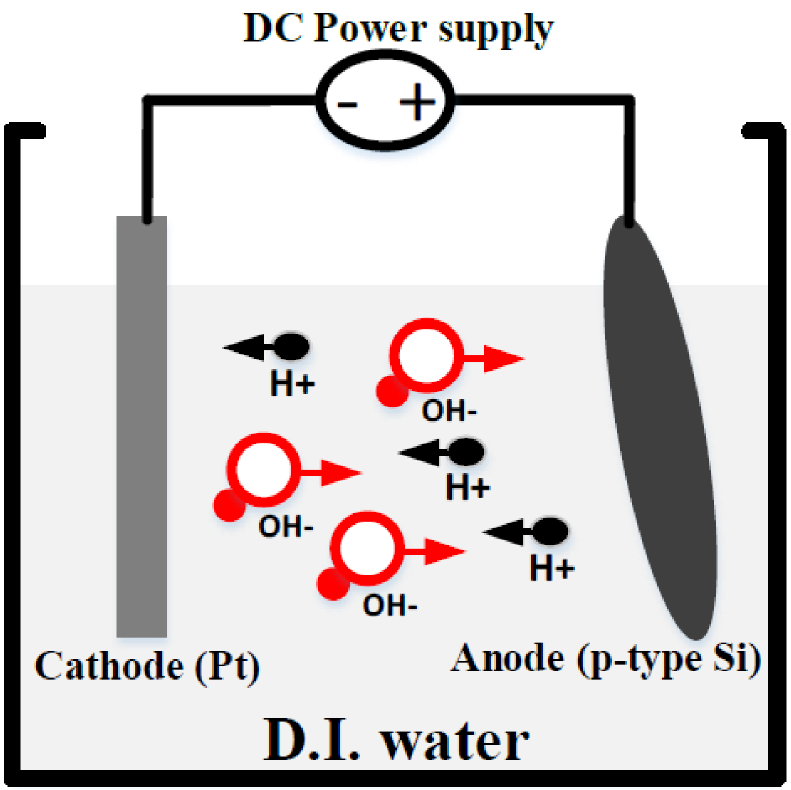




ETO MIS

Y.-C. Yang, et al., ECS Journal of Solid State Science and Technology, vol. 9, no. 10, p. 103006, 2020/11/03 2020, doi: 10.1149/2162-8777/abc576.

Anodic Oxidation (ANO) System



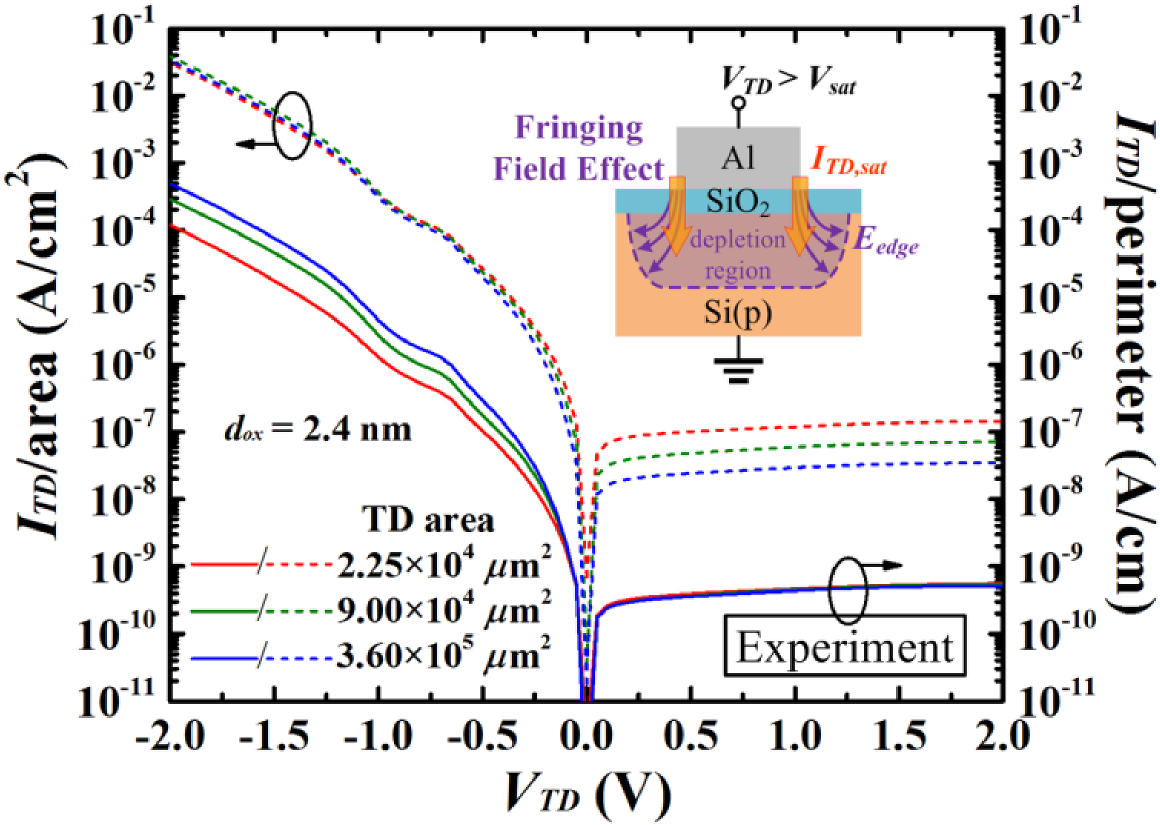
$$Si_{(s)} + 2OH^{-}_{(aq)} \rightarrow SiO_{2(s)} + 2H^{+}_{(aq)} + 4e^{-}$$

$$4H^{+}_{(aq)} + 4e^{-} \rightarrow 2H_{2(g)}$$

$$Si_{(s)} + 2H_2O_{(l)} \rightarrow SiO_{2(s)} + 2H_{2(g)}$$

Jun-Yao Chen, “Effect of Compensatory Embedded Aluminum on the Electrical Characteristics of MIS Tunnel Diode with Ultrathin Oxide” Master thesis, Graduate Institute of Electronics Engineering, College of Electrical Engineering and Computer Science, National Taiwan University 2016.

Perimeter-Dependencies of *I–V* Curves



- **Edge flowing** current dominant at $V_G > 0$ [∵ Fringing field effect (E_{edge})].
- $E_{edge} > E_{bulk}$.
- $V_{ox,edge} > V_{ox,bulk}$.
- $\phi^*_{Bp,\,edge} < \phi^*_{Bp,\,bulk}$.
- $I_{h,edge} > I_{h,bulk}$.

$$q\phi^*_{Bp} = q\chi_S - q\Phi_M + E_g - qV_{ox}$$

$$I_h = A^* A_{eff}\, P_t\, T^2 exp\left(-\frac{q\phi^*_{Bp}}{k_B T}\right)\left[1 - exp\left(-\frac{qV_{TD}}{k_B T}\right)\right]$$

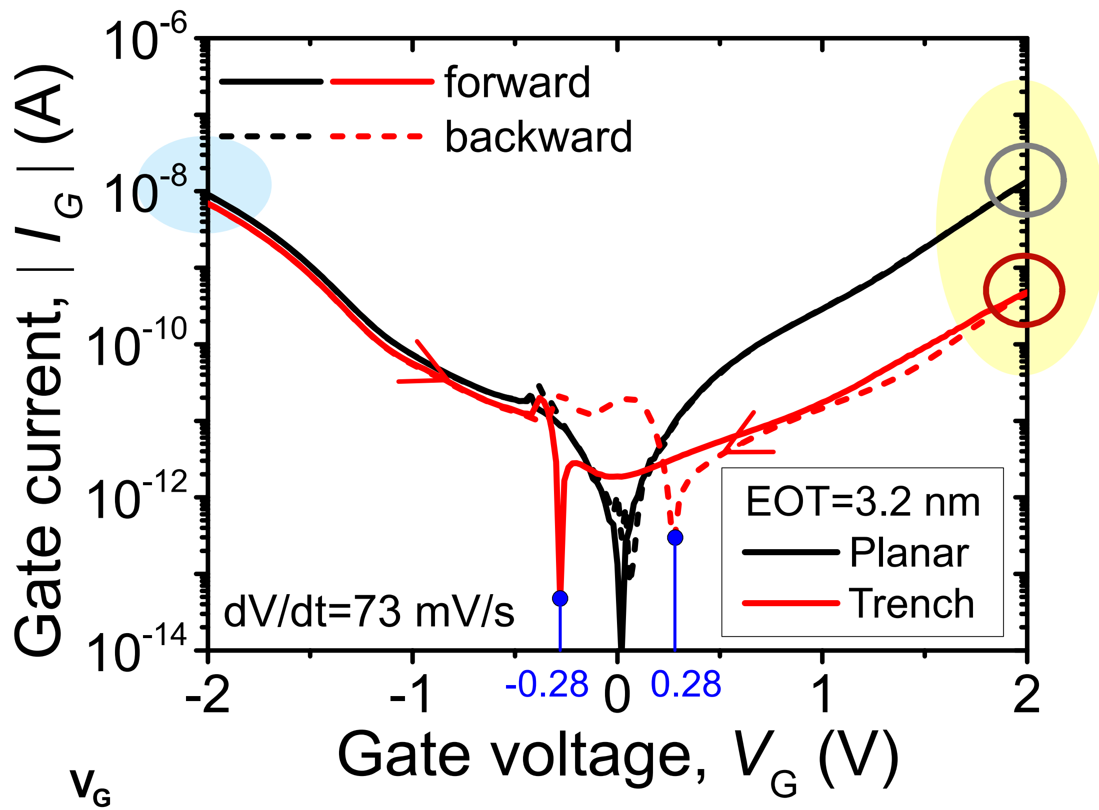
Similar Forward Bias Current

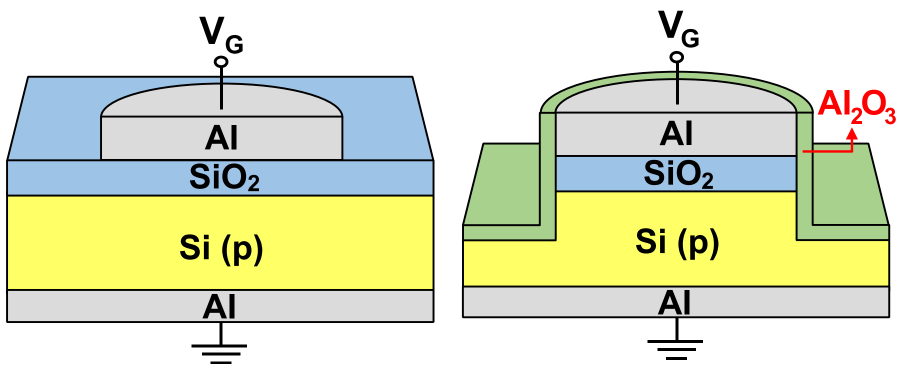
For Trench at –2V:

- **majority carriers (h^+)** accumulate.
- can still offer **enough h^+**.
- similar V_{ox}.

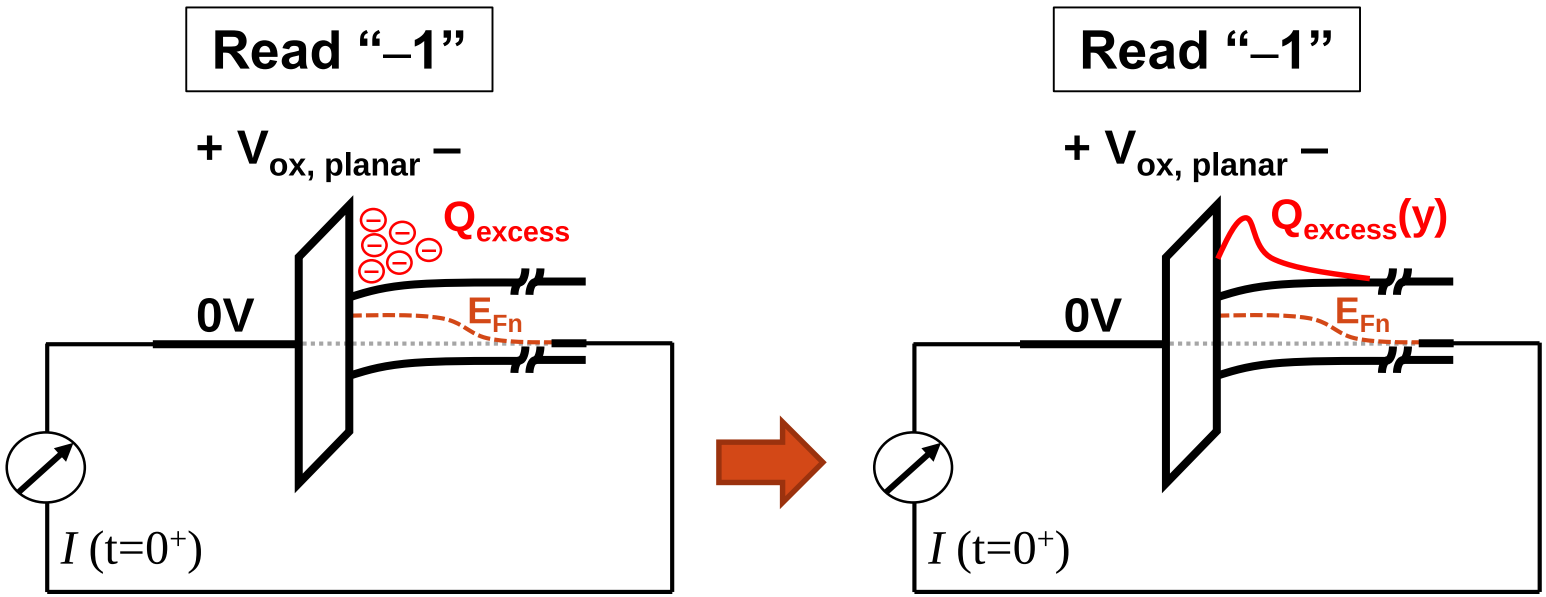
For Trench at +2V:

- **minority carriers (e^-)** accumulate.
- **insufficient e^- supply**.
- average smaller V_{ox}.





Other Factor Affecting Transient Current



Previous discussion ignore the effect of Q_{excess} distribution.

Distribution Profile of Q_{excess} might influence transient current and its retention time.

$$I_{G,\,read\,"-1"}(t) = |I_{e(T)}(t)| + |I_{h(T)}(t)| - \boxed{|I_{h(D)}(t)|}$$

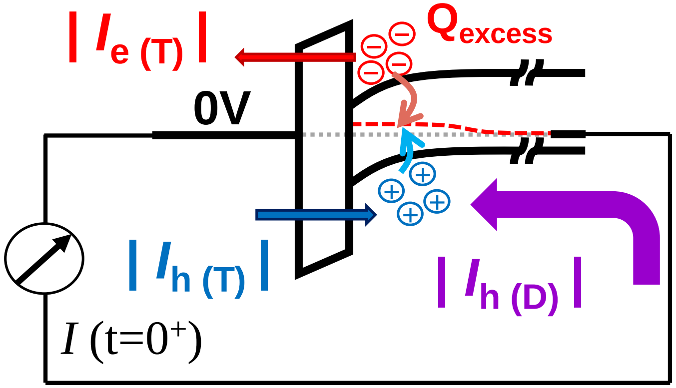
$\propto |Q_{excess}|$

Assumption of the Similar $I_{h(D)}$

$V_{ox,\ planar} > V_{ox,\ trench}$

$|I_{e\ (T)}| + |I_{h\ (T)}|_{(planar)} \gg |I_{e\ (T)}| + |I_{h\ (T)}|_{(trench)}$

$|I_{h\ (D)}|_{(planar)} \approx |I_{h\ (D)}|_{(trench)}$



$$I_{G,\,read\text{"}-1\text{"}}(t) = |I_{e(T)}(t)| + |I_{h(T)}(t)| - \boxed{|I_{h(D)}(t)|}$$

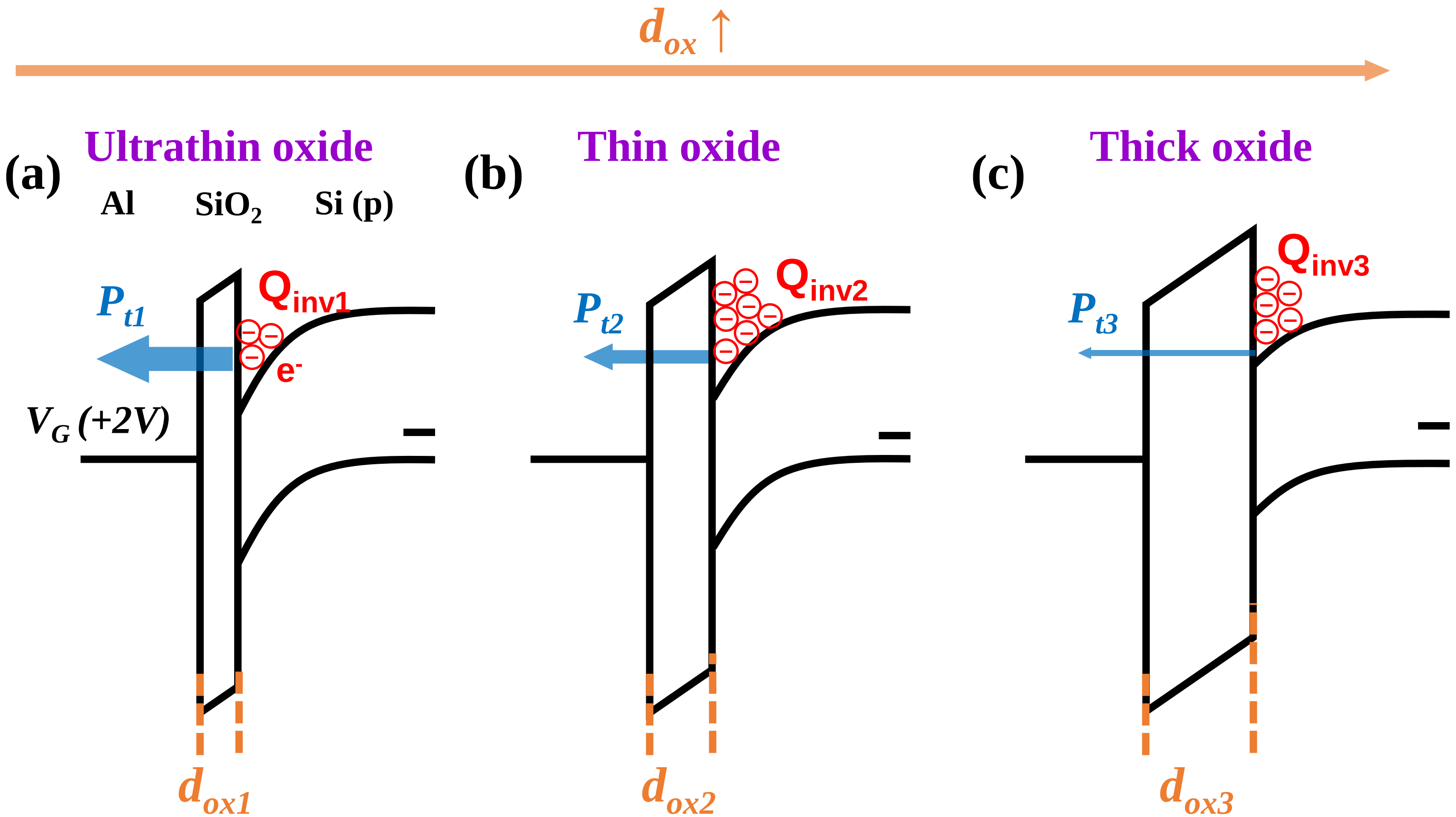
$\propto |Q_{excess}|$

$$q\phi^{*}_{Bp} = q\chi_S - q\Phi_M + E_g - qV_{ox}$$

$$I_h = A^{*} A_{eff} P_t T^2 exp\left(-\frac{q\phi^{*}_{Bp}}{k_B T}\right)\left[1 - exp\left(-\frac{qV_{TD}}{k_B T}\right)\right] \qquad V_{ox} = -\frac{Q_d + Q_{inv}}{C_{ox}}$$

- $I_{h\ (D)}$ might also be related to the distribution profile of electrons.
- Planar and Trench devices might have similar profile.→ similar $I_{h\ (D)}$.

Inversion Charges and CW



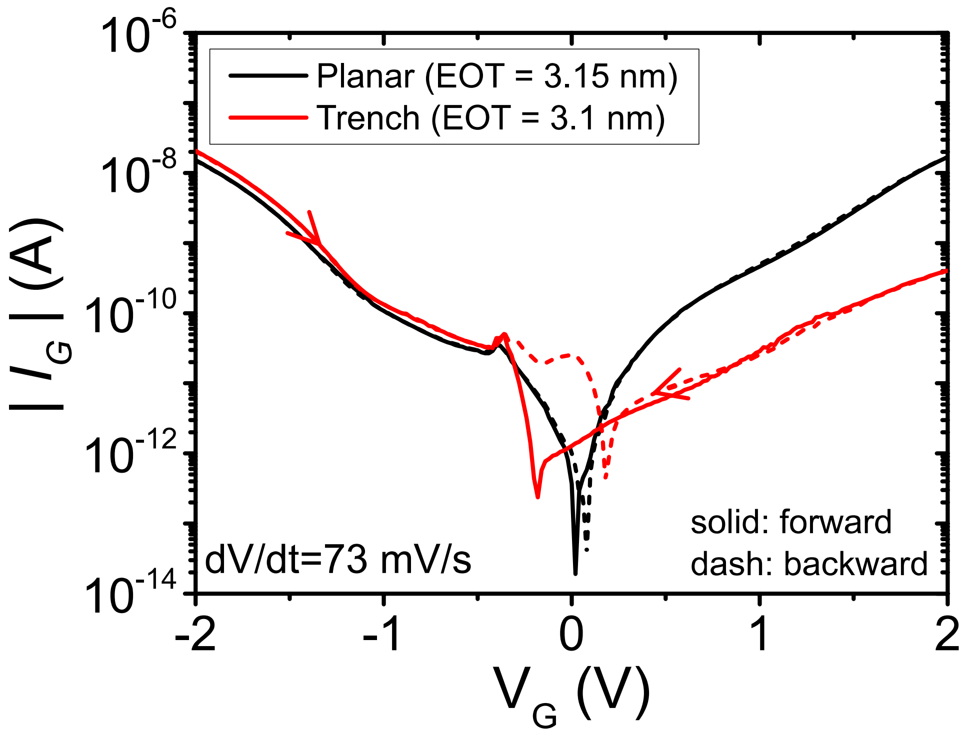
$d_{ox1} < d_{ox2} < d_{ox3}$

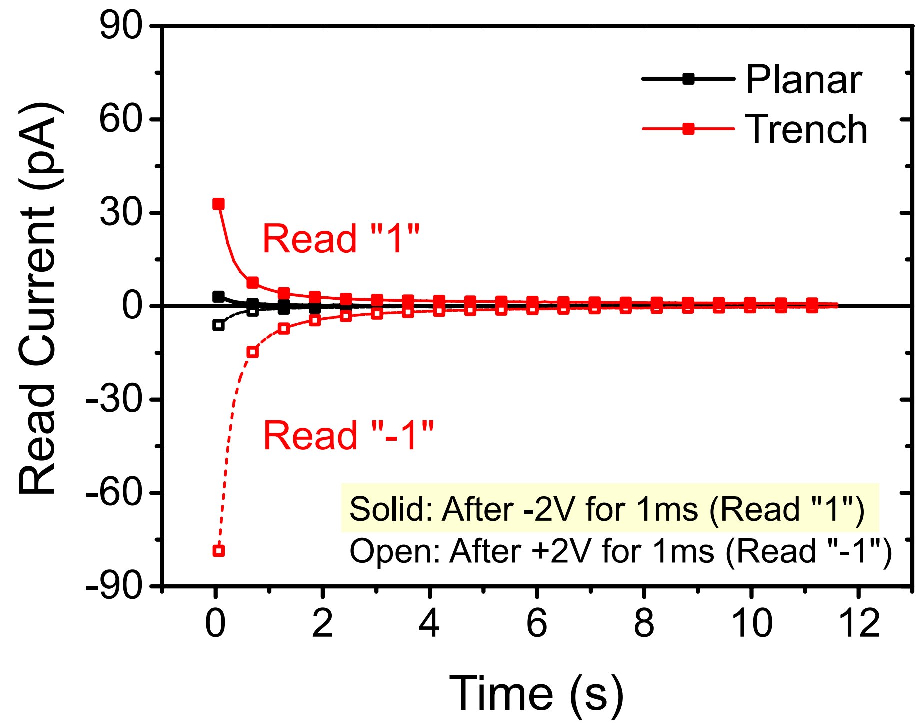
$P_{t1} > P_{t2} > P_{t3}$

$Q_{inv1} < Q_{inv2} > Q_{inv3}$

$CW_1 < CW_2 > CW_3$

Positive Transient Current

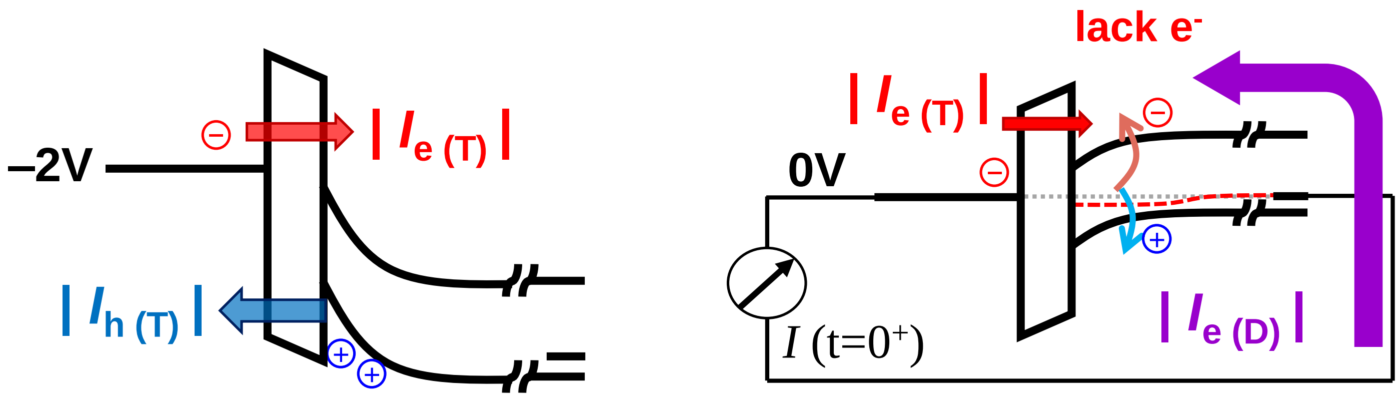




- Write "–1" (+2V) to Read "–1" (0V) ➔ negative transient current (larger).
  - Recombination current (recombine excess electrons).
- Write "1" (–2V) to Read "1" (0V) ➔ positive transient current (smaller).
  - Generation current (generate electrons).

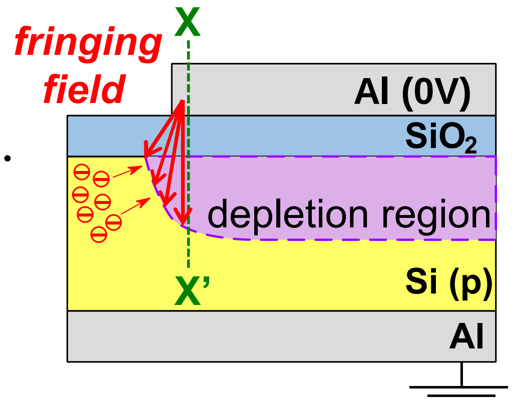
Positive Transient Current

Write “1” (–2V) to Read “1” (0V)

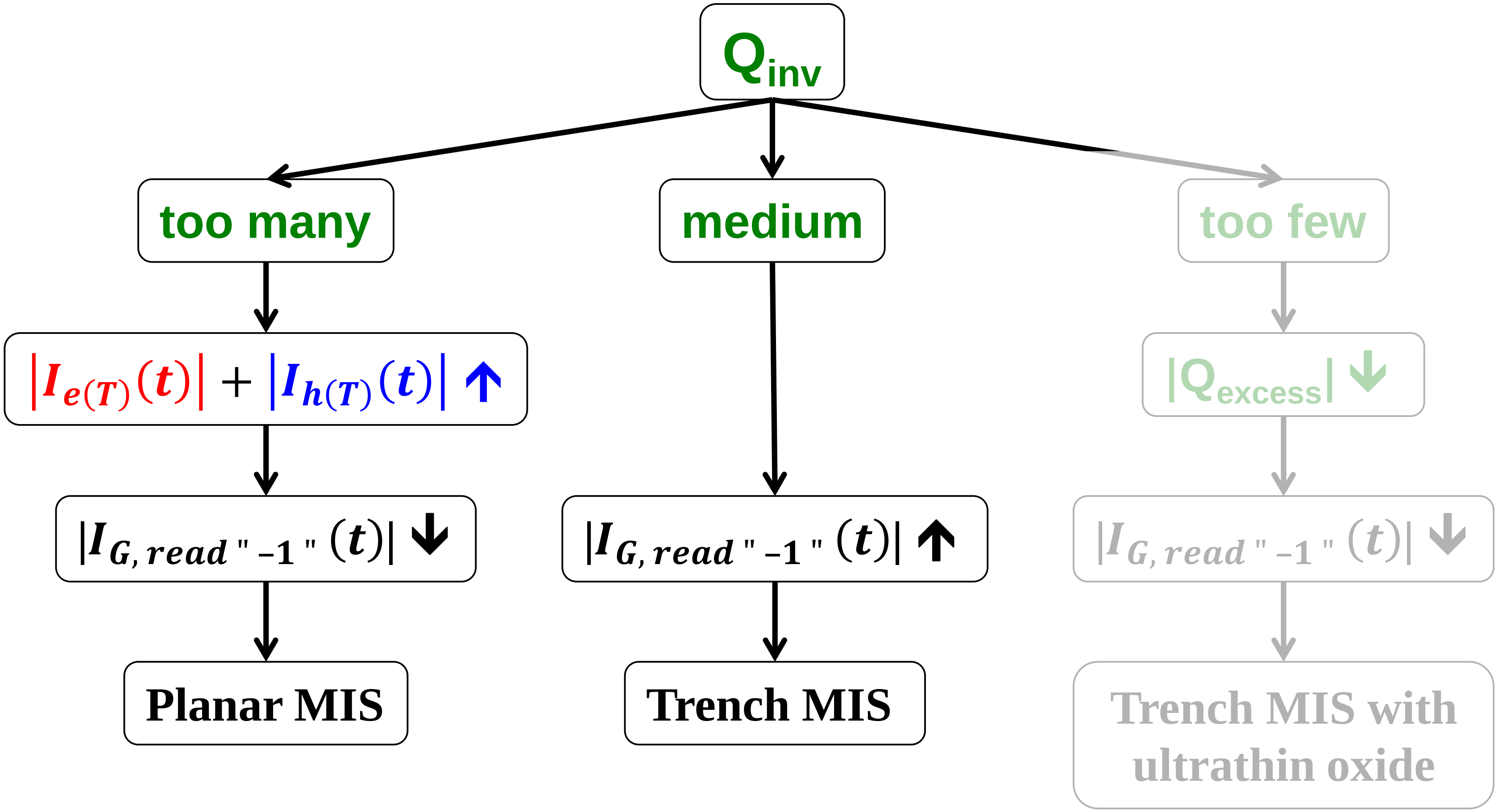


- For **Trench MIS TDs:**
  - ∵Lack of electrons.
  - **positive transient displacement current** to supply electrons.

- For **Planar MIS TDs**:
  - sufficient lateral electrons supply from substrate.
  - **No lack of electrons** despite fast switching.
  - small transient current.

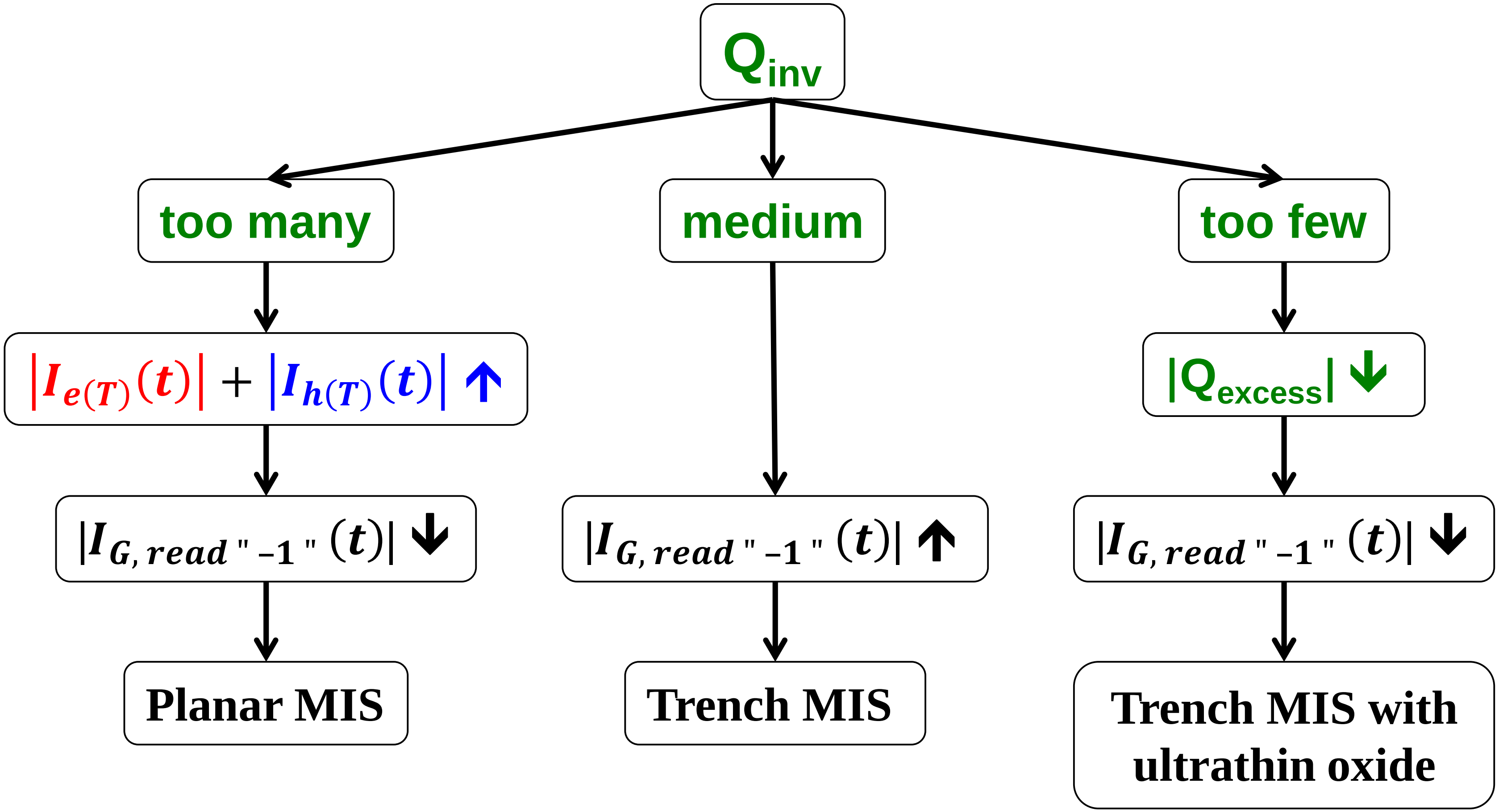


Q_{inv}, Q_{excess}, and $I_{G,\,read\ \text{“}-1\text{”}}$



$$I_{G,read\ "-1"}(t) = \underbrace{\boxed{|I_{e(T)}(t)| + |I_{h(T)}(t)|}}_{\propto V_{ox} \propto |Q_{inv}|} - \underbrace{\boxed{|I_{h(D)}(t)|}}_{\propto |Q_{excess}|}$$

Q_{inv}, Q_{excess}, and $I_{G,\ read\ \text{“–1”}}$



$$I_{G,read\ "-1"}(t) = \underbrace{\boxed{|I_{e(T)}(t)| + |I_{h(T)}(t)|}}_{\propto V_{ox} \propto |Q_{inv}|} - \underbrace{\boxed{|I_{h(D)}(t)|}}_{\propto |Q_{excess}|}$$

TCAD Simulation: Models

- **MODELS** conmob srh auger bgn fldmob print bqp.n bqp.p gate temperature=293 qtunnsc qtnl.derivs

Table 1-1 Summary of Physical Models and Numerical Calculation Method Used in TCAD Simulation

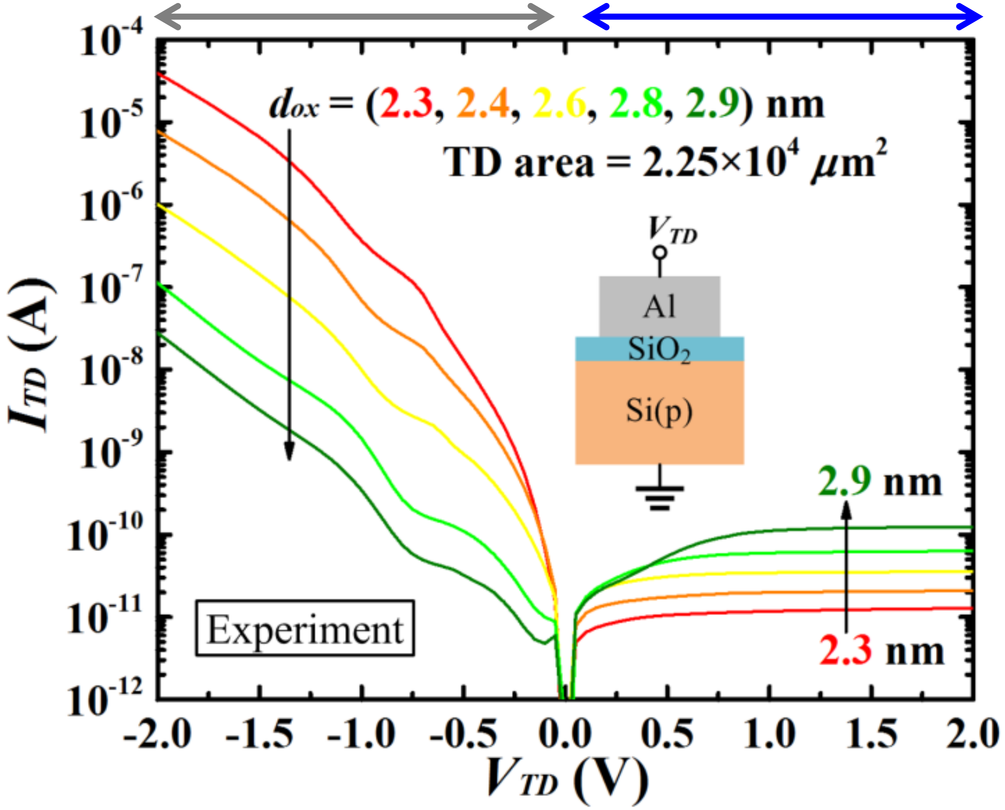
Physical Models	Numerical Calculation Method	
1. Concentration-dependent mobility (conmob)		
2. SRH (srh)		
3. Auger (auger)		
4. Band gap narrowing (bgn)		
5. Field-dependent mobility (fldmob)	Gummel + Newton Method	
6. Quantum/direct tunneling (qtunnsc)		electrons, holes, and band-to-band tunneling
~~7. FN tunneling (fn.cur)~~		
8. Bohm quantum potential (bqp) models		consider distribution of electrons in the inversion layer (quantum confinement)

*qtnl.derivs: improve convergence

Y. K. Lin, "Effect of Lateral Diffusion Current in Inversion I-V Characteristic of MOS Devices with Ultrathin Oxide and Its Applications," M.S. Thesis Dept. Elect. Eng. Nat. Taiwan Univ., Taipei, Taiwan, R.O.C., 2014.

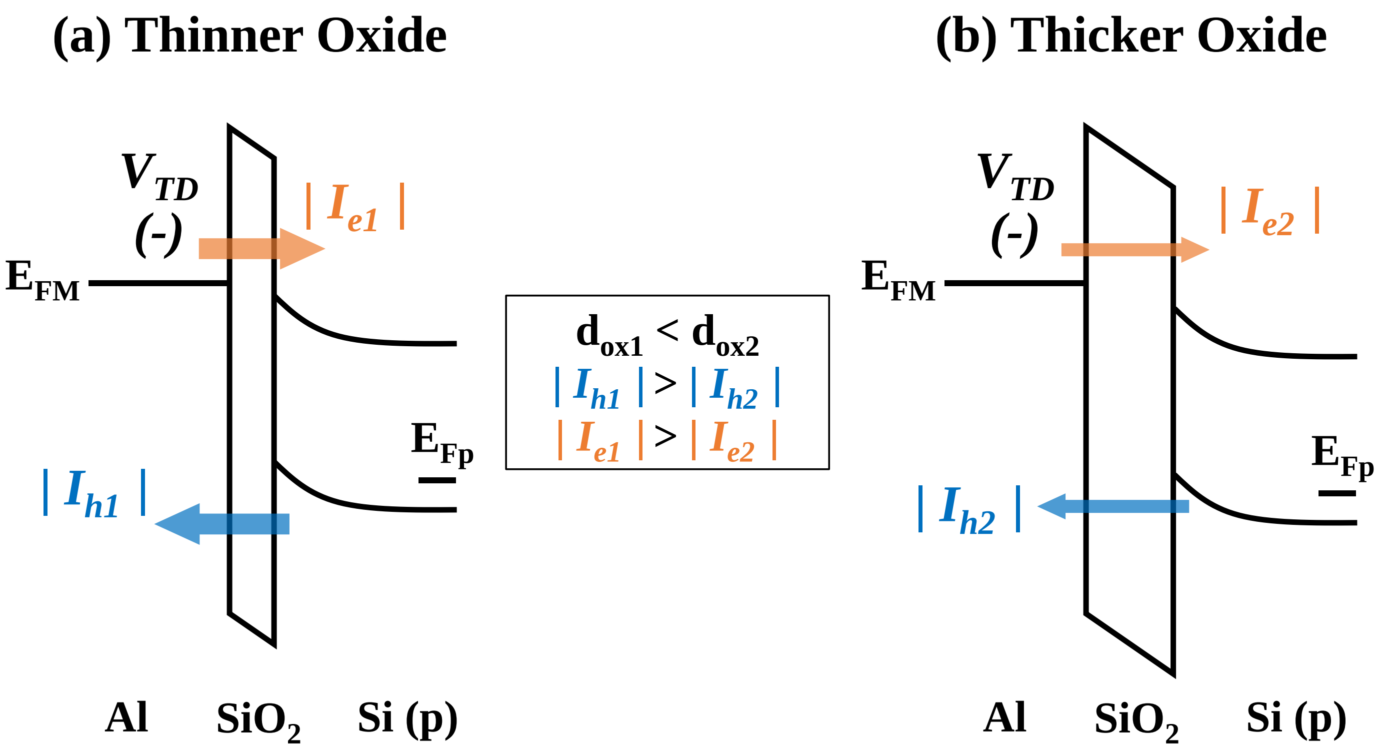
Oxide tunneling limited

Minority carriers supply limited



Forward Bias no SBH

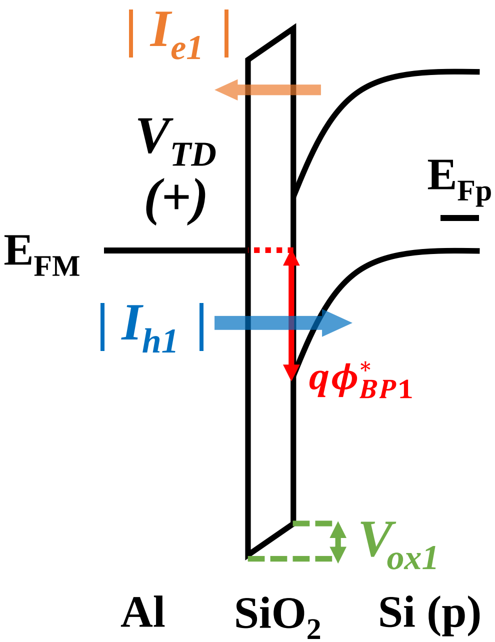
At forward bias (V_{TD} < 0 V)



Reverse Bias has SBH

At reverse bias (V_{TD} > 0 V)

(a) Thinner Oxide



$d_{ox1} < d_{ox2}$

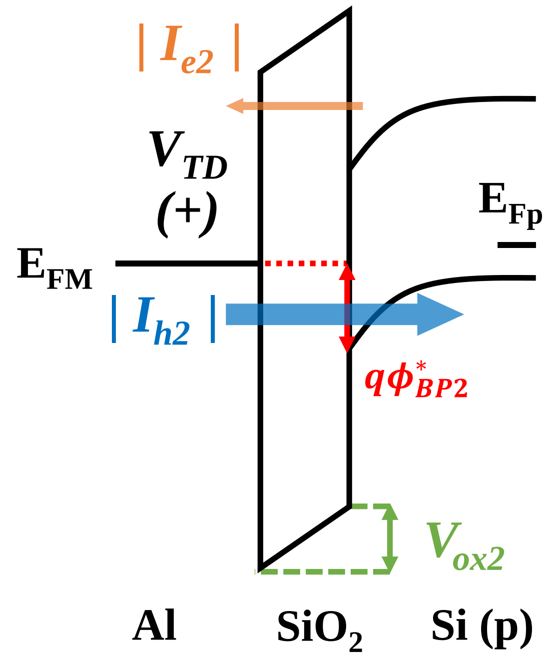
$V_{ox1} < V_{ox2}$

$q\phi^*_{BP1} > q\phi^*_{BP2}$

$| I_{h1} | < | I_{h2} |$

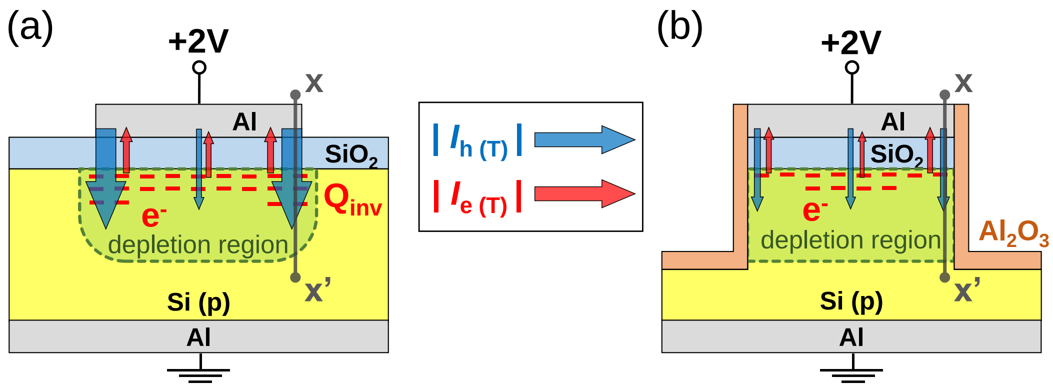
$| I_{e1} | > | I_{e2} |$

(b) Thicker Oxide

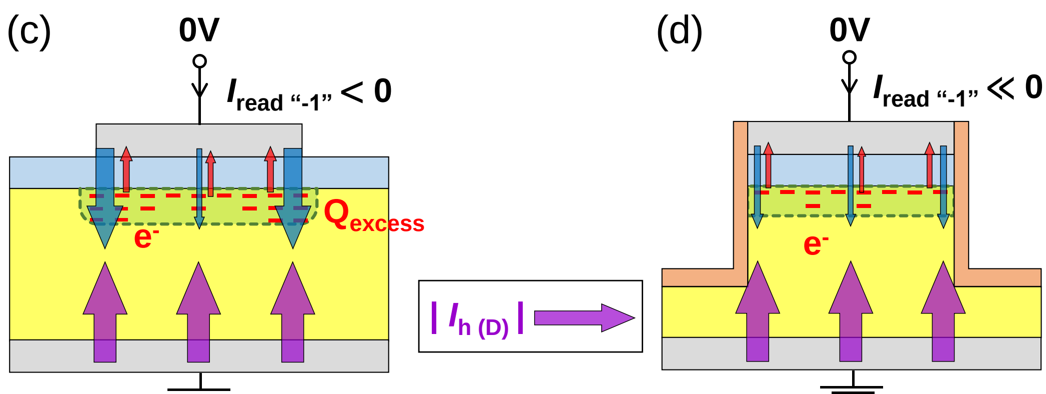


Thermal Equilibrium Model

1. Write "-1" (+2V, steady-state)



2. Read "-1" @ t=0⁺s (non-equilibrium)



$|I_{e\,(T)}| + |I_{h\,(T)}|_{(planar)} \gg |I_{e\,(T)}| + |I_{h\,(T)}|_{(trench)}$

$|I_{h\,(D)}|_{(planar)} \approx |I_{h\,(D)}|_{(trench)}$

$|I_{read\ “-1”}|_{(planar)} \ll |I_{read\ “-1”}|_{(trench)}$

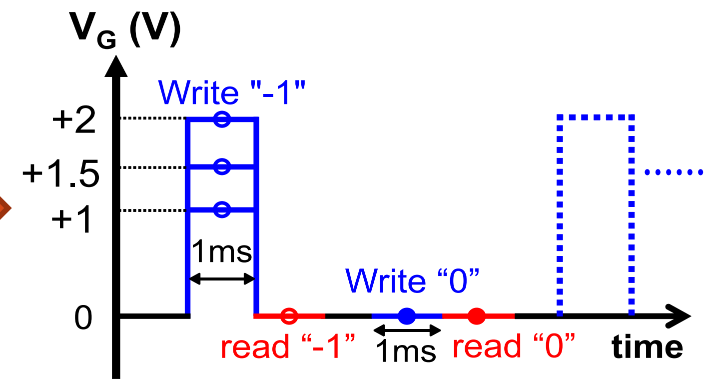
Verification of Thermal Equilibrium Model

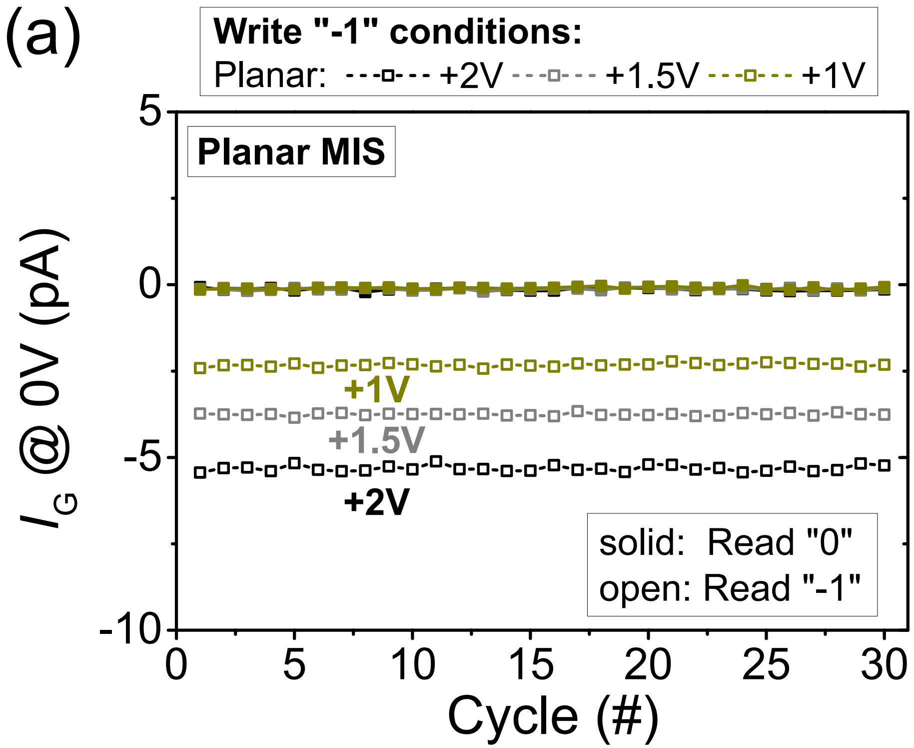
- **<u>Experimental way</u>**

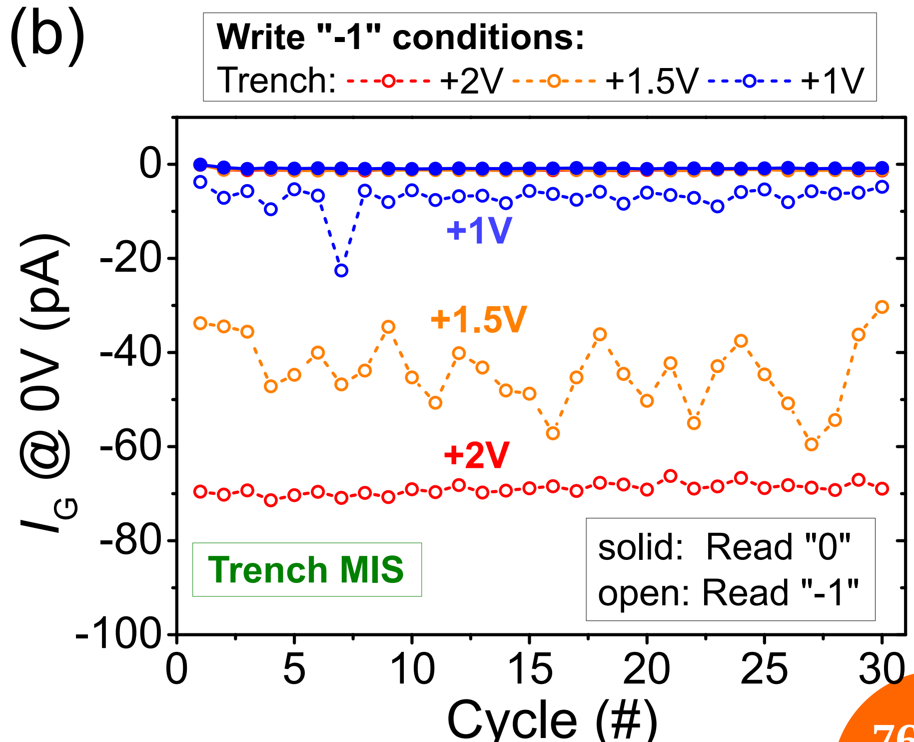
Based on the proposed model,

| transient current | ∝ | Q_{excess} |.

$Q_{excess}(" - 1 "\ state)$
$\approx Q_{inv}(@ + 2\sim + 1\ V) - Q_{inv}(@\ 0\ V)$

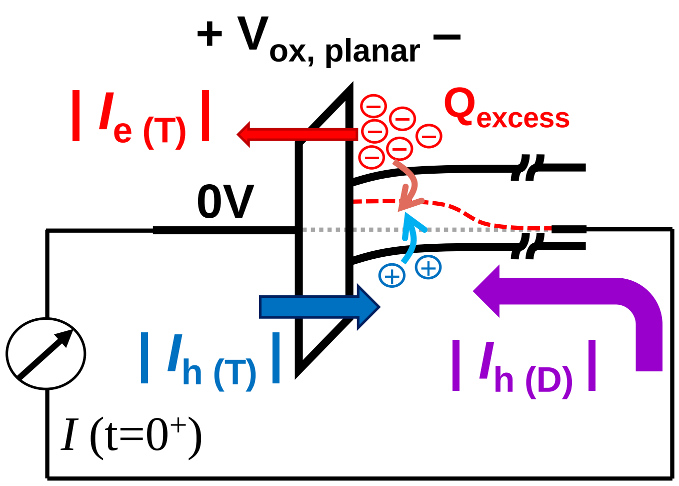


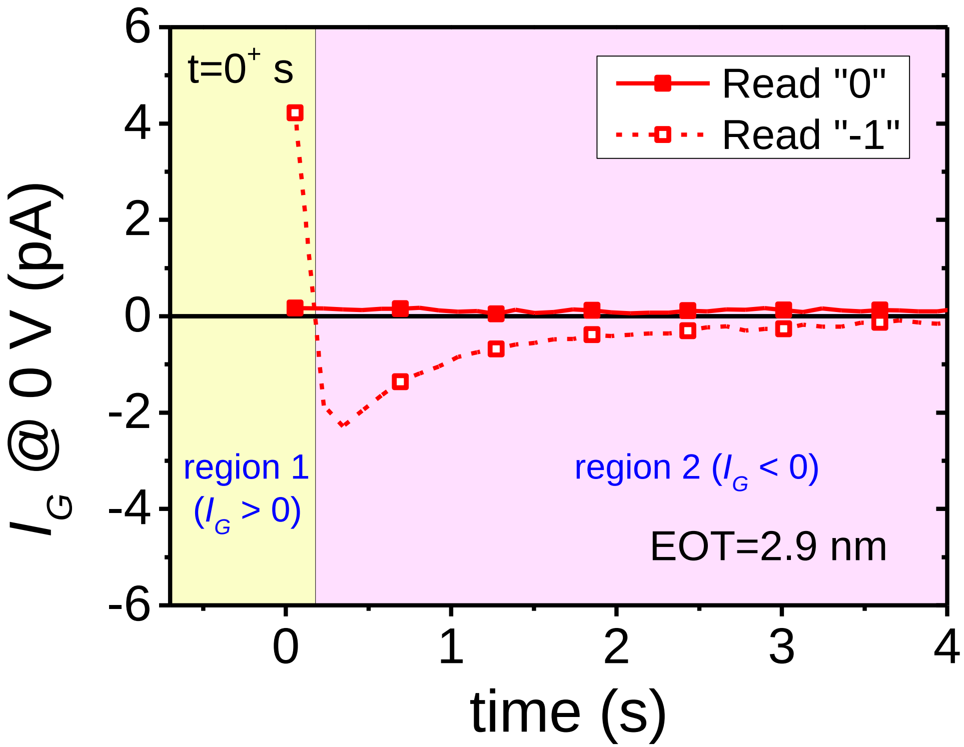




Verification of Thermal Equilibrium Model

- **Experimental way**



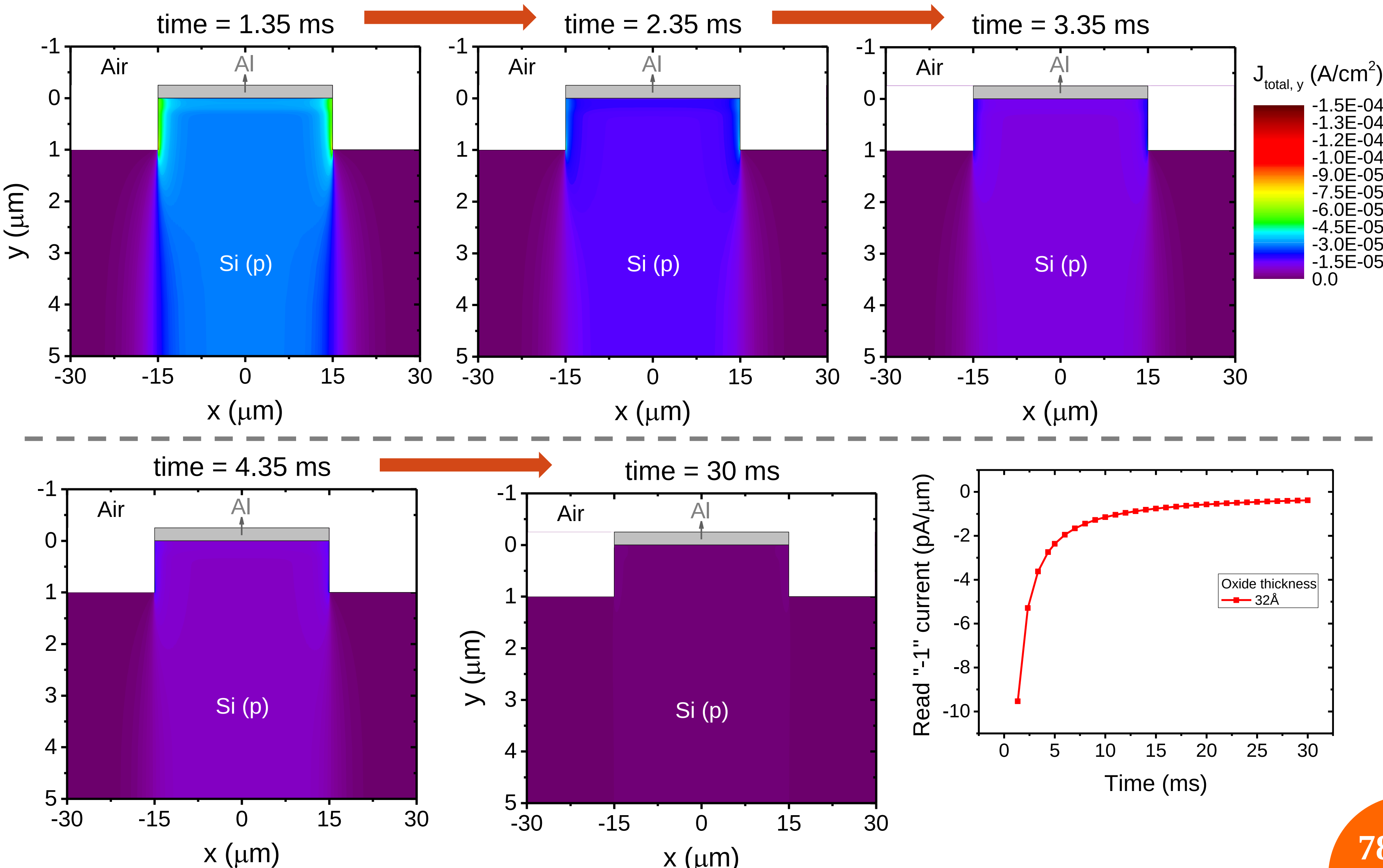


- 9 out of 24 planar devices show the existence of positive transient current ($|I_{e(T)}(t)| + |I_{h(T)}(t)|$).
- Because of **more Q_{inv} @+2V.**

$$I_{G,read\,"-1"}(t) = |I_{e(T)}(t)| + |I_{h(T)}(t)| - |I_{h(D)}(t)|$$

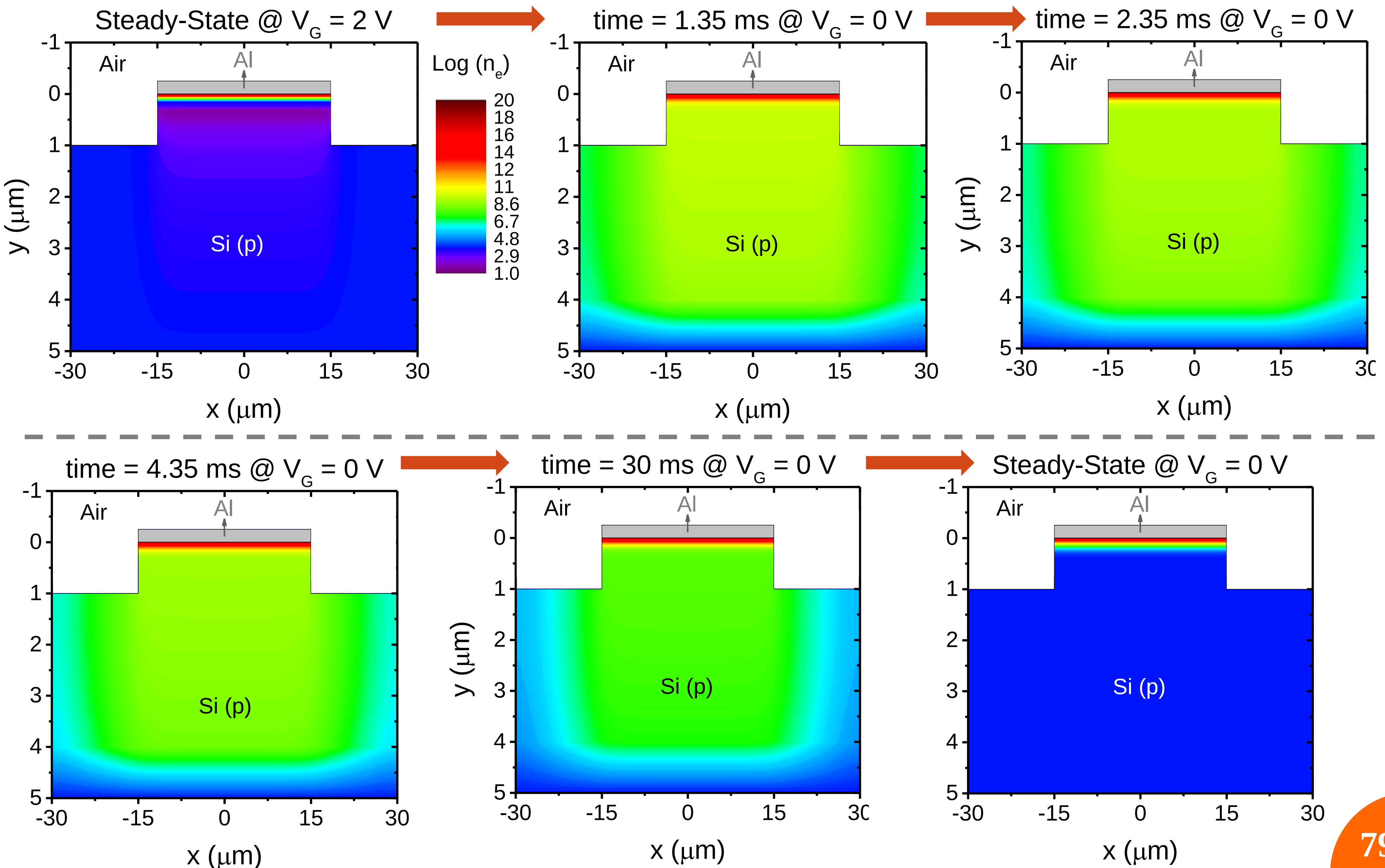
Verification of Thermal Equilibrium Model

- **Total current density @ y-direction (same d_{ox})**



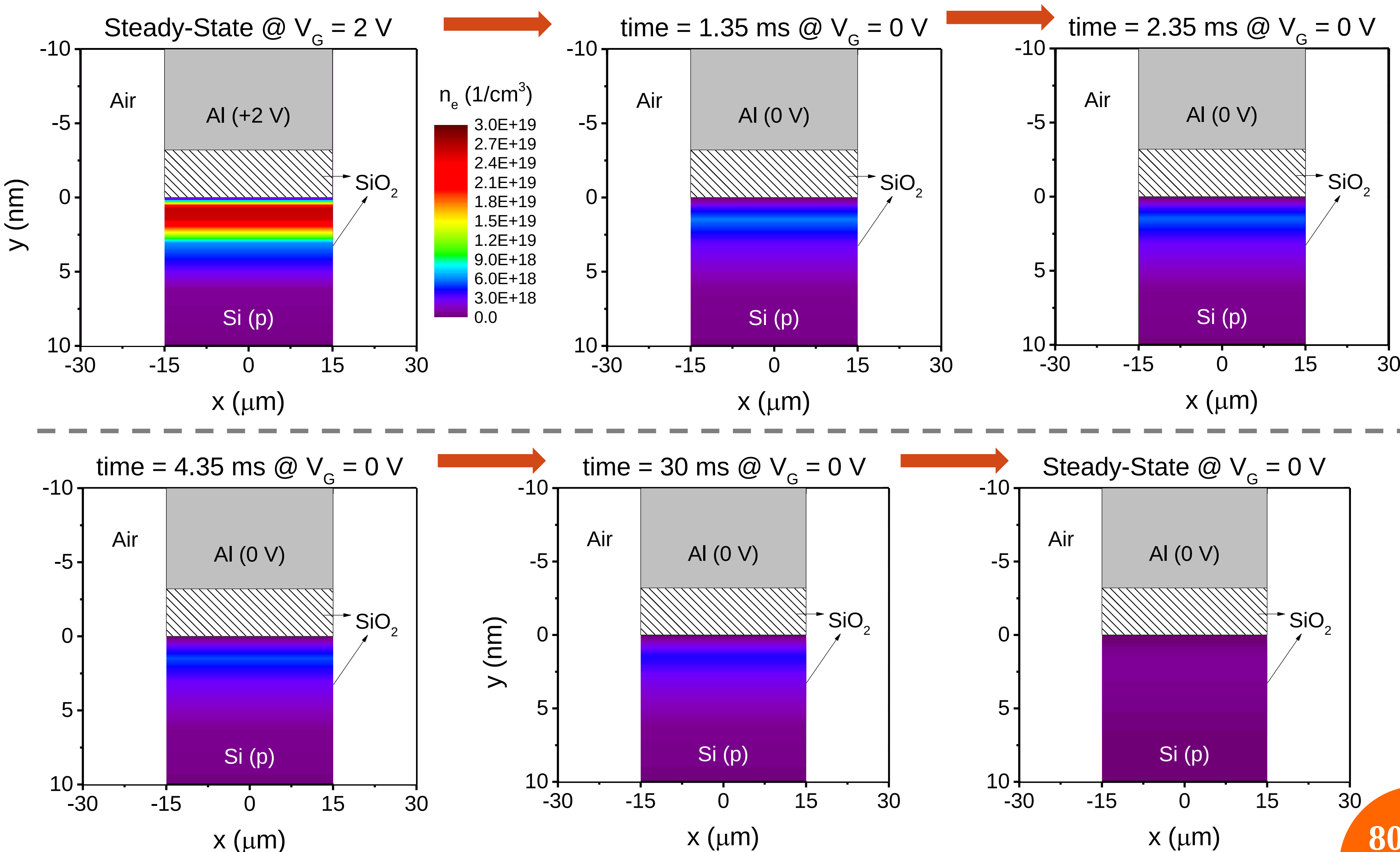
Verification of Thermal Equilibrium Model

- **<u>Electron concentration under log scale (same d_{ox})</u>**



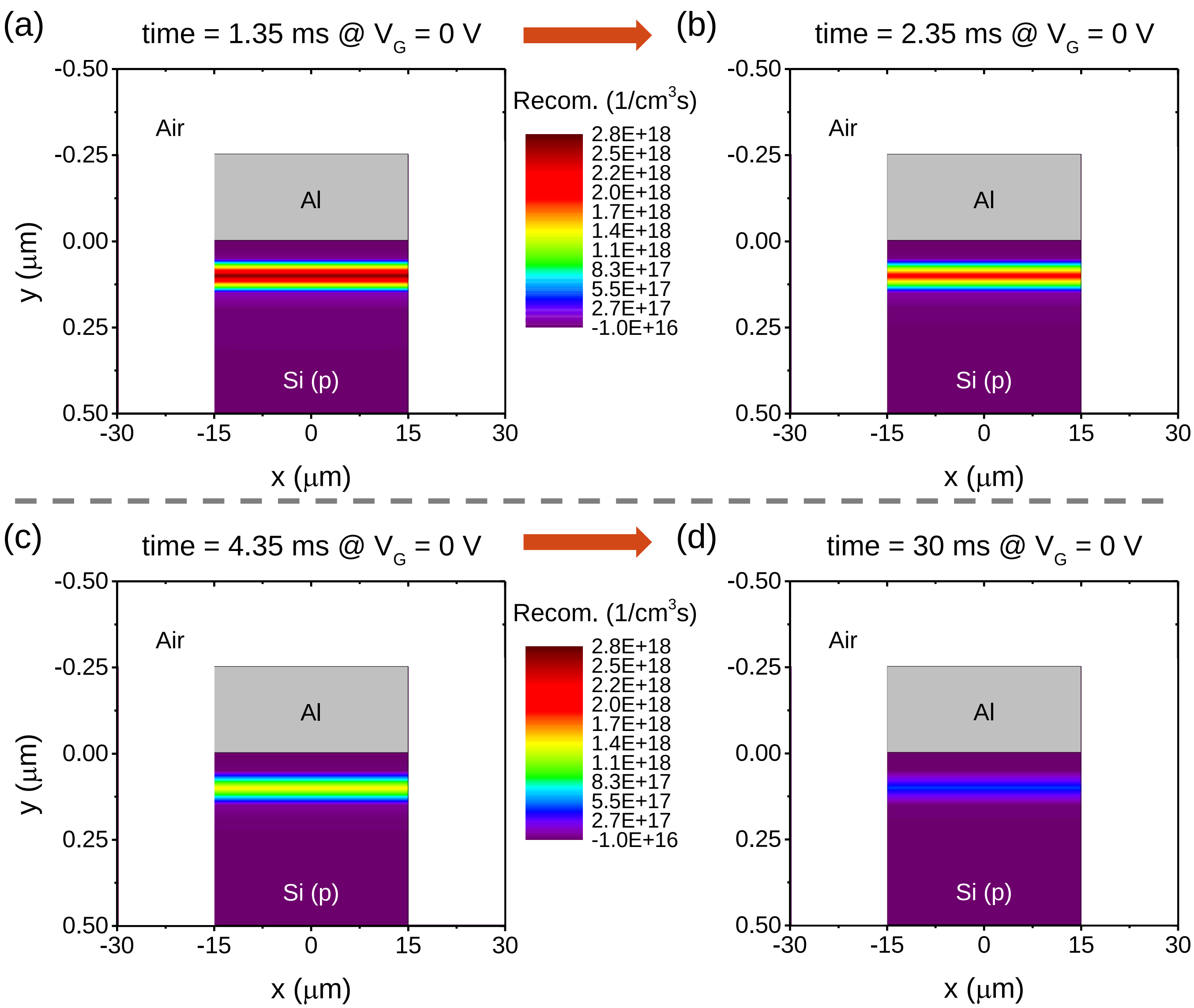
Verification of Thermal Equilibrium Model

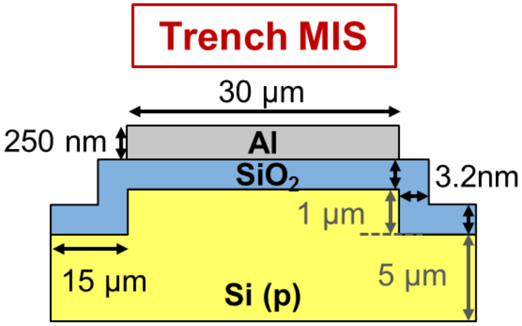
- **<u>Electron concentration under linear scale (same d_{ox})</u>**



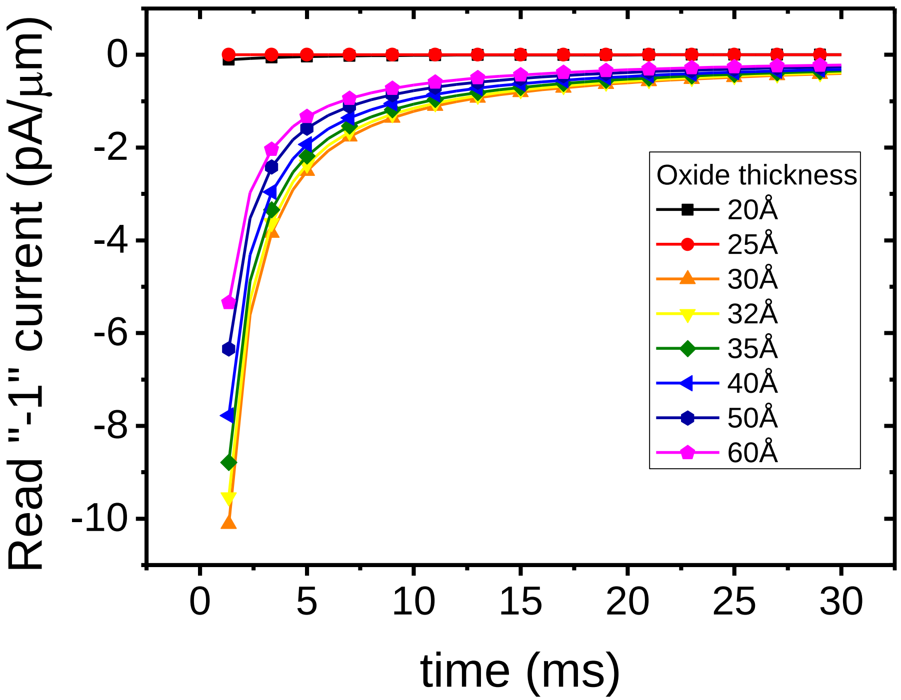
Verification of Thermal Equilibrium Model

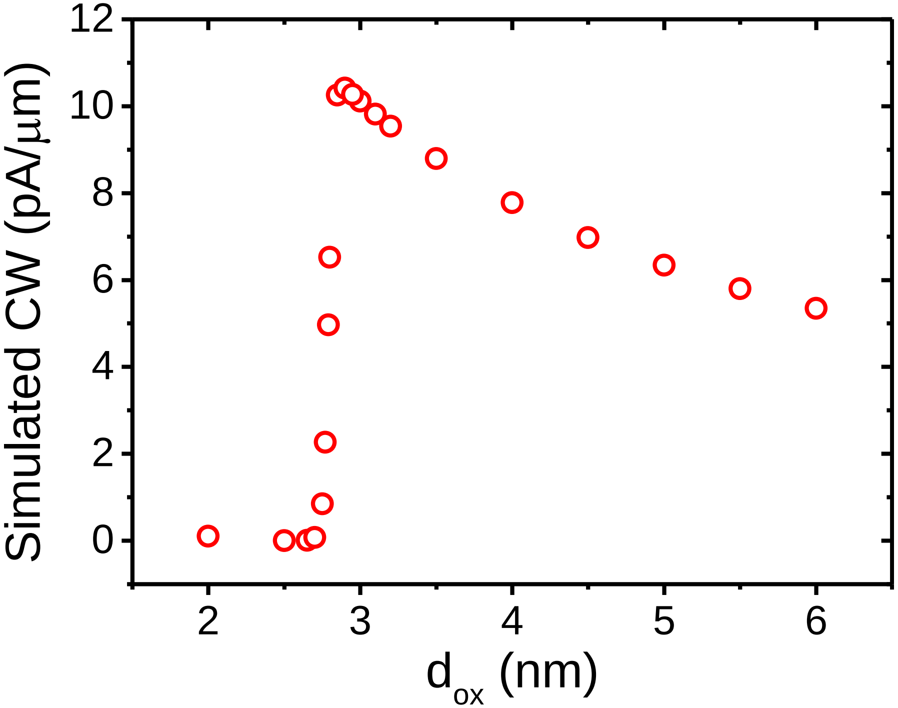
- **Transient TCAD: Recombination rate (same d_{ox})**





Simulated Retention under Various EOTs

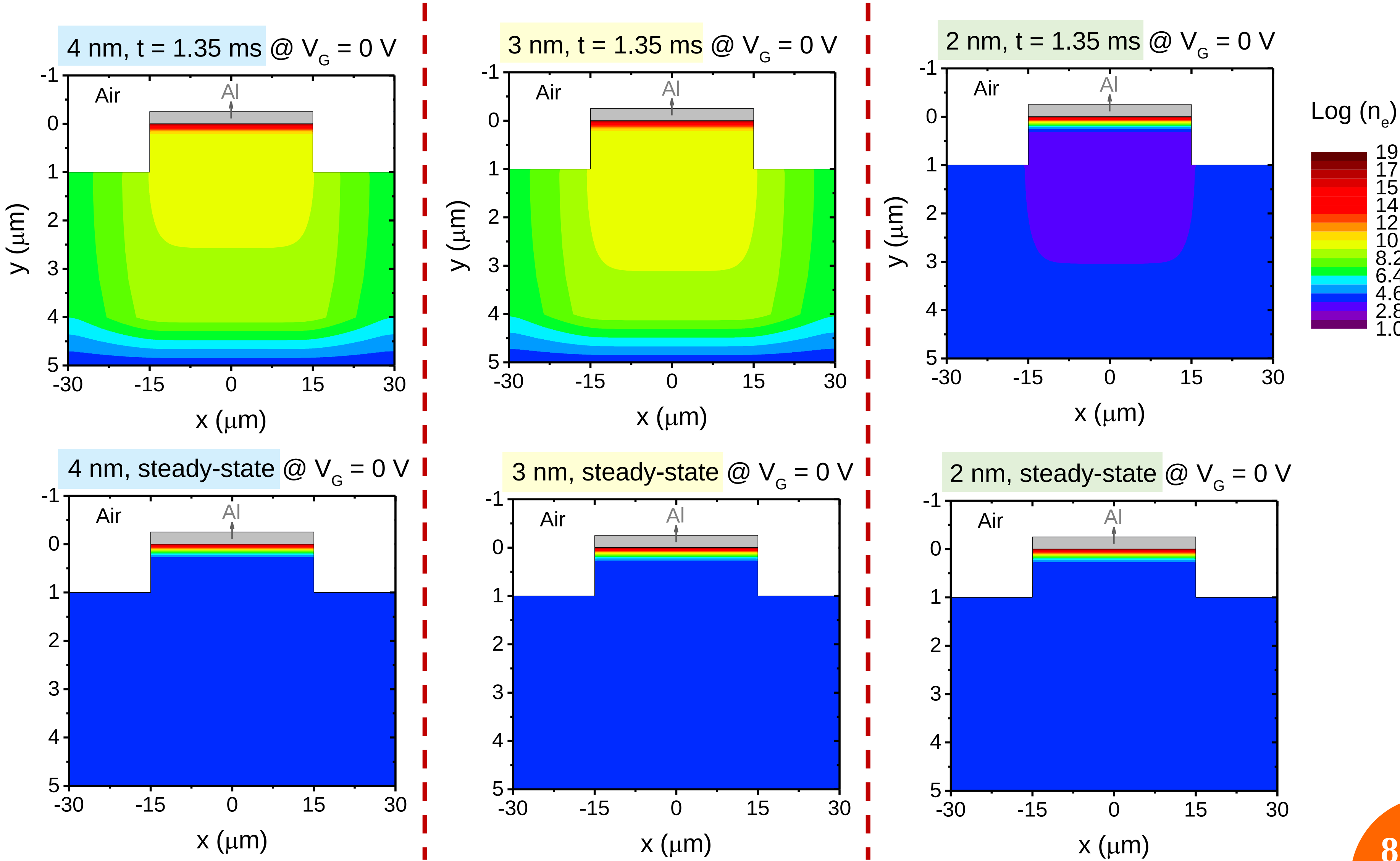




$$CW \approx -I_{G,read\,"-1"}$$

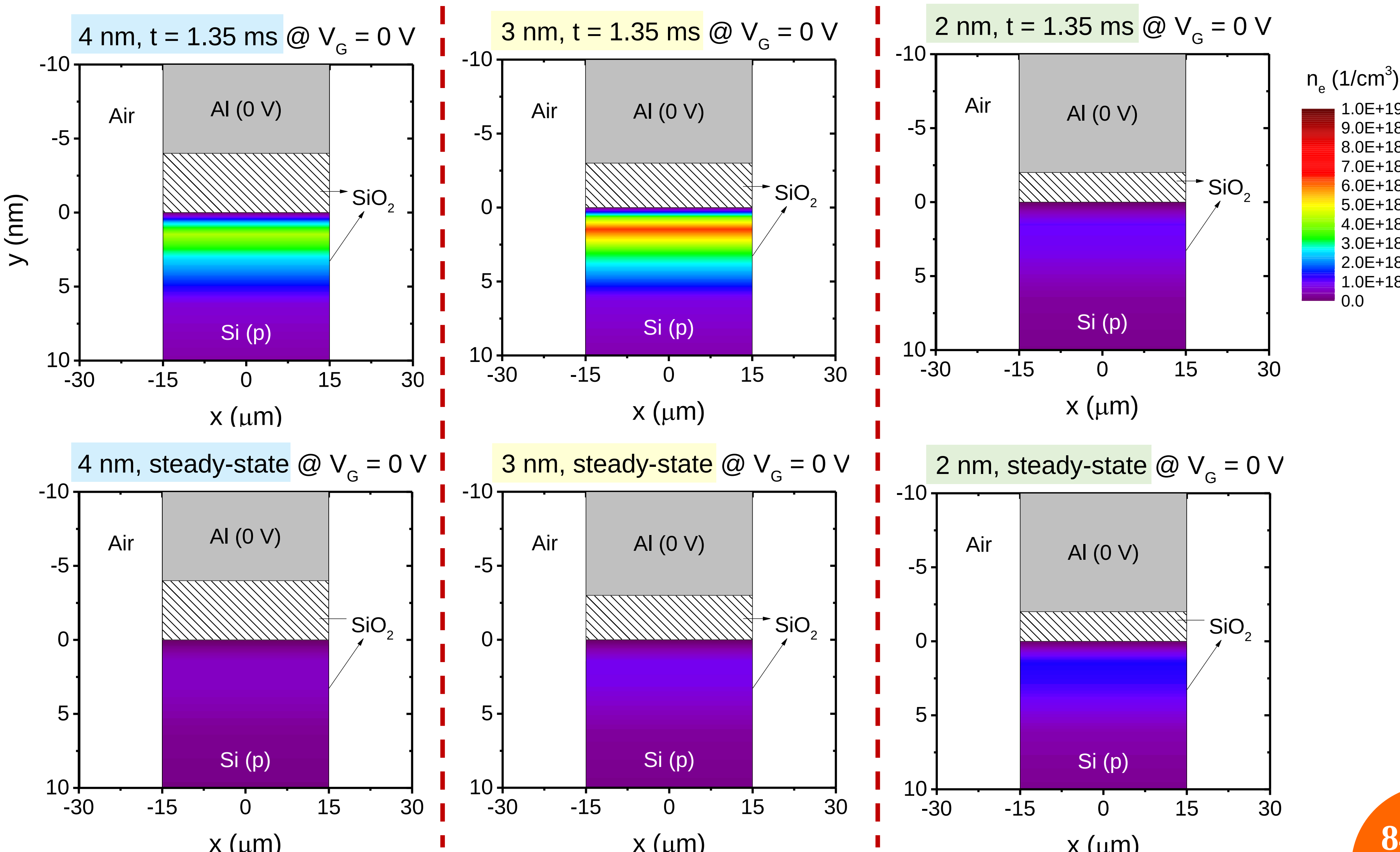
Transient TCAD with Different EOTs

- **Electron concentration under log scale (different d_{ox})**



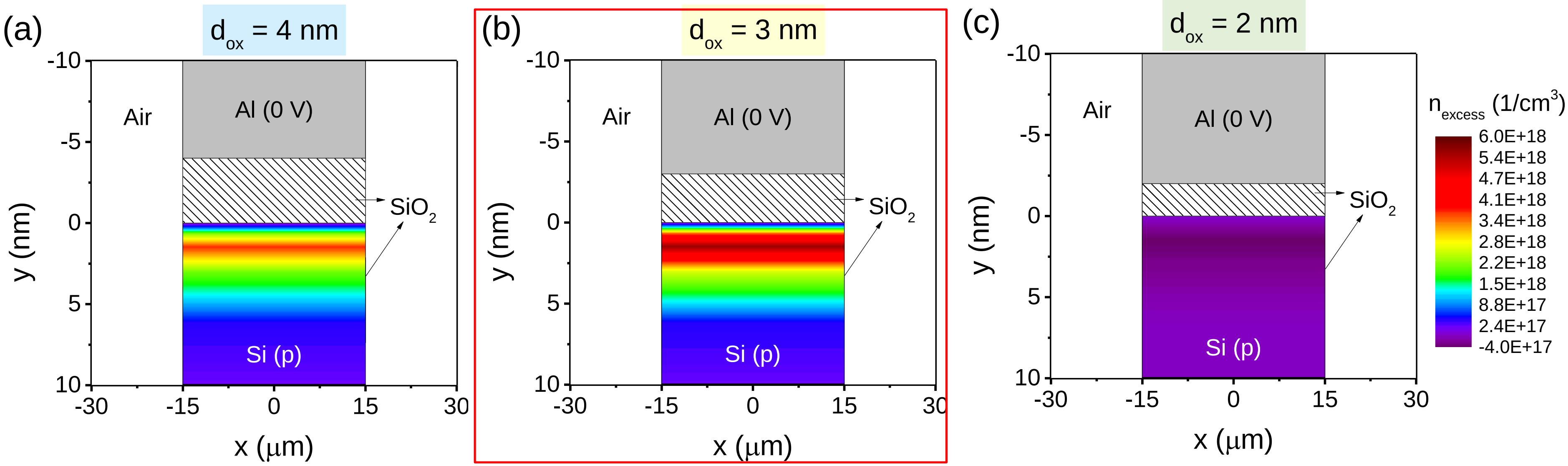
Transient TCAD with Different EOTs

- **Electron concentration under linear scale (different d_{ox})**



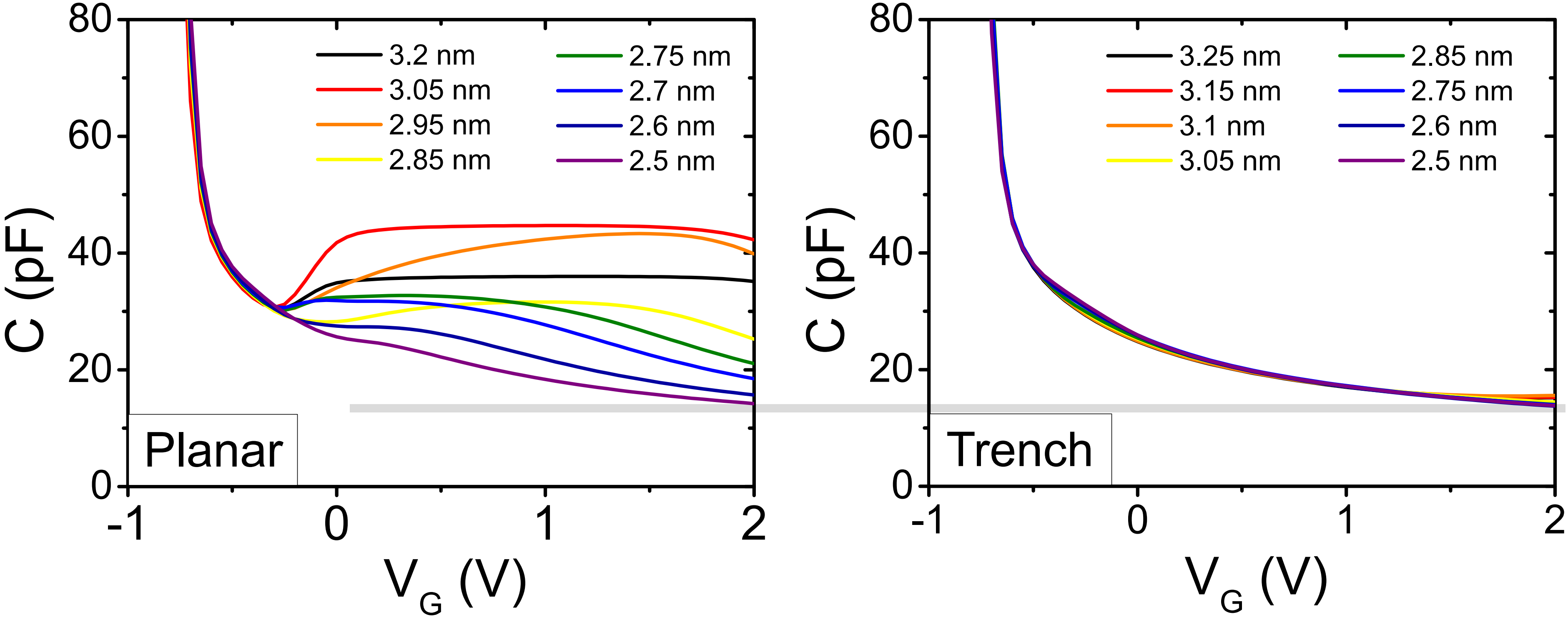
Transient TCAD with Different EOTs

- **Excess carrier concentration under linear scale (different d_{ox})**



$$n_{excess} = n_e(@\, t = 1.35\, ms) - n_e(@\, t = \infty)$$

C–V with Different EOTs @ 100kHz

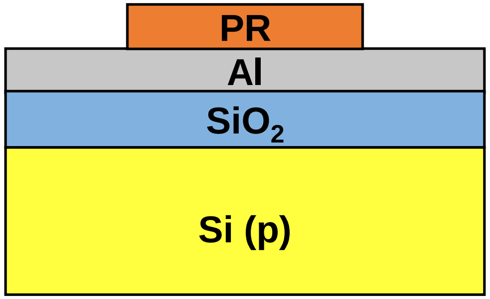


Undercut

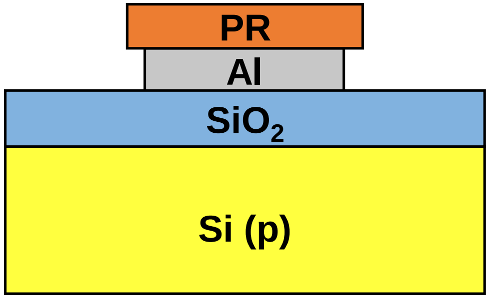
1. Anodic Oxidation

2. Deposit Al

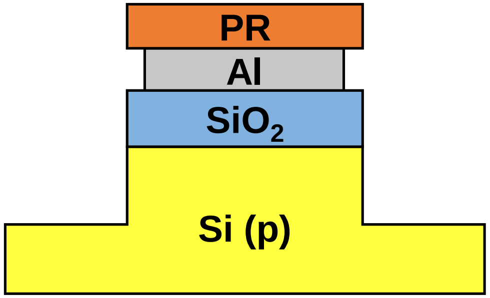
3. Photolithography



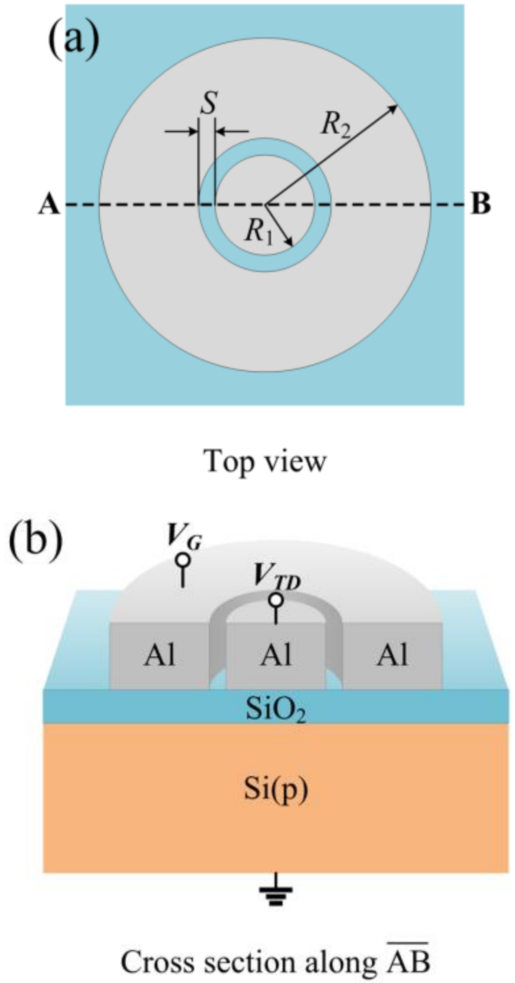
4. Wet etch Al (undercut)

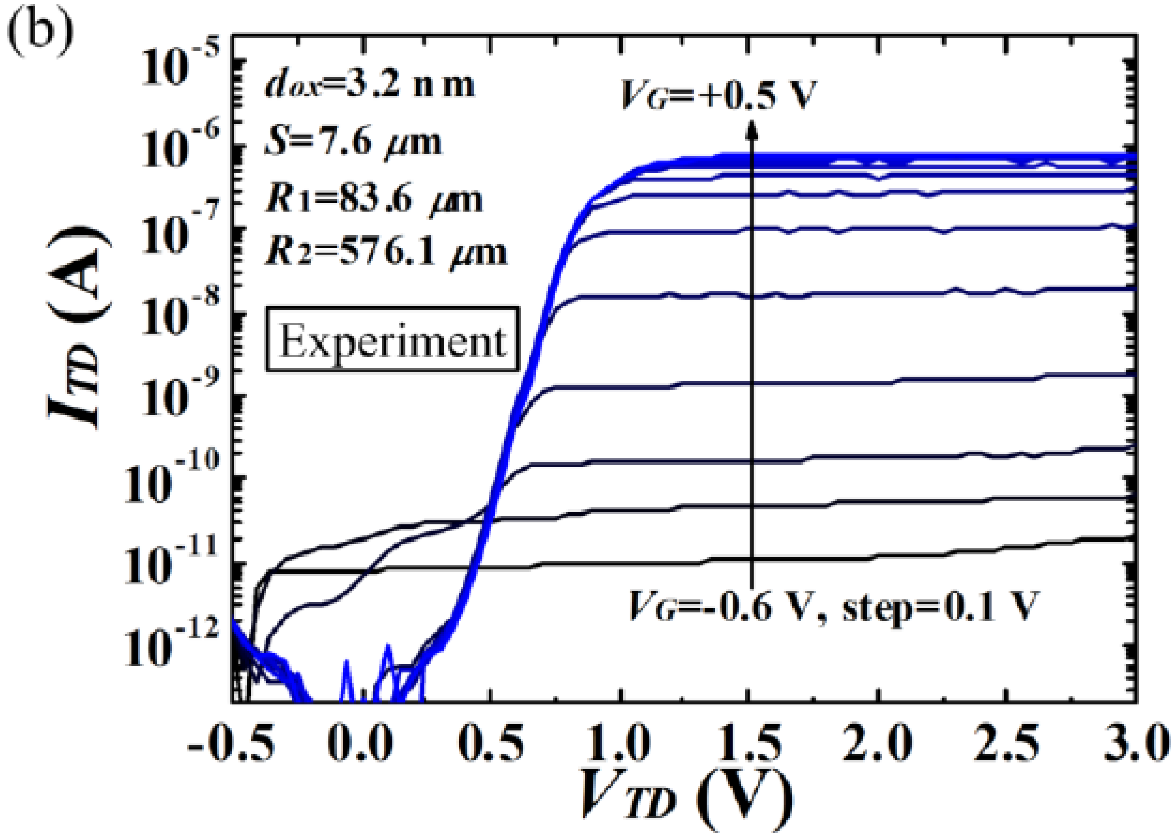


5. RIE etch SiO_2 ,Si
then dip BOE



Gated-MIS Tunnel Transistor





- The **electron concentration (n_e) under the gate** has great impact on the current of the center MIS TD.
  - **MIS TD is sensitive to the neighboring n_e.**

C. Liao and J. Hwu, "Subthreshold Swing Reduction by Double Exponential Control Mechanism in an MOS Gated-MIS Tunnel Transistor," in IEEE Transactions on Electron Devices, vol. 62, no. 6, pp. 2061-2065, June 2015, doi: 10.1109/TED.2015.2424245.