

An Interleaved Series-Capacitor Tapped Buck Converter for High Step-Down DC/DC Application

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Abstract—High step-down dc/dc converters are widely utilized in telecom and modern industrial applications. Due to the high step-down ratio, conventional Buck converter cannot provide satisfactory performance. To solve this problem, quite a few new topologies have been proposed to improve the performance of high step-down dc/dc converters, such as series-capacitor Buck (SC-Buck) converter, 3-level Buck converters, tapped inductor Buck converters, and LLC resonant converters. In this paper, the twice step-down benefit of SC-Buck converter and the zero-voltage switching benefit of series-capacitor tapped Buck (SC-TaB) converter are combined together to propose a new topology: interleaved series-capacitor tapped Buck (ISC-TaB) converter. To analyze the performance of the proposed ISC-TaB converter, the operation principles are discussed and the voltage conversion ratio is derived. In addition, to guide the design procedure and optimization, the current waveforms and voltage waveforms of the proposed ISC-TaB are derived. In order to verify the performance of the proposed ISC-TaB, hardware prototype of the proposed ISC-TaB converter and conventional two-phase series-capacitor tapped Buck converter (2ph-TaB) are designed and tested. The application is targeted at telecom with 48-V input and 3.3 V/20 A output. The test results are compared between these two converters. A peak efficiency of 95.6% is achieved on the proposed ISC-TaB and the efficiency of the ISC-TaB over all load range is at least 1% higher than that of 2ph-TaB.

Index Terms—dc-dc power converters, pulse width modulation converters, switched capacitor circuits, switching converter, zero voltage switching.

I. INTRODUCTION

HIGH step-down dc/dc converters are widely utilized in industrial, automotive, and telecommunication areas [1]–[14]. Driven by big data and cloud computing, data center power delivery is becoming more critical and high-efficiency power conversion is becoming more and more important. In data center application area, popular voltage conversion ratio includes 60 V/48 V/24 V to 5 V/3.3 V/1.8 V [10].

Buck converter is the most popular topology for dc/dc step down conversions due to its simple implementation and low cost. It is commonly utilized in consumer's electronics, automobile, and industrial applications [15]–[17]. However, for a typical 2-level Buck converter, with the increase of voltage

step-down ratio, super narrow on-time and high current pulse going through the high-side device cannot be easily handled by silicon power switches. Meanwhile, super small duty-cycle requires that control circuit have higher pulselwidth modulation (PWM) resolution which is hard to implement. This limits the application of 2-level Buck converters in high step-down conversion area. 3-level Buck converter [19]–[21] can double the turn-ON time since the output voltage on switch node is half of the input voltage. However, with the same die area, the conduction loss of 3-level is usually higher than that of 2-level Buck converters since the current has to go through two switches at the same time. In addition, although 3-level Buck converter can double the step-down conversion ratio, the step-down ratio cannot be further pushed up.

Series-capacitor Buck (SC-Buck) converter is a step-down dc/dc converter that combines a switched capacitor circuit and a multiphase buck converter together [8], [22]–[24]. Compared with conventional Buck converter, the beneficial characteristic includes smaller size, higher efficiency, and automatic current sharing [1]–[4]. As shown in Fig. 1(a), two inductors are utilized with interleaving operation to cancel the current ripple on the output capacitor and the inductor size can also be reduced [3], [23]. As indicated by Fig. 1(b), the voltage on both switching nodes is half of the input voltage due to the series capacitor. Compared with 3-level Buck converter, the conduction loss is reduced since the freewheeling only goes through one power device. However, this topology limits the maximum output voltage to $\frac{V_{in}}{4}$. This idea is further developed in [2] to achieve a higher step-down ratio. Switch node voltage in [2] is $\frac{V_{in}}{3}$ and the maximum output voltage is $\frac{V_{in}}{6}$.

Another trend to achieve a high step-down ratio is to utilize magnetic components. These solutions include full-bridge converter with current-doubler rectifier [26]–[28], LLC [29], [30], Sigma converters [18], [29], and tapped inductor Buck converters [6], [7], [9]–[12]. Full-bridge converter cannot achieve zero-voltage switching (ZVS) for all primary switches at light load, causing an efficiency drop at light-loading conditions. In addition, the bulky inductors at output side impact the power density. LLC converter can deliver power with high efficiency [31] at the resonant frequency. However, the dynamic performance is limited by the control method and the efficiency will drop quickly if the working point is not at resonant frequency. To solve this problem, Sigma converter is proposed which combines a LLC converter with a Buck converter. LLC is optimized to work at resonant frequency to maintain very high efficiency and Buck converter focus on load transient response. However,

Manuscript received May 14, 2018; revised August 10, 2018; accepted October 5, 2018. Date of publication October 21, 2018; date of current version May 2, 2019. Recommended for publication by Associate Editor M. M. Peretz. (*Corresponding author: Lanhua Zhang*.)

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Digital Object Identifier 10.1109/TPEL.2018.2877309

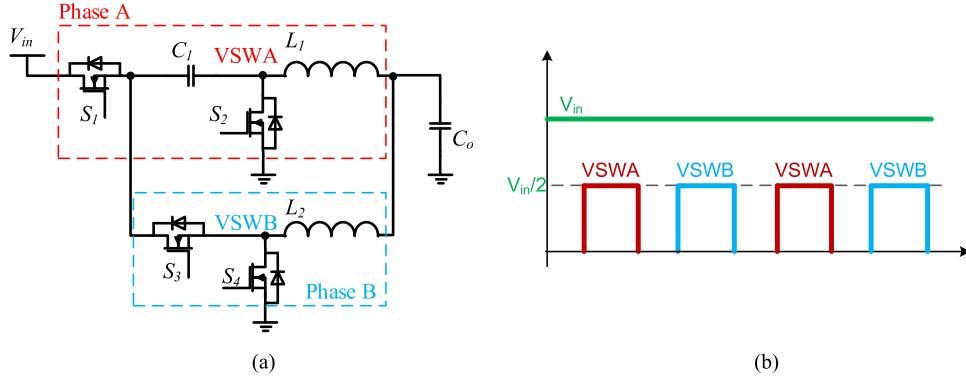
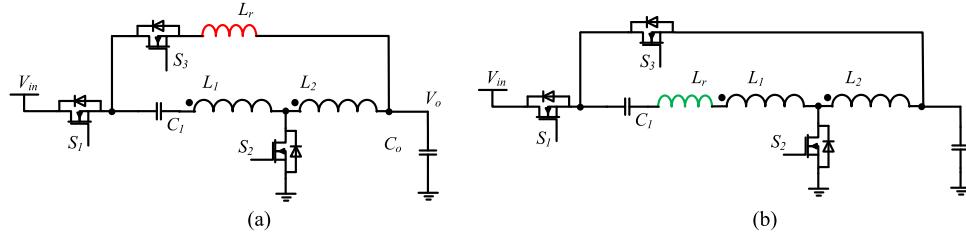
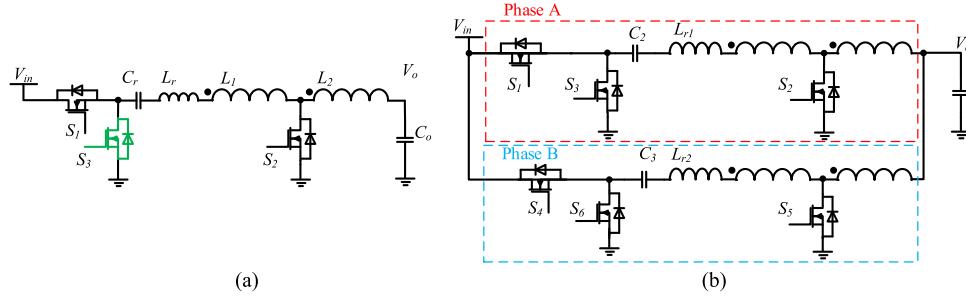


Fig. 1. (a) SC-Buck converter. (b) Operating waveforms.

Fig. 2. (a) HTB Buck converter. (b) SC-TaB converter with S_3 source connected to output.Fig. 3. (a) SC-TaB with S_3 source connected to ground. (b) 2ph SC-TaB.

since LLC converter handles most of the power at steady state and Buck converter handles most of the power at transition, both LLC and Buck converter have to be designed with capability to handle the whole system power. Meanwhile, control complexity is increased due to the parallel structure.

Tapped inductor Buck converter was originally proposed to handle high step-down ratio power conversion [5]–[7]. However, the leakage inductance of the tapped inductor resonates with the switch capacitance, causing additional voltage ring. Hybrid-transformer-based (HTB) Buck converter added one more switch (S_3) and an inductor to obtain soft-switching operation and lower voltage ring [7] as shown in Fig. 2(a). By utilizing the leakage inductance of the tapped inductor as the resonant inductor, series-capacitor tapped Buck (SC-TaB) converter is drawn in Fig. 2(b). By changing the source connection of S_3 from output to ground, another high step-down topology can be obtained [10]–[13], as shown in Fig. 3(a). The two-phase (2ph) interleaved configuration of this converter is shown in Fig. 3(b). Compared with the converters in Fig. 2, converters in

Fig. 3 have simple gate driver configuration. In this paper, unless stated otherwise, SC-TaB in this paper indicates the converters in Fig. 3(a) and 2ph SC-TaB indicated the converter in Fig. 3(b).

The main benefits of SC-TaB and 2ph SC-TaB are ZVS for all switches allowing high conversion efficiency. However, with the increase of the step-down ratio, the turns ratio of the coupled inductor has to increase. High turns ratio will put more stress on coupled inductor which impacts the efficiency. To overcome this drawback and considering that SC-Buck has the capability to double the step-down ratio, a new converter topology is proposed by introducing a capacitor C_1 , as shown in Fig. 4. The new topology is named as interleaved series-capacitor tapped Buck converter (ISC-TaB). The proposed converter combines the benefits of SC-Buck and SC-TaB together. Compared with conventional SC-TaB, it doubles the conversion step-down ratio, which makes this converter especially suitable for high step-down applications.

In this paper, the operation principles of the proposed ISC-TaB are introduced. By the use of mathematic soft-

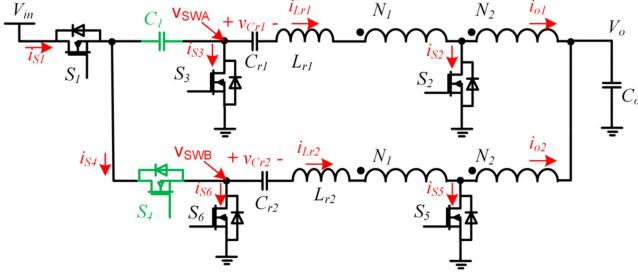


Fig. 4. Proposed ISC-TaB converter.

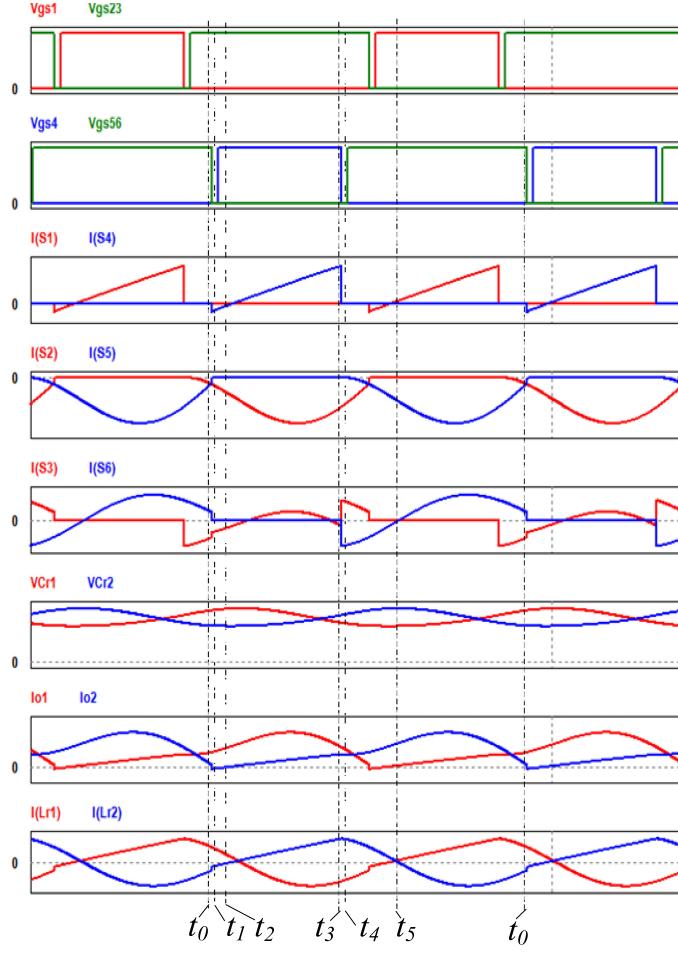
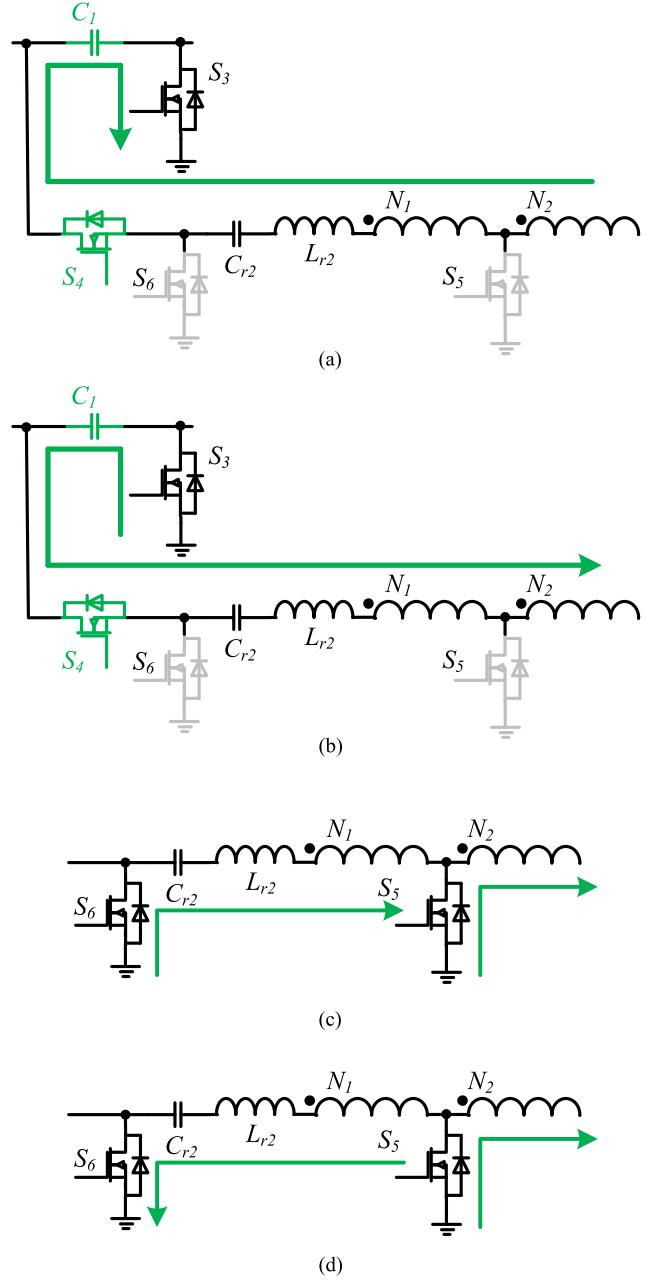


Fig. 5. Operation waveforms of the proposed ISC-TaB.

ware Mathcad, the operation waveforms are obtained. The performance is verified by both analysis and prototype hardware. Test results of ISC-TaB are compared with that of conventional 2ph SC-TaB and the efficiency of ISC-TaB is higher than 2ph SC-TaB over the whole load range.

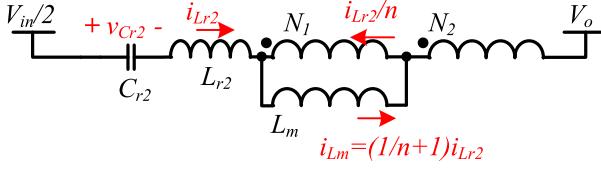
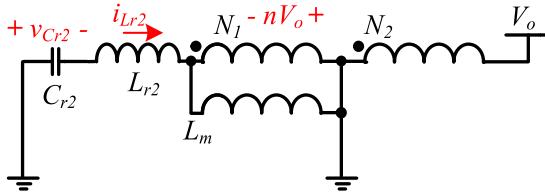
II. OPERATION PRINCIPLES

The operation principles of the proposed ISC-TaB are shown in Figs. 5 and 6. The operation for phase A and phase B is similar. Gating signals of phase A and phase B are 180° phase shifted. V_{gs1} is the gating signal for S_1 and V_{gs23} is the gating signal for S_2 and S_3 . V_{gs4} is the gating signal for S_4 and V_{gs56}

Fig. 6. Operation principles of the proposed ISC-TaB. (a) t_0-t_2 . (b) t_2-t_3 . (c) t_3-t_5 . (d) t_5-t_6 .

is the gating signal for S_5 and S_6 . $I(S1)-I(S6)$ is the current of power switches S_1-S_6 , respectively. S_2 and S_3 are turned ON and OFF at the same time. S_5 and S_6 are turned ON and OFF at the same time. In addition, voltage of resonant capacitors C_{r1} C_{r2} , current of resonant inductors L_{r1} L_{r2} , and output current of each phase are indicated in Fig. 5. In Fig. 6, phase B is utilized as an example for operation analysis and the difference between phase A and phase B will be stated.

[t_0-t_2]: The current actual direction during this time interval is shown in Fig. 6(a). During this time interval, the direction of i_{Lr1} is negative. During [t_0-t_1], the current goes through the body diode of S_4 , which prepares zero-voltage turn-ON for S_4 . At time instant t_1 , S_4 is turned ON with zero-voltage. As shown

Fig. 7. Resonant network during $[t_0-t_2]$.Fig. 8. Resonant network during $[t_3-t_5]$.

in Fig. 7, the current going through the magnetizing inductor L_m is $(\frac{1}{n} + 1)i_{Lr2}$, so the voltage across the couple inductor is $(\frac{1}{n} + 1)^2 i_{Lr2} L_m$. During this time interval $[t_0-t_2]$, C_{r2} resonates with $(\frac{1}{n} + 1)^2 L_m + L_{r2}$. At steady state, the average voltage on C_{r2} is $\frac{V_{in}}{2}$. Differential equations of the resonant network can be obtained as

$$\begin{cases} \frac{V_{in}}{2} - V_o - v_{Cr2} = L_{r2} \frac{di_{Lr2}}{dt} + L_m \frac{di_{Lr2}}{dt} \frac{(n+1)^2}{n^2} \\ i_{Lr2} = C_{r2} \frac{dv_{Cr2}}{dt}. \end{cases} \quad (1)$$

$[t_2-t_3]$: During this time interval, C_{r2} keeps resonating with $(\frac{1}{n} + 1)^2 L_m + L_{r2}$. At time instant t_2 , the actual current direction changes as indicated by Fig. 6(b).

$[t_3-t_5]$: At time instant t_3 , S_4 is turned OFF. During $[t_3-t_4]$, the current goes through the body diode of S_5 and S_6 , which prepares zero-voltage turn-ON for both S_5 and S_6 . The current direction is shown in Fig. 6(c). At t_4 , both S_5 and S_6 are turned ON at the same time. The resonant network is composed by C_{r2} and L_{r2} , as shown in Fig. 8. The differential equations during $[t_3-t_5]$ can be obtained as

$$\begin{cases} -v_{Cr2} + nV_o = L_{r2} \frac{di_{Lr2}}{dt} \\ i_{Lr2} = C_{r2} \frac{dv_{Cr2}}{dt}. \end{cases} \quad (2)$$

$[t_5-t_0]$: C_{r2} keeps resonating with L_{r2} . At time instant t_5 , the current going through the resonant inductor changes its direction. The current path and direction is shown in Fig. 6(d). At t_0 , S_5 and S_6 is turned OFF at the same time. Due to the direction of i_{Lr2} , the current will go through the body diode of S_4 and prepare zero-voltage turn-ON for the next switching cycle.

The operation of phase A is similar to phase B. A difference between phase A and phase B is noticed during $[t_0-t_3]$. Both phases has current going through S_3 , which causes the current waveform of S_3 to be different from the current of S_6 . The difference can be seen in Fig. 5.

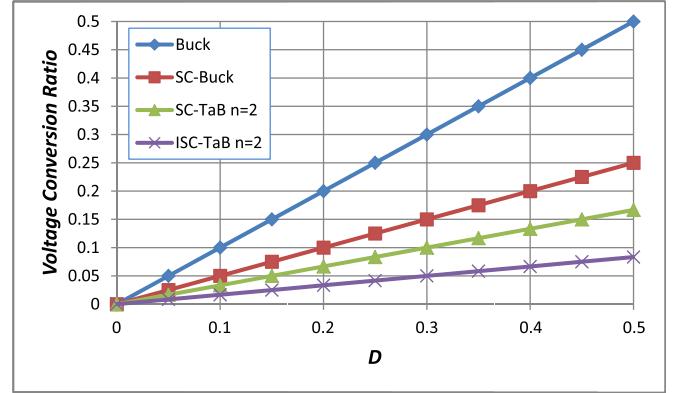


Fig. 9. Voltage conversion ratio of discussed converters.

III. ANALYSIS

A. Voltage Conversion Ratio

To simplify the analysis, V_{Cr2} is utilized to represent the average voltage across C_{r2} in a switching period. T_s is the switching period and DT_s represents the time from t_0 to t_3 .

From (1), during $[t_0, t_3]$, the average voltage across L_{r2} is

$$V_{Lr2} = \frac{\frac{V_{in}}{2} - V_o - V_{Cr2}}{1 + \frac{L_m}{L_{r2}} \cdot \frac{(n+1)^2}{n^2}}. \quad (3)$$

From the current relationship shown in Fig. 7, the voltage across L_m during $[t_0, t_3]$ can be obtained as

$$V_{Lm} = \frac{L_m}{L_{r2}} \cdot \left(1 + \frac{1}{n}\right) \cdot V_{Lr2}. \quad (4)$$

Considering (1) and (2), the voltage-second balance on L_{r2} can be obtained as

$$V_{Lr2} \cdot D + (-V_{Cr2} + nV_o) \cdot (1 - D) = 0. \quad (5)$$

The voltage-second balance on L_m can also be obtained as

$$V_{Lm} \cdot D + (1 - D)(-nV_o) = 0. \quad (6)$$

Combining (3)–(6) and assuming $L_{r1} = L_{r2} = L_r$, the voltage conversion ratio of the proposed ISC-TaB can be obtained as

$$\frac{V_o}{V_{in}} = \frac{D}{2 \cdot (n+1 + \frac{L_r}{L_m} \cdot \frac{n^2}{n+1})}. \quad (7)$$

The voltage conversion ratio of Buck, SC-Buck, SC-TaB, and ISC-TaB are drawn in Fig. 9. As shown in (7) and Fig. 9, the conversion ratio of the proposed ISC-TaB converter is half of the SC-TaB [9]. As aforementioned, the proposed ISC-TaB is a suitable topology for high step-down dc/dc applications.

B. Waveform Derivation

The current waveforms of S_1 and S_4 can be derived based on the input power of the proposed converter. The derivation of i_{S4} is utilized as an example in this section. P_{in} represents the total input power of the proposed converter. $I_{S4,\text{avg}}$ is the average

current of S_4 and it can be obtained by

$$I_{S4\text{-avg}} = \frac{P_{\text{in}}/2}{V_{\text{in}}/2}. \quad (8)$$

To get the minimum value of i_{S4} , the current of L_{r2} during $[t_0, t_3]$ is assumed to be linear. The minimum current of i_{S4} can be derived by

$$i_{S4\text{-min}} = I_{S4\text{-avg}} - \frac{DT_s}{2} \cdot \frac{V_{\text{Lr2}}}{L_r} \quad (9)$$

where V_{Lr2} is defined in (3).

$[t_0, t_3]$: Voltage on C_{r2} at t_0 is assumed as v_{Cr0} . Current of L_{r2} at t_0 is equal to $i_{S4\text{-min}}$. $C_{r1} = C_{r2} = C_r$. Differential equations in (1) can be solved as

$$\begin{cases} v_{\text{Cr2_D}}(t) = \frac{i_{S4\text{-min}}}{C_r \omega_1} \sin \omega_1 t + \left(v_{\text{Cr0}} - \left(\frac{V_{\text{in}}}{2} - V_o \right) \right) \\ \cos \omega_1 t + \frac{V_{\text{in}}}{2} - V_o \\ i_{\text{Lr2_D}}(t) = -C_r \omega_1 \left(v_{\text{Cr0}} - \left(\frac{V_{\text{in}}}{2} - V_o \right) \right) \sin \omega_1 t \\ + i_{S4\text{-min}} \cos \omega_1 t \end{cases} \quad (10)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{[(\frac{1}{n}+1)^2 L_m + L_r] \cdot C_r}}.$$

$[t_3, t_0]$: The value of $v_{\text{Cr2_D}}(t)$ and $i_{\text{Lr2_D}}(t)$ at the end of the resonant process [$i_{\text{Lr2_D}}(DT_s)$ and $v_{\text{Cr2_D}}(DT_s)$, respectively] is the initial state of the resonant process during $[t_3, t_0]$. Then by the use of $i_{\text{Lr2_D}}(DT_s)$ and $v_{\text{Cr2_D}}(DT_s)$, the differential equations in (2) can also be solved as follows:

$$\begin{cases} v_{\text{Cr2_D'}}(t) = \frac{i_{\text{Lr2_D}}(DT_s)}{C_r \omega_2} \sin \omega_2 t + (v_{\text{Cr2_D}}(DT_s) - nV_o) \\ \times \cos \omega_2 t + nV_o \\ i_{\text{Lr2_D'}}(t) = -C_r \omega_2 (v_{\text{Cr2_D}}(DT_s) - nV_o) \sin \omega_2 t \\ + i_{\text{Lr2_D}}(DT_s) \cos \omega_2 t \end{cases} \quad (11)$$

$$\text{where } \omega_2 = \frac{1}{\sqrt{L_r C_r}}.$$

At steady state, the value of v_{Cr0} at the start point of the switching cycle t_0 is same as that at the end point of the switching cycle. To solve v_{Cr0} , the following equation can be utilized:

$$v_{\text{Cr2_D'}}((1-D)T_s) = v_{\text{Cr0}}. \quad (12)$$

In this paper, the value of v_{Cr0} is solved in Mathcad.

In (10), the current waveform of L_{r2} is obtained. Based on this and (4) and (6), the magnetizing current i_{Lm} can be obtained.

$$i_{\text{Lm}}(t) = \begin{cases} \left(1 + \frac{1}{n}\right) i_{\text{Lr2_D}}(t), & 0 < t < DT_s \\ \left(1 + \frac{1}{n}\right) i_{\text{Lr2_D}}(DT_s) - \frac{nV_o}{L_m}(t - DT_s), & DT_s \leq t \leq T_s. \end{cases} \quad (13)$$

Other waveforms, such as current going through all switches and output current, can be obtained based on these derived waveforms and no further derivation of other waveforms are

included in this paper. Based on these derived waveforms, the rms current of each power switches and inductor winding can be obtained and the voltage rating of the resonant capacitor can be obtained. Derived waveforms are shown in Fig. 10 with parameters from Table II. These data are useful in the converter design and efficiency optimization.

C. ZVS Transition

Combining (10) and (11), the current going through the resonant inductor can be solved. To ensure ZVS operations of S_1 and S_4 with different input voltage and different load current, sign of i_{Lr1} and i_{Lr2} should be negative enough when S_3 or S_6 is turned OFF. To better understand the ZVS transition, the equivalent circuit when S_3 is turned OFF and S_1 is going to turn ON is shown in Fig. 11. At this time, S_2 and S_6 are still ON, so they are directly connected to ground in the equivalent circuit. After S_3 is turned OFF, the left-over current on L_{r1} will charge C_{ds3} and C_{ds4} , discharging C_{ds1} . During this interval, the following differential equation can be obtained:

$$\begin{cases} C_{\text{ds1}} \frac{d(V_{\text{in}} - v_{\text{C1}} - v_{\text{SWA}})}{dt} - i_{\text{Lr1}} \\ = (C_{\text{ds3}} + C_{\text{ds4}}) \frac{dV_{\text{SWA}}}{dt} \\ L_{r1} \frac{di_{\text{Lr1}}}{dt} = v_{\text{SWA}} - v_{\text{Cr1}} - V_{\text{Pri}}. \end{cases} \quad (14)$$

Initial conditions are: $i_{\text{Lr1}}(0) = I_{\text{Lr1_0}}$, $v_{\text{SWA}}(0) = 0$, where $I_{\text{Lr1_0}}$ is the end state of resonance and the value can be obtained from (11). To simplify the analysis, v_{Cr1} and v_{C1} can be seen as constant during the ZVS transition and assume $v_{\text{Cr1}} = v_{\text{Cr0}}$ and $v_{\text{C1}} = \frac{V_{\text{in}}}{2}$. V_{pri} can be obtained based on turns ratio and output voltage, so $V_{\text{pri}} = -nV_o$. Then the differential equations can be solved as

$$v_{\text{SWA}}(t) = -(v_{\text{cr0}} - nV_o) \cos \omega_z t - \frac{I_{\text{Lr1_0}}}{\omega_z (C_{\text{ds1}} + C_{\text{ds3}} + C_{\text{ds4}})} \sin \omega_z t + v_{\text{cr0}} - nV_o \quad (15)$$

$$\omega_z = \frac{1}{\sqrt{L_{r1}(C_{\text{ds1}} + C_{\text{ds3}} + C_{\text{ds4}})}}. \quad (16)$$

To ensure zero-voltage turn-ON of S_1 , $v_{\text{SWA}}(t)$ has to be at least $\frac{V_{\text{in}}}{2}$ when S_1 is turned ON. This should be checked with different load current and different input voltage. If ZVS is not achieved, resonant network has to be adjusted to get lower $I_{\text{Lr1_0}}$. Meanwhile, if $I_{\text{Lr1_0}}$ is too negative, more conduction loss will be introduced, so $I_{\text{Lr1_0}}$ needs optimized design.

D. Topology Comparison

As shown in Table I, the comparison among different topologies is summarized. It can be seen that 2ph SC-TaB and ISC-TaB has the maximum switch numbers among these topologies. S_2 and S_4 of SC-Buck has the benefits to use switches with rated voltage $\frac{V_{\text{in}}}{2}$. Even the operating voltage of S_1 in SC-Buck is $\frac{V_{\text{in}}}{2}$, S_1 has to stand for input voltage V_{in} when C_1 is not charged up. So the rated voltage of S_1 in SC-Buck is V_{in} . Compared with 2ph SC-TaB, ISC-TaB has two less switches rated at V_{in} ,

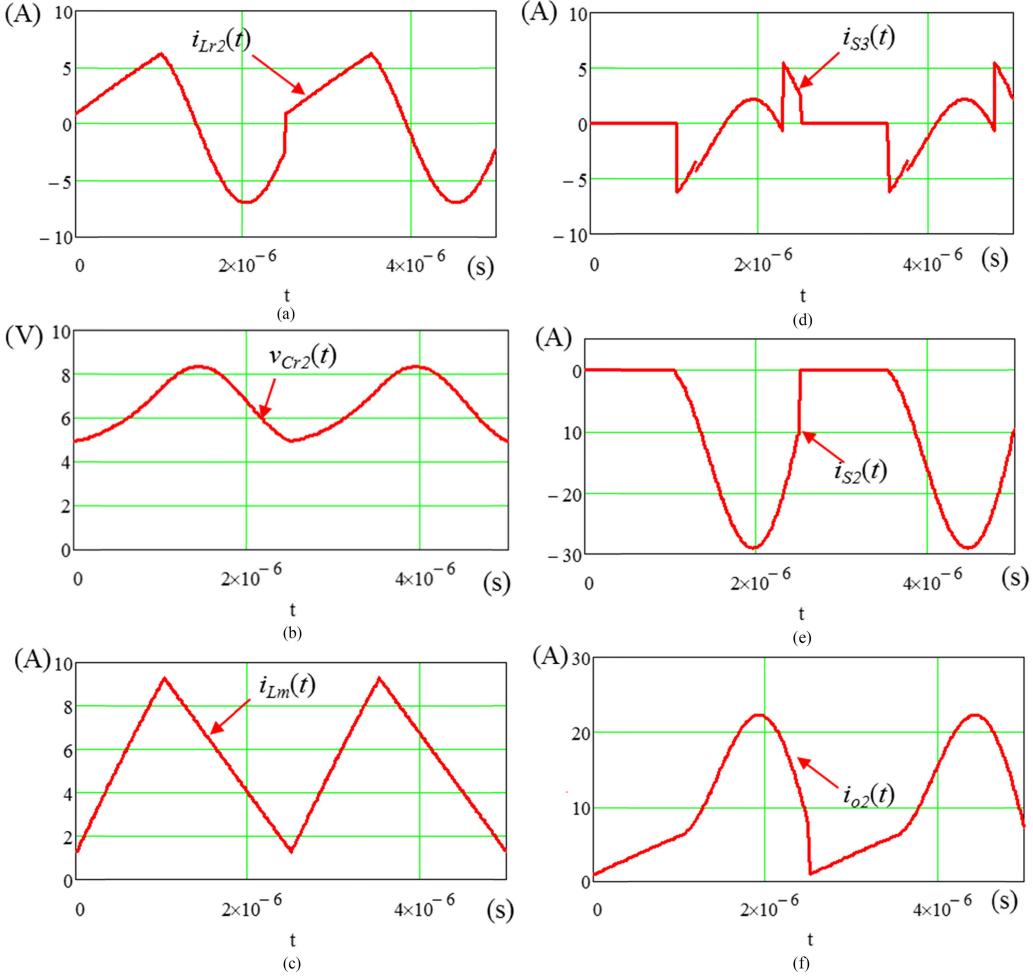


Fig. 10. Derived waveforms. (a) Current waveform of resonant inductor L_{r2} . (b) Voltage waveform of resonant capacitor C_{r2} . (c) Magnitizing current of L_m . (d) Current waveform of S_3 . (e) Current waveform of S_2 . (f) Current waveform of i_{o2} .

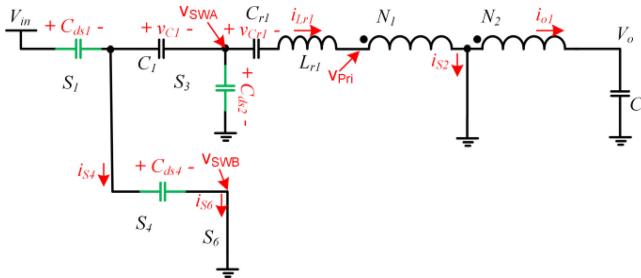


Fig. 11. S_1 turn-ON transition equivalent circuit.

benefiting from the introduction of capacitor C_1 . ISC-TaB has the minimum voltage conversion ratio among these topologies as aforementioned. However, ISC-TaB has the maximum number of capacitors among these topologies.

IV. EXPERIMENTAL VERIFICATION

A hardware prototype of proposed ISC-TaB is designed to verify the proposed topology and the picture of the hardware prototype is shown in Fig. 12. To handle the high out-

put current, the printed circuits board (PCB) board is fabricated with four layers and the thickness of each layer is 140 μm . Meanwhile, high current path is optimized in the PCB design and a 2ph SC-TaB is also tested for comparison purpose. Circuit parameters of two boards are shown in Table II. To save cost, the 2ph SC-TaB utilized the same PCB as ISC-TaB with different configurations. For the proposed ISC-TaB, J_1 is short and J_2 is open, then the source of S_4 is connected to the drain of S_1 . C_1 is populated. For the 2ph SC-TaB, J_2 is short and J_1 is open, which directly connects the drain of S_4 to V_{in} . C_1 is not populated and short instead. To achieve a fair comparison, the power level, input/output voltage is kept the same. Power switches are selected based on the rated voltage in Table I. To get a similar duty cycle between two boards, the turns ratio for ISC-TaB is set at 2:1 and the turns ratio for 2ph SC-TaB is set at 5:1.

The test setup is shown in Fig. 13. A DSP board is utilized to generate PWM signal. PWM setup can be updated by computer through joint test action group (JTAG) connector. Electronic load (E-Load) is utilized to test different loads.

Experimental waveforms of ISC-TaB are shown in Figs. 14 and 15. In Fig. 14, the waveforms of ISC-TaB with different load

TABLE I
COMPARISON AMONG DIFFERENT TOPOLOGIES

	Buck	SC-Buck	2ph SC-TaB	ISC-TaB
Switch Numbers	2	4	6	6
Switch Voltage Rating	V_{in}	$V_{in} \cdot 2$ $V_{in}/2 \cdot 2$	$V_{in} \cdot 4$ $V_{in}/(n+1) \cdot 2$	$V_{in} \cdot 2$ $V_{in}/2 \cdot 2$ $V_{in}/(n+1) \cdot 2$
Voltage Conversion Ratio	D	$\frac{D}{2}$	$\frac{D}{n+1 + \frac{L_r}{L_m} \cdot \frac{n^2}{n+1}}$	$\frac{D}{2 \cdot (n+1 + \frac{L_r}{L_m} \cdot \frac{n^2}{n+1})}$
Capacitor Numbers	1	2	3	4

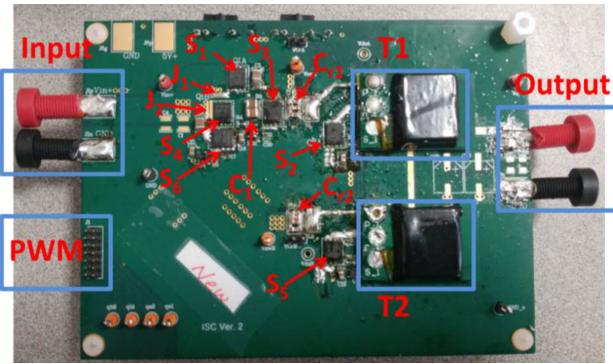


Fig. 12. Hardware prototype.

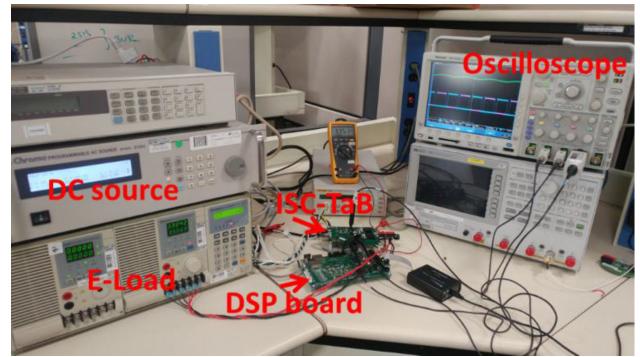


Fig. 13. Hardware test setup.

TABLE II
PROTOTYPE HARDWARE PARAMETERS

Description	2ph SC-TaB	ISC-TaB
Resonant Inductor ($L_{rl}=L_{r2}=L_r$)	120 nH	210 nH
Resonant capacitor	2 μ F	2 μ F
Magnetizing Inductance (L_m)	2.2 uH	6.6 uH
Series capacitor (C_s)	N/A	2*10 μ F
Power switches	$S_1/S_4/S_3/S_6$: BSC072N08NSS S_2/S_5 : BSC009NE2LS	S_3/S_6 : BSC035N04S S_1/S_4 : BSC072N08NSS S_2/S_5 : BSC009NE2LS
Turns ratio (n)	5	2
Rated power (P_{out})	66 W	
Input voltage (V_{in})	48 V	
Output voltage (V_o)	3.3 V	
Output current (I_o)	20 A	
Switching frequency (f_s)	400 kHz	
Magnetic core	PC95ELT18	

are shown. Waveforms include the current of the resonant inductor, voltage of the resonant capacitor, switch-node waveforms of phase A and phase B. It can be seen that the switch-node voltage is 180° phase shifted from each other, and the amplitude is half of the V_{in} due to the introduction of C_1 . The turn-ON instant of S_4 with 10-A load current is shown in Fig. 15 and it is seen that the drain-source voltage (V_{ds}) falls down before the rise of gate-source voltage (V_{gs}). This proves the turn-ON of S_4 have ZVS, as aforementioned. To achieve ZVS of S_4 , it requires

i_{Lr2} to be negative at the turn-OFF of S_6 . As shown in Fig. 14, with the increase of load, it is easier to achieve ZVS since i_{Lr2} has more negative current.

The loss breakdown of the proposed ISC-TaB is shown in Fig. 16. P_{cond} represents the conduction loss of all power switches. P_{Qg} is the gate driver loss of all power switches. $P_{Cr,Co}$ is the loss of C_{r1} , C_{r2} , and C_o . $P_{ind,core}$ indicates the core loss of the coupled inductors and $P_{ind,copper}$ indicates the conduction loss of coupled inductors. As indicated by the loss breakdown chart, the biggest portion of the loss is the copper loss of the coupled inductors. This portion of the loss could be further reduced by integrating the PCB of the coupled inductors and the main PCB together.

The efficiency curves of both ISC-TaB and 2ph SC-TaB are drawn in Fig. 17. The loss breakdown comparison of ISC-TaB and 2ph SC-TaB are shown in Fig. 18. It is seen that the efficiency of the proposed ISC-TaB is higher than SC-TaB at any load current. As for the loss breakdown, it is seen that the ISC-TaB has high conduction loss than 2ph SC-TaB. This is caused because the input current of ISC-TaB doubles the current of 2ph SC-TaB since the equivalent input voltage of ISC-TaB is reduced to half of the V_{in} . Although the voltage ratings of S_3/S_6 in ISC-TaB are reduced, the conduction loss of ISC-TaB is still higher. ISC-TaB has lower P_{Qg} , and the reason is low voltage power switches have lower gate charge in ISC-TaB. The in-

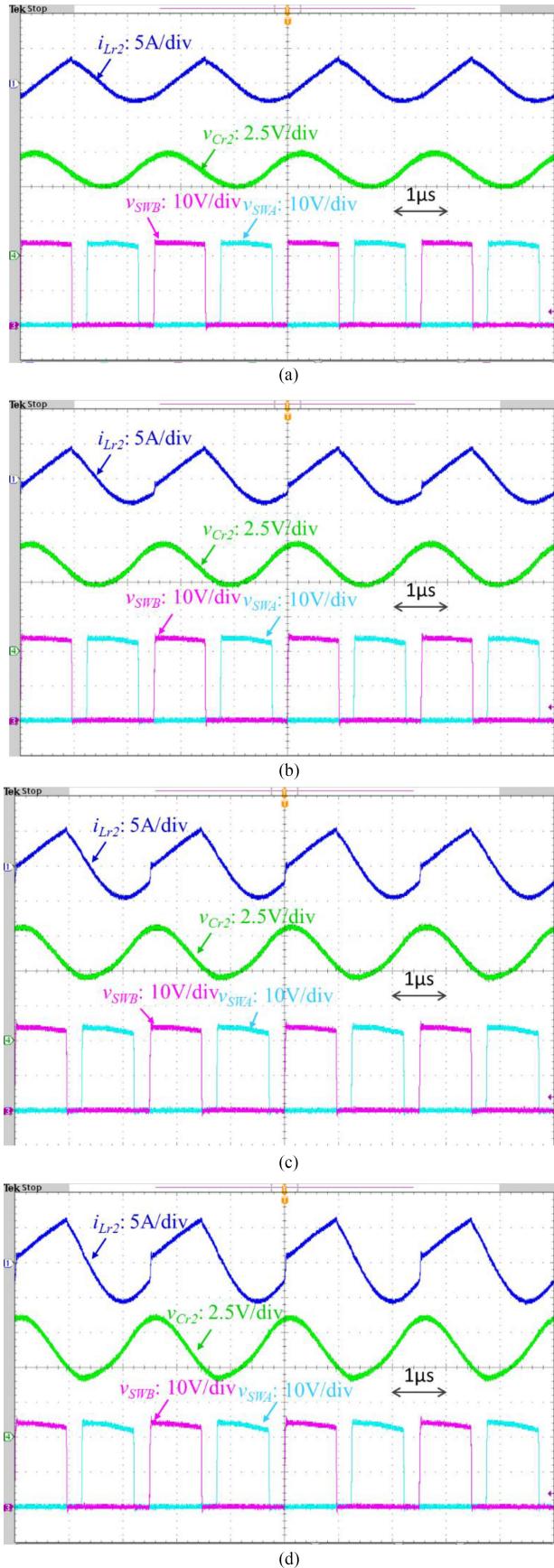


Fig. 14. Experimental waveforms of ISC-TaB. (a) $V_{in} = 48V$, $I_o = 5A$. (b) $V_{in} = 48V$, $I_o = 10A$. (c) $V_{in} = 48V$, $I_o = 15A$. (d) $V_{in} = 48V$, $I_o = 20A$.

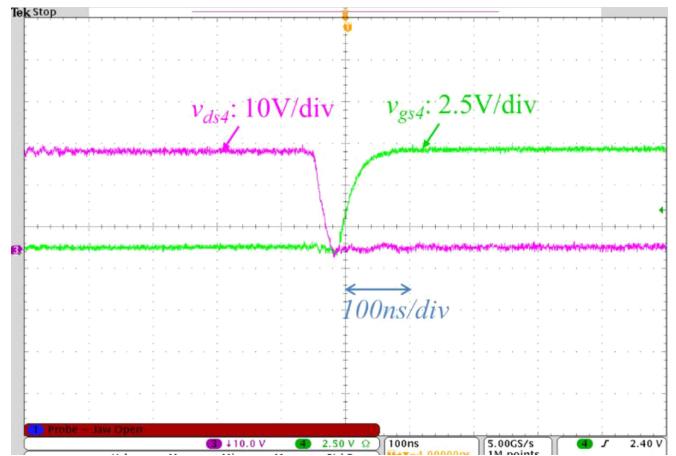


Fig. 15. ZVS proof of S_4 with 10-A load current.

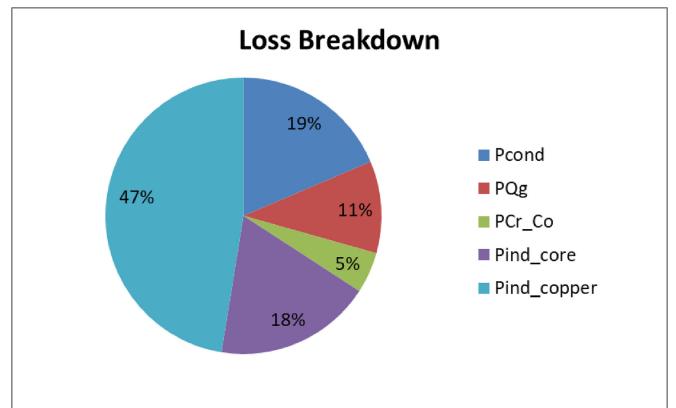


Fig. 16. Loss breakdown of the proposed converter.

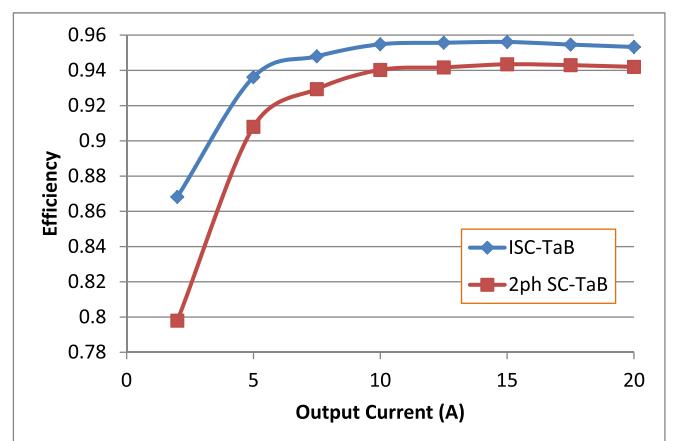


Fig. 17. Efficiency comparison.

ductor copper loss of ISC-TaB is significantly lower than 2ph SC-TaB because the turns ratio of ISC-TaB is 2:1 while the turns ratio of 2ph SC-TaB is 5:1.

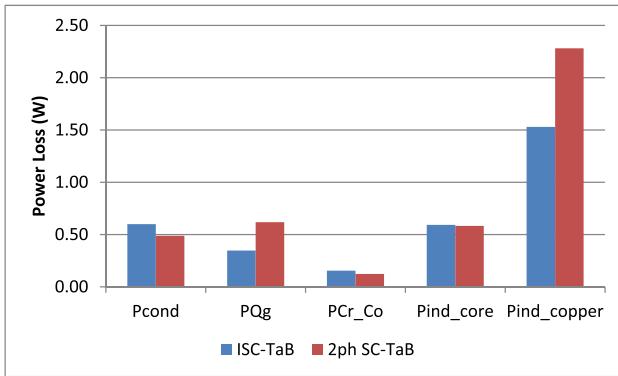


Fig. 18. Comparison of loss breakdown.

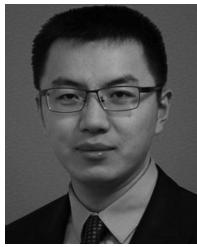
V. CONCLUSION

In this paper, the topologies for high step-down dc/dc converters are discussed and a new converter topology ISC-TaB converter is proposed, analyzed, and verified. Key features of this paper include:

- 1) The proposed ISC-TaB converter combines the benefits of SC-Buck converter and SC-TaB converter. New topology allows S_3/S_6 to use low voltage rated power switches and zero-voltage turn-ON to reduce switching loss. Meanwhile, ISC-TaB has less stress on coupled inductors since the introduction of series-capacitor C_1 doubles the step-down ratio.
- 2) The operation principles of the ISC-TaB converter are analyzed and all voltage and current waveforms are obtained. Therefore the power loss can be calculated to optimize the design. ZVS transition is analyzed and the design guideline of ZVS operation is discussed.
- 3) In order to verify the performance of the proposed ISC-TaB, the prototype hardware is designed and tested. Meanwhile, a 2ph SC-TaB converter is also designed for comparison. Based on the test results, ISC-TaB has higher efficiency over the whole load range and a peak efficiency of 95.6% is achieved.

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