VLSI Testing and Design for Testability Assignment 5

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1. How to compile codes

   Go to the folder /podem, then enter “make” in command line to compile all codes.

2. The algorithm and idea of my codes

   In problem 1-c, I referenced and modified the code void CIRCUIT::FaultSimVectors() and void CIRCUIT::FaultSim() in fsim.cc to implement this problem. I deleted the codes about branch and revised the ways which check the activated fault and choose the faulty gate. If two bridging fault values are same, the faults are non-activated.

3. Several case results

   A. Fault simulation

Circuit	Fault Coverage	
	Origin	Checkpoint
c17	100%	100%
c432	13.42%	13.42%
c880	59.60%	59.55%
c1355	62.44%	62.44%
c5315	99.45%	99.45%
c7552	98.42%	98.42%

   The fault coverage between fault simulation and checkpoint theorem is almost same.

   B. Parallel fault simulation

Circuit	Run Time (s)					
	1	4	8	16	32	64
c17	0.69	0.70	0.70	0.68	0.69	0.69
c432	185.17	147.07	124.06	115.97	110.55	109.33
c880	119.93	105.74	92.62	88.44	84.61	81.98
c1355	226.52	204.04	177.90	164.78	155.59	155.32
c5315	235.27	206.67	190.43	183.79	183.61	181.84
c7552	2648.37	2172.36	1842.13	1756.79	1676.93	1559.15

Circuit	Speed up					
	1	4	8	16	32	64
c17	1	0.985714	0.985714	1.014706	1	1
c432	1	1.25906	1.492584	1.596706	1.674989	1.69368
c880	1	1.134197	1.294861	1.356061	1.417445	1.462918
c1355	1	1.110174	1.2733	1.374681	1.455878	1.458408
c5315	1	1.138385	1.235467	1.280102	1.281357	1.29383
c7552	1	1.219121	1.437667	1.507505	1.579297	1.698599

We can see that when we simulate more faults per pass, we can spend lower simulation time

C. Parallel fault simulator

Circuit	Coverage
c17	100%
c432	12.74%
c880	58.70%
c1355	35.41%
c5315	88.94%
c7552	67.56%

I use the pattern generated from problem 1-a to simulate this problem. Some of them have lower fault coverage.