Final Report

Team 1

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Table of Content

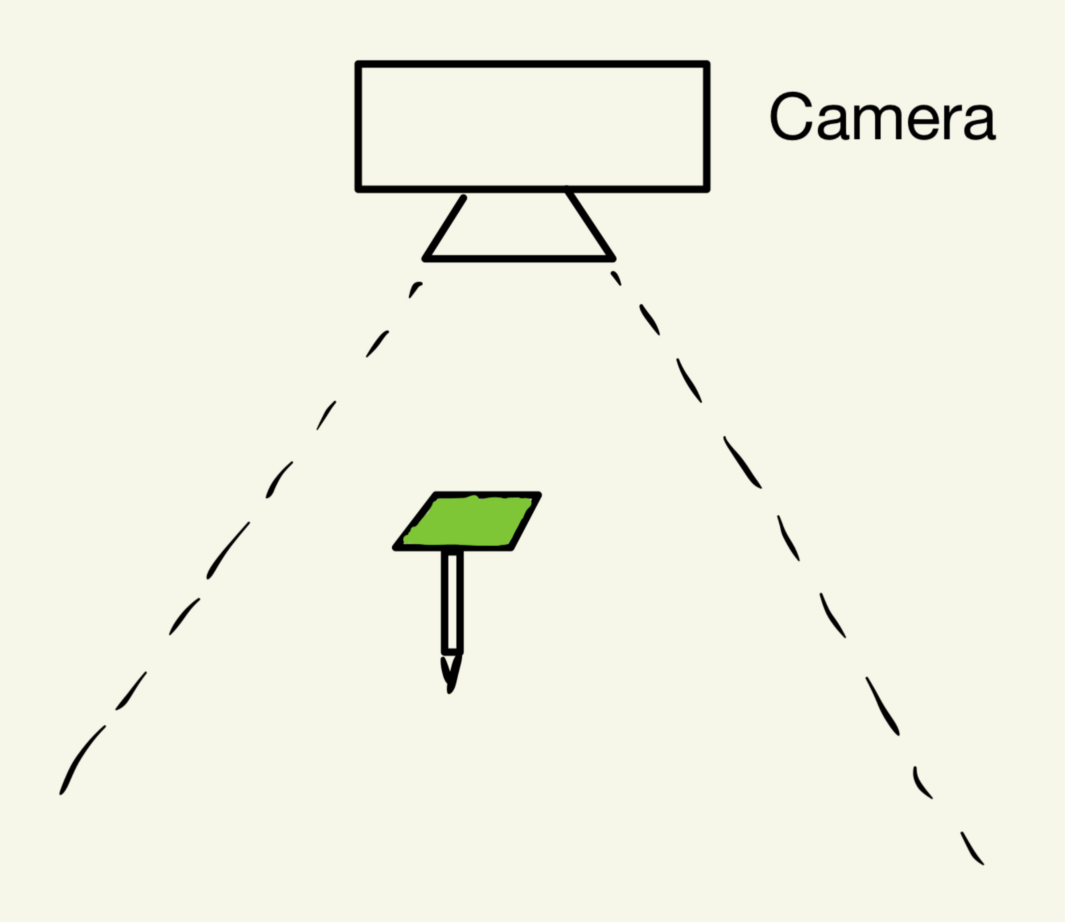
- Project Overview
- Block Level Overview
- Work Distribution
- Architecture
- Simulation/ Verification
- Implementation
- Results
- Future Work

Project Overview

- **Goal:**
- Track the position of a stylus in a 3D coordinate system using FPGA and a camera

Project Overview

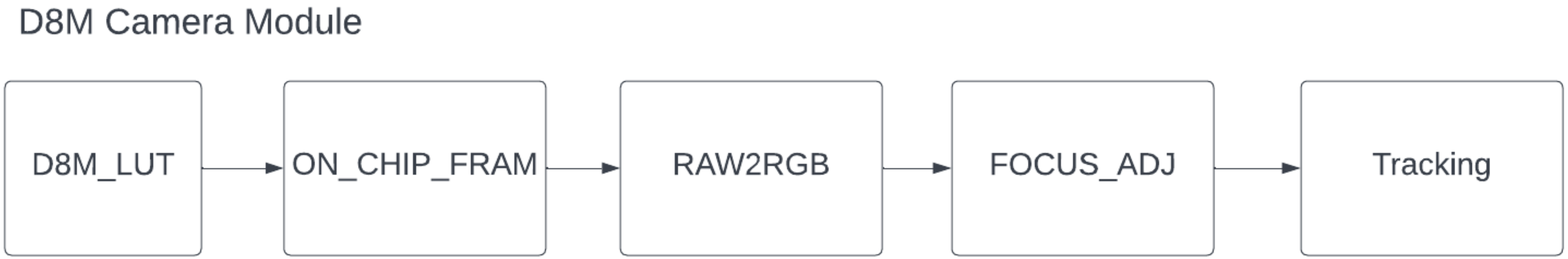
- **Our Solution:**
- Uses one overhead camera to detect a green marker attached to the back of the pen
- Obtain x and y coordinates by finding the center of the marker
- Derive z coordinate based on the size of the marker in the screen.



Block Level Overview

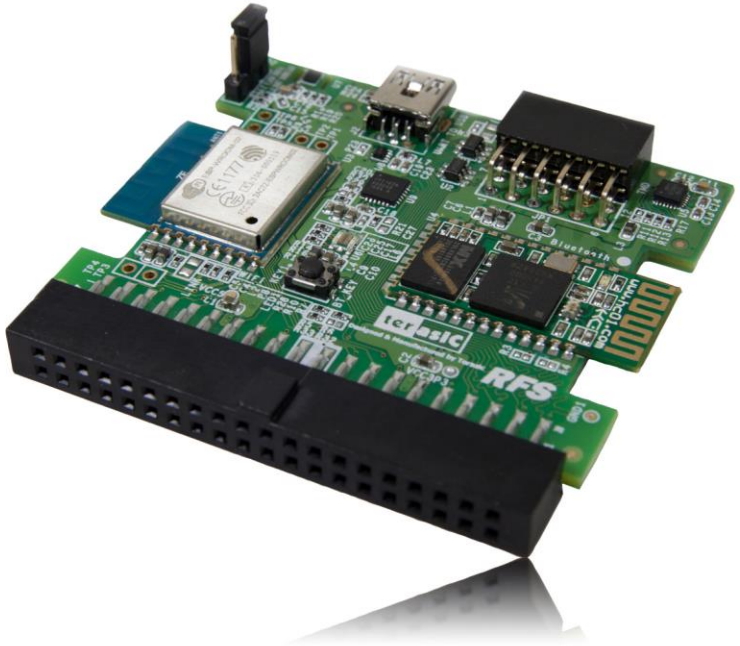
- **D8M Camera Module**
  - Control Camera (Autofocus, Frame Rate, Resolution…)
  - Convert RAW to RGB
  - Buffer Image Data
  - Control Video Output
  - Perform Location Tracking
  - Generate Highlighted Video Stream

Block Level Overview

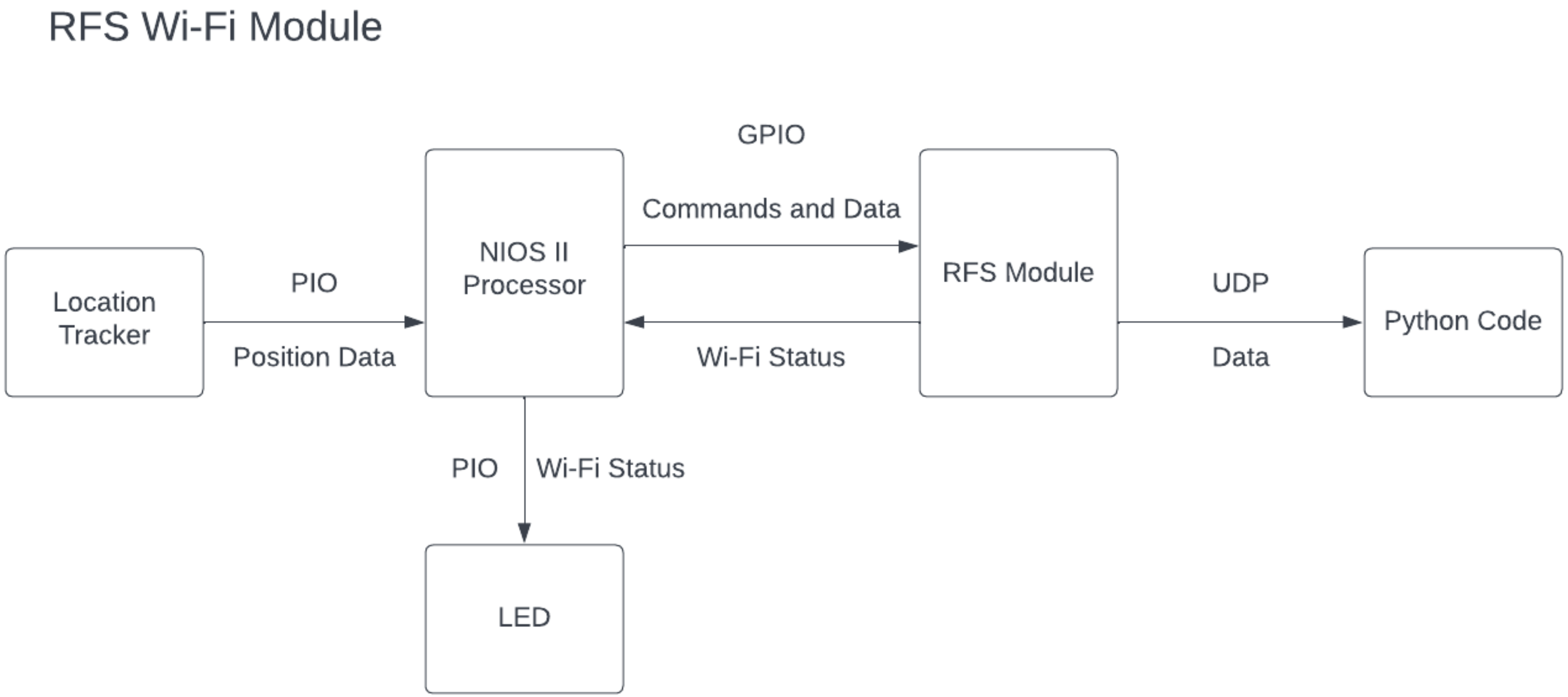


Block Level Overview

- **RFS Wi-Fi Module**
  - Establish and Maintain Wi-Fi Connection
  - Read Location Tracker
  - Create Data Payload
  - Send UDP Packet to PC



Block Level Overview



Work Distribution

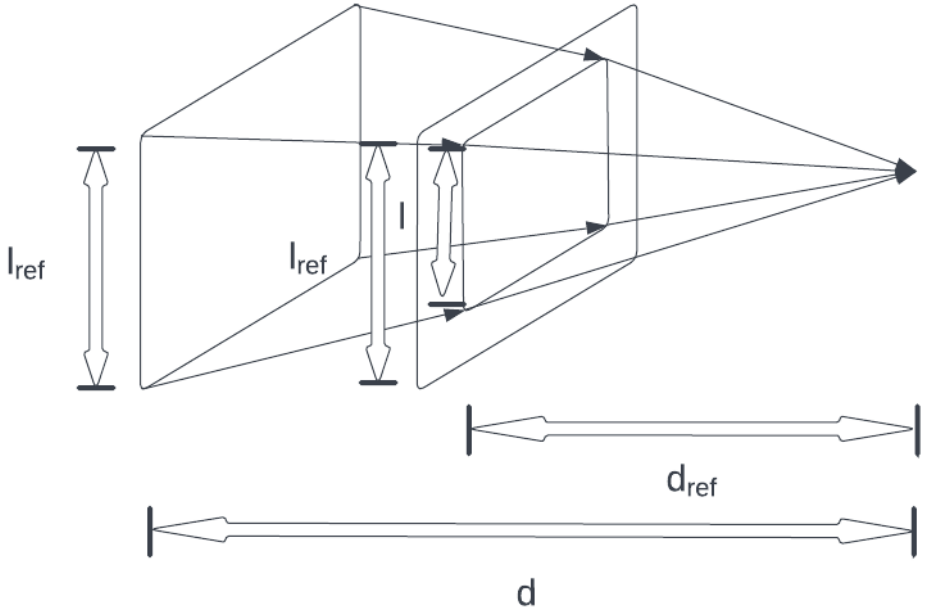
- **Brian:**
- Developed the Tracking Code and Testbench
- Optimized the Tracking Design

- **Yan:**
- Developed the camera module and integrated with Wi-Fi module
- Add location information to video output through tracker

- **Jerry:**
- Developed the Wi-Fi module and integrated with camera module
- Tested and fixed the integrated system
- Developed the Python plotting code

Architecture – Strategy

- **Location Tracker**
- Use a streaming architecture similar to Sobel
- FPGA record the line number of the first and last green pixels it sees to obtain y coordinate
- Record the column number of the rightmost and leftmost green pixel to obtain x coordinate
- Use the average of the ratio of x and y pixel count of a reference position with the measured x and y pixel count to find the z coordinate

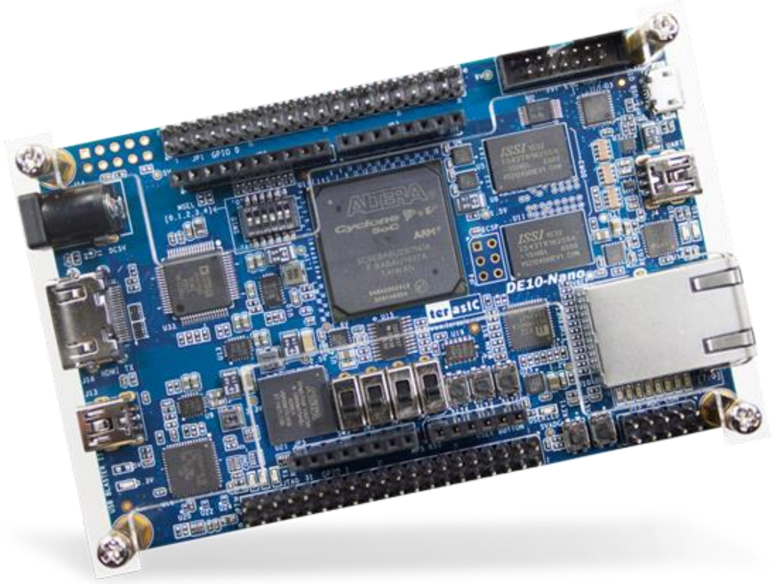


$$\frac{d_{ref}}{d} = \frac{l}{l_{ref}} \qquad d = \frac{l_{ref} d_{ref}}{l}$$

$$\frac{l_{ref}}{l} = \sqrt{\frac{w_{ref} h_{ref}}{wh}}$$

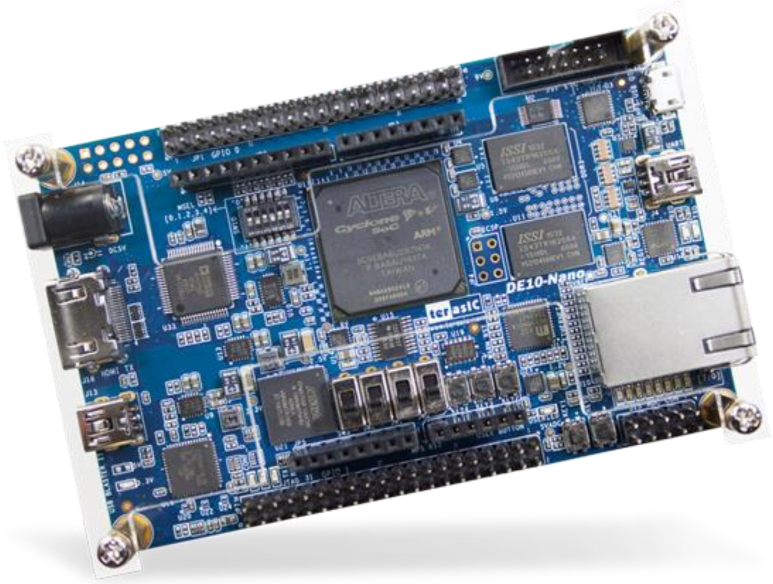
Architecture – Strategy

- **Wi-Fi and D8M Camera Module**
- Developed separately based on samples from Altera
- Modified the sample code to achieve desired functions
- Verify using simulation and on-board testing
- Merged into one large design



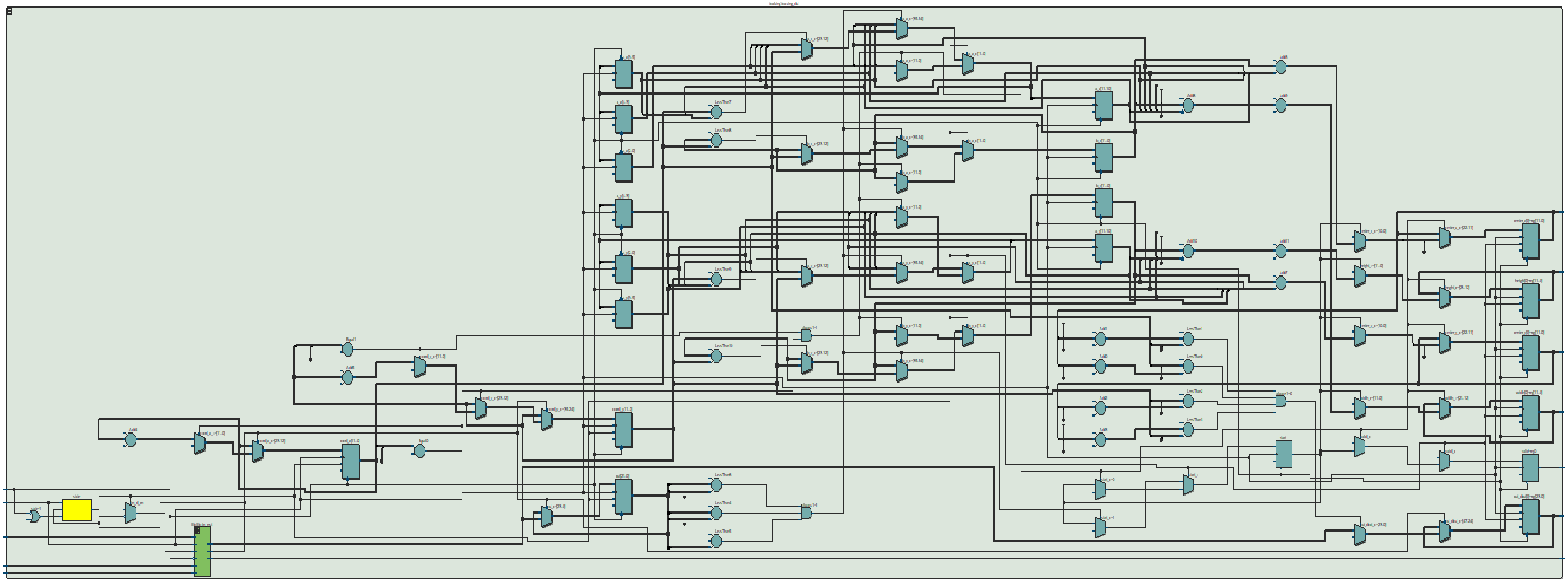
Architecture – Optimizations

- Reduce number of states in state machine
- Optimize task division between states
- Change multiplication and division to shifting
- Reduce memory overhead
- Remove unused modules



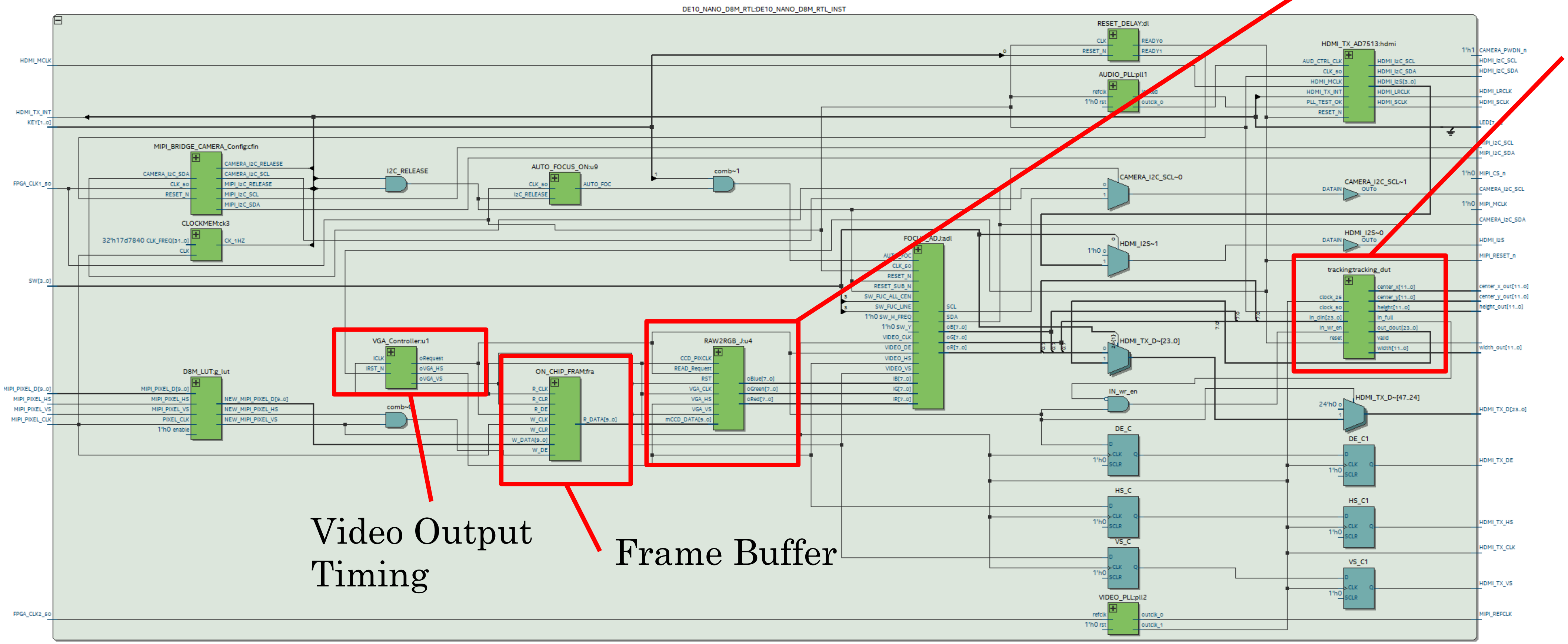
Architecture – Schematics

- **Location Tracker**



Architecture – Schematics

- **D8M Camera Module Top Level**



RAW to RGB Conversion

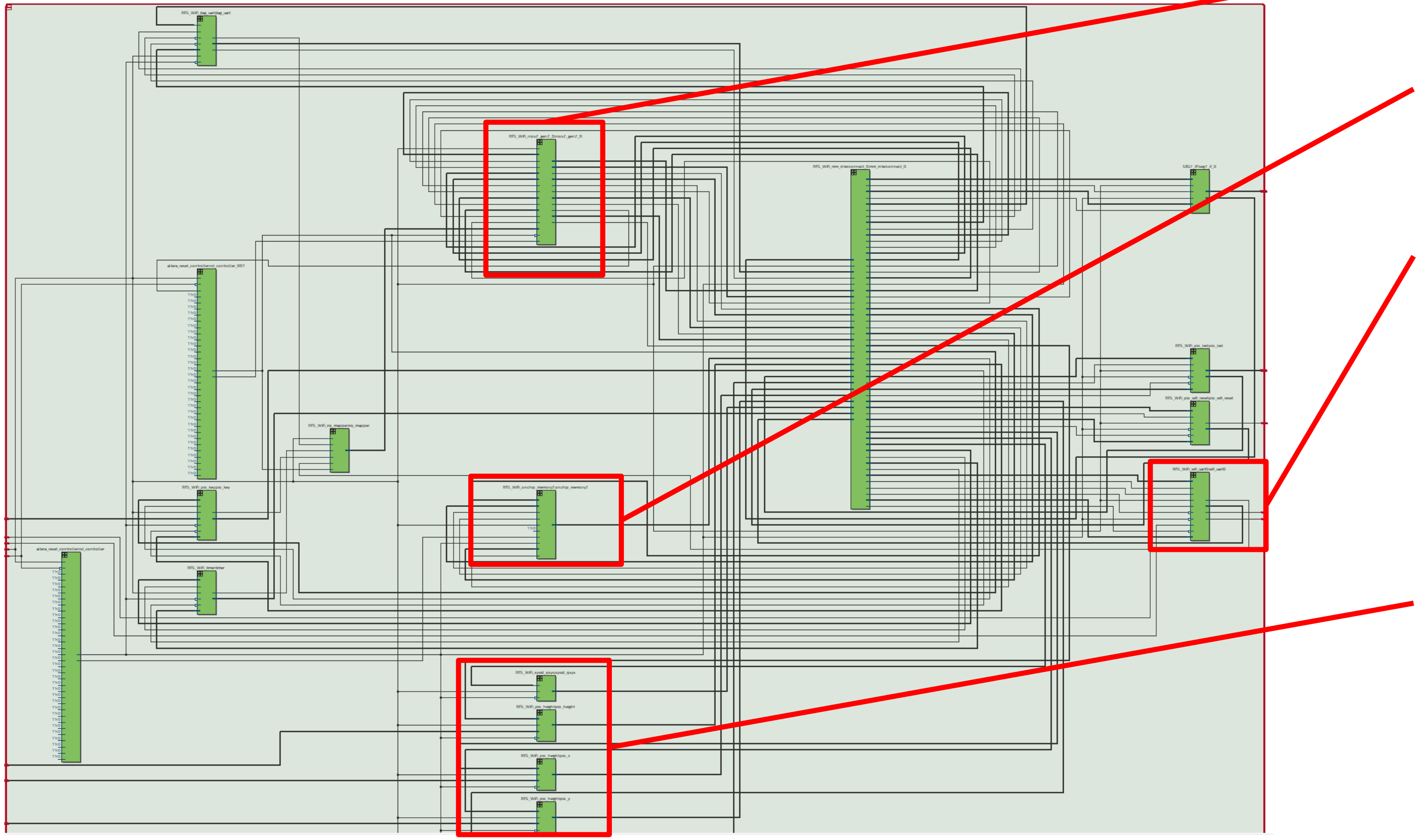
Tracker

Video Output Timing

Frame Buffer

Architecture – Schematics

- **RFS Wi-Fi Module**



NIOS II Processor

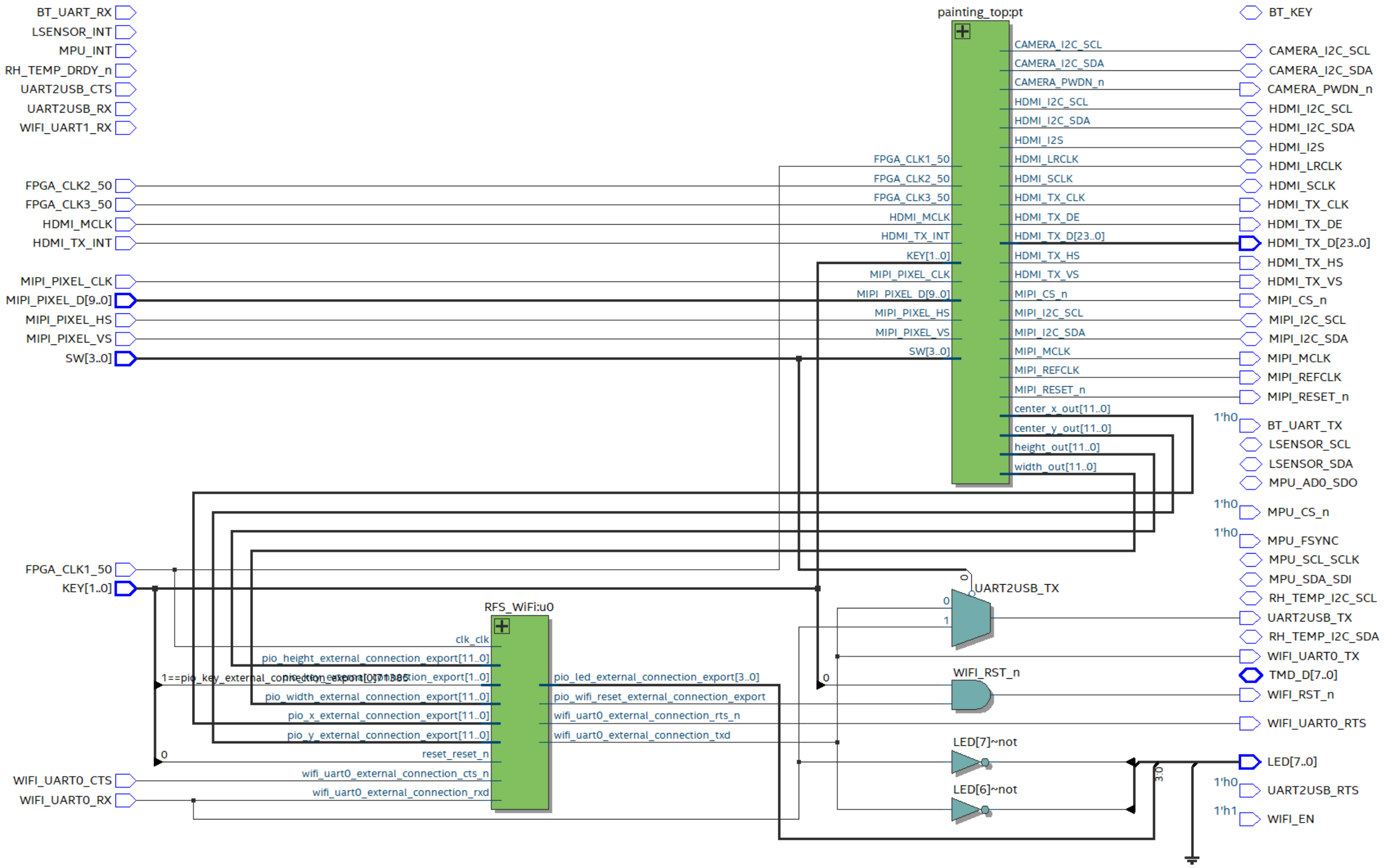
On-Chip Memory

Interface with RFS

Interface with Tracker

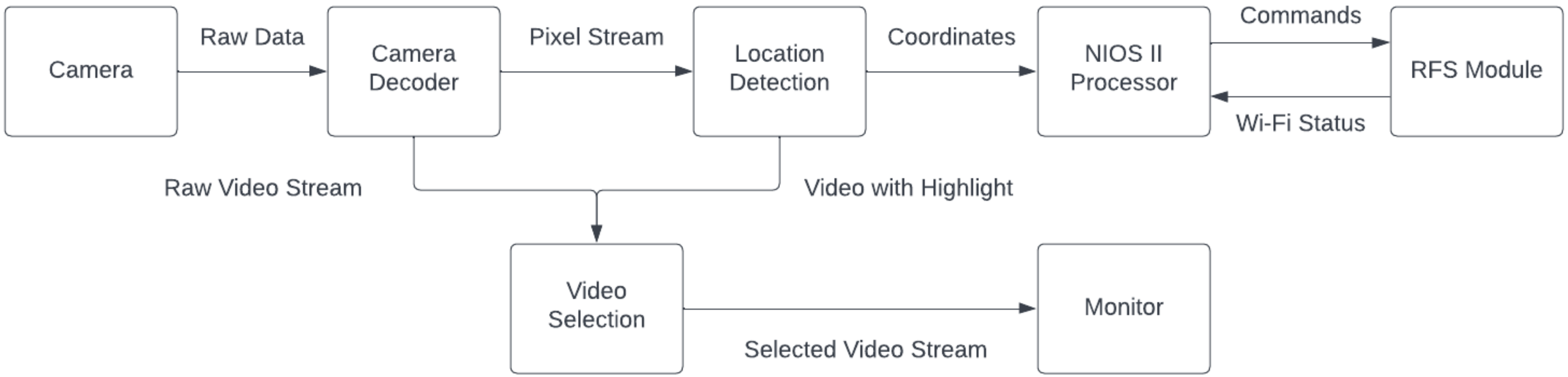
Architecture – Schematics

- **System Top Level**



Architecture – Data Flow

- **Structure of Overall Design**

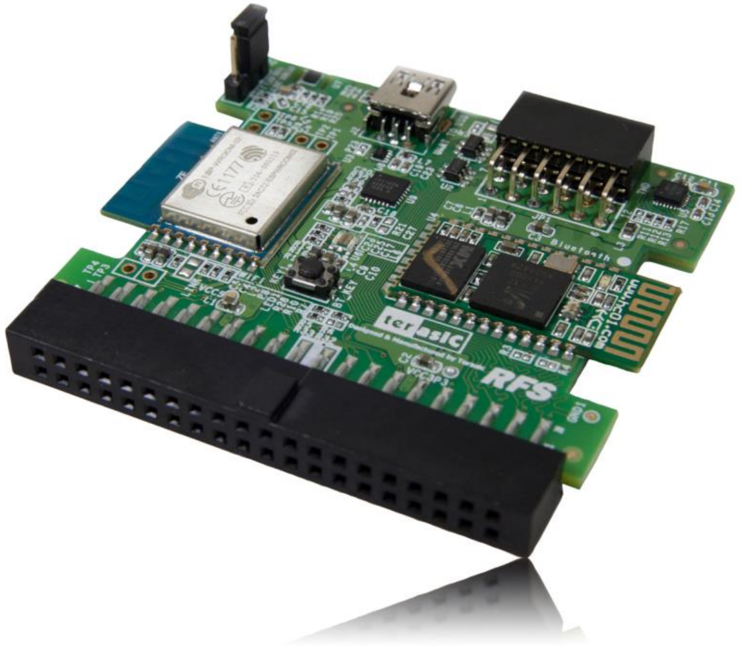


Architecture – Design Difficulties

- **D8M Camera Module**
  - Understand the functions of different modules
  - Understand the content of signals
  - Design the tracker based on VGA control signals
  - Reduce number of states so that every pixel only takes 2 cycles
  - Generate global reset signal to ensure synchronization across components

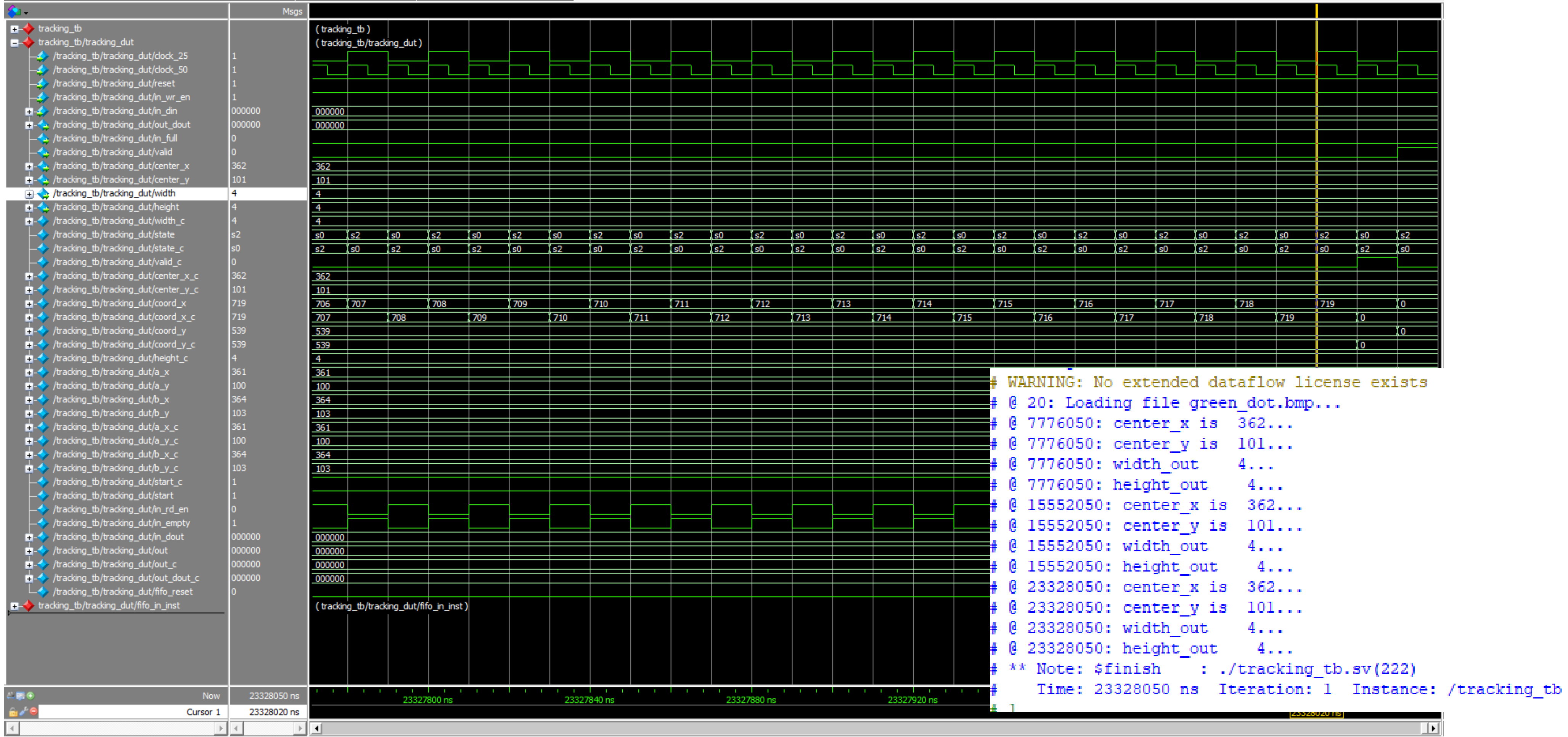
Architecture – Design Difficulties

- **RFS Wi-Fi Module**
  - Control memory utilization
  - Generate and send outputs using C Code
  - Debug with standard C Errors
  - Design and implement SOPC with Platform designer



Simulation/Verification

- **Green Region Detection**



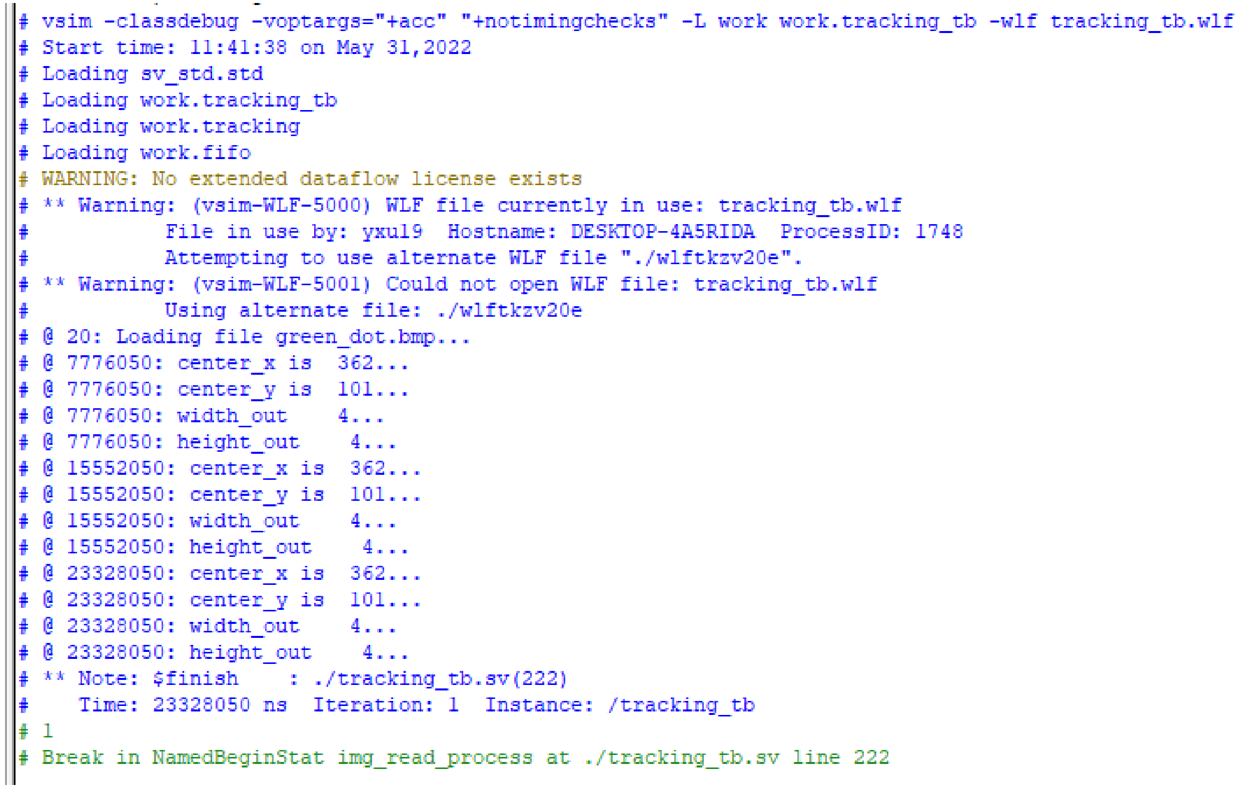
	Msgs
tracking_tb	
tracking_tb/tracking_dut	
/tracking_tb/tracking_dut/clock_25	1
/tracking_tb/tracking_dut/clock_50	1
/tracking_tb/tracking_dut/reset	1
/tracking_tb/tracking_dut/in_wr_en	1
/tracking_tb/tracking_dut/in_din	000000
/tracking_tb/tracking_dut/out_dout	000000
/tracking_tb/tracking_dut/in_full	0
/tracking_tb/tracking_dut/valid	0
/tracking_tb/tracking_dut/center_x	362
/tracking_tb/tracking_dut/center_y	101
/tracking_tb/tracking_dut/width	4
/tracking_tb/tracking_dut/height	4
/tracking_tb/tracking_dut/width_c	4
/tracking_tb/tracking_dut/state	s2
/tracking_tb/tracking_dut/state_c	s0
/tracking_tb/tracking_dut/valid_c	0
/tracking_tb/tracking_dut/center_x_c	362
/tracking_tb/tracking_dut/center_y_c	101
/tracking_tb/tracking_dut/coord_x	719
/tracking_tb/tracking_dut/coord_x_c	719
/tracking_tb/tracking_dut/coord_y	539
/tracking_tb/tracking_dut/coord_y_c	539
/tracking_tb/tracking_dut/height_c	4
/tracking_tb/tracking_dut/a_x	361
/tracking_tb/tracking_dut/a_y	100
/tracking_tb/tracking_dut/b_x	364
/tracking_tb/tracking_dut/b_y	103
/tracking_tb/tracking_dut/a_x_c	361
/tracking_tb/tracking_dut/a_y_c	100
/tracking_tb/tracking_dut/b_x_c	364
/tracking_tb/tracking_dut/b_y_c	103
/tracking_tb/tracking_dut/start_c	1
/tracking_tb/tracking_dut/start	1
/tracking_tb/tracking_dut/in_rd_en	0
/tracking_tb/tracking_dut/in_empty	1
/tracking_tb/tracking_dut/in_dout	000000
/tracking_tb/tracking_dut/out	000000
/tracking_tb/tracking_dut/out_c	000000
/tracking_tb/tracking_dut/out_dout_c	000000
/tracking_tb/tracking_dut/fifo_reset	0
tracking_tb/tracking_dut/fifo_in_inst	
Now	23328050 ns
Cursor 1	23328020 ns

```
# WARNING: No extended dataflow license exists
# @ 20: Loading file green_dot.bmp...
# @ 7776050: center_x is  362...
# @ 7776050: center_y is  101...
# @ 7776050: width_out     4...
# @ 7776050: height_out     4...
# @ 15552050: center_x is  362...
# @ 15552050: center_y is  101...
# @ 15552050: width_out     4...
# @ 15552050: height_out     4...
# @ 23328050: center_x is  362...
# @ 23328050: center_y is  101...
# @ 23328050: width_out     4...
# @ 23328050: height_out     4...
# ** Note: $finish    : ./tracking_tb.sv(222)
#    Time: 23328050 ns  Iteration: 1  Instance: /tracking_tb
```

(tracking_tb)
(tracking_tb/tracking_dut)
(tracking_tb/tracking_dut/fifo_in_inst)
23327800 ns
23327840 ns
23327880 ns
23327920 ns

Simulation/Verification

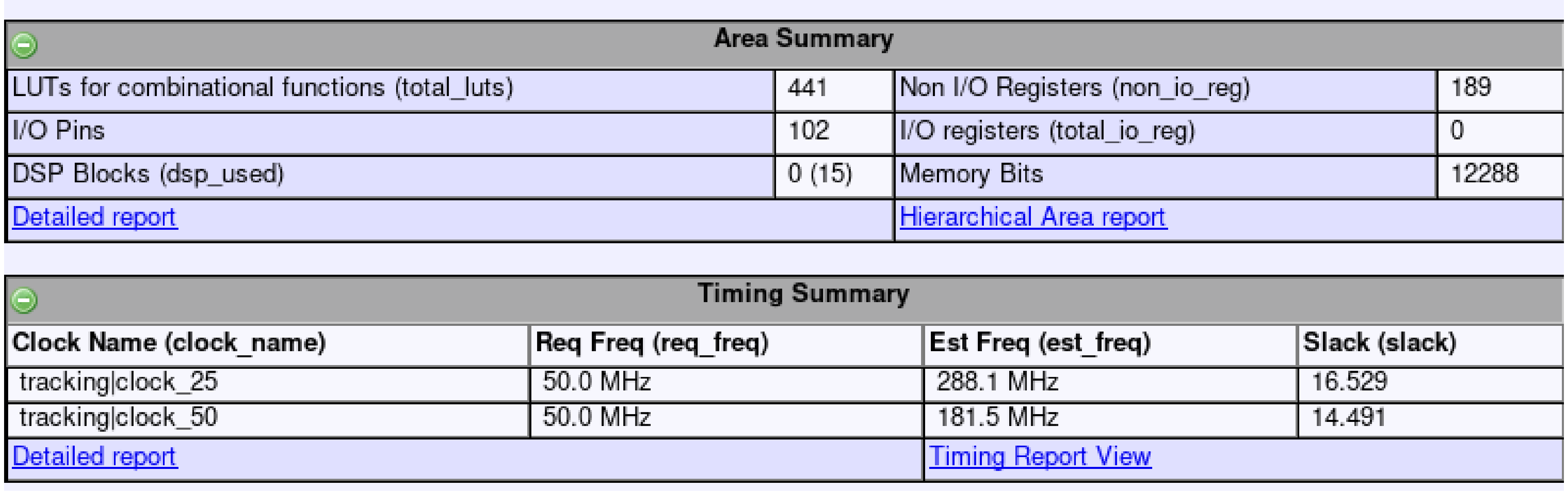
- **Serialized Green Region Detection**
  - **The counter is set to three.**
  - **Smooth execution and FIFO works fine.**



```
# vsim -classdebug -voptargs="+acc" "+notimingchecks" -L work work.tracking_tb -wlf tracking_tb.wlf
# Start time: 11:41:38 on May 31,2022
# Loading sv_std.std
# Loading work.tracking_tb
# Loading work.tracking
# Loading work.fifo
# WARNING: No extended dataflow license exists
# ** Warning: (vsim-WLF-5000) WLF file currently in use: tracking_tb.wlf
#           File in use by: yxul9  Hostname: DESKTOP-4A5RIDA  ProcessID: 1748
#           Attempting to use alternate WLF file "./wlftkzv20e".
# ** Warning: (vsim-WLF-5001) Could not open WLF file: tracking_tb.wlf
#           Using alternate file: ./wlftkzv20e
# @ 20: Loading file green_dot.bmp...
# @ 7776050: center_x is  362...
# @ 7776050: center_y is  101...
# @ 7776050: width_out    4...
# @ 7776050: height_out    4...
# @ 15552050: center_x is  362...
# @ 15552050: center_y is  101...
# @ 15552050: width_out    4...
# @ 15552050: height_out    4...
# @ 23328050: center_x is  362...
# @ 23328050: center_y is  101...
# @ 23328050: width_out    4...
# @ 23328050: height_out    4...
# ** Note: $finish    : ./tracking_tb.sv(222)
#    Time: 23328050 ns  Iteration: 1  Instance: /tracking_tb
# 1
# Break in NamedBeginStat img_read_process at ./tracking_tb.sv line 222
```

Simulation/Verification

- **Timing Analysis for Tracking Module**
  - Required Clock Frequency
    - Clock_25: 25MHz Clock_50 : 50 MHz



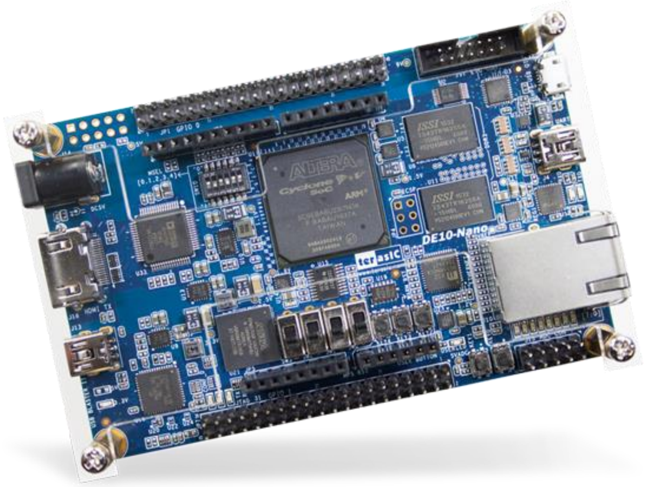
Area Summary

LUTs for combinational functions (total_luts)	441	Non I/O Registers (non_io_reg)	189
I/O Pins	102	I/O registers (total_io_reg)	0
DSP Blocks (dsp_used)	0 (15)	Memory Bits	12288
Detailed report		Hierarchical Area report	

Timing Summary

Clock Name (clock_name)	Req Freq (req_freq)	Est Freq (est_freq)	Slack (slack)
tracking|clock_25	50.0 MHz	288.1 MHz	16.529
tracking|clock_50	50.0 MHz	181.5 MHz	14.491
Detailed report		Timing Report View	

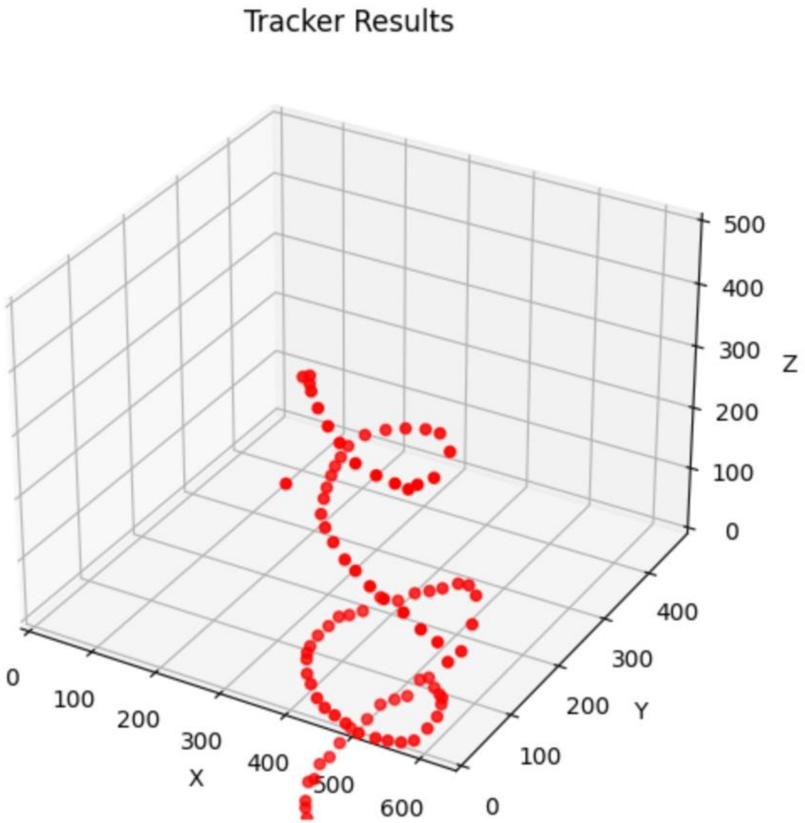
Implementation



- **Resource Utilization**
- Logic utilization (in ALMs) 9,664 / 41,910 (23 %)
- Total registers 16805
- Total pins 108 / 314 (34 %)
- Total virtual pins 0
- Total block memory bits 4,317,376 / 5,662,720 (76 %)
- Total DSP Blocks 5 / 112 (4 %) Total PLLs 2 / 6 (33 %)
- Total DLLs 0 / 4 (0 %)

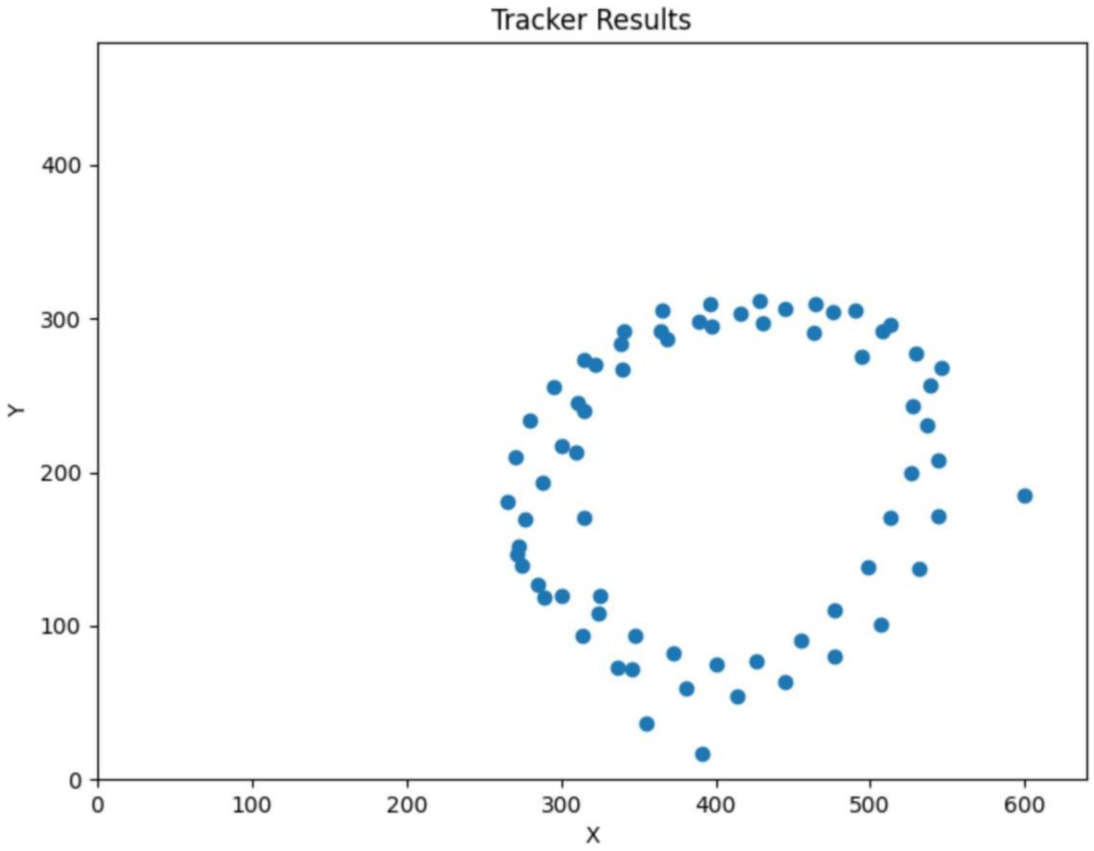
Results

- **Spiral Movement Tracking Result**



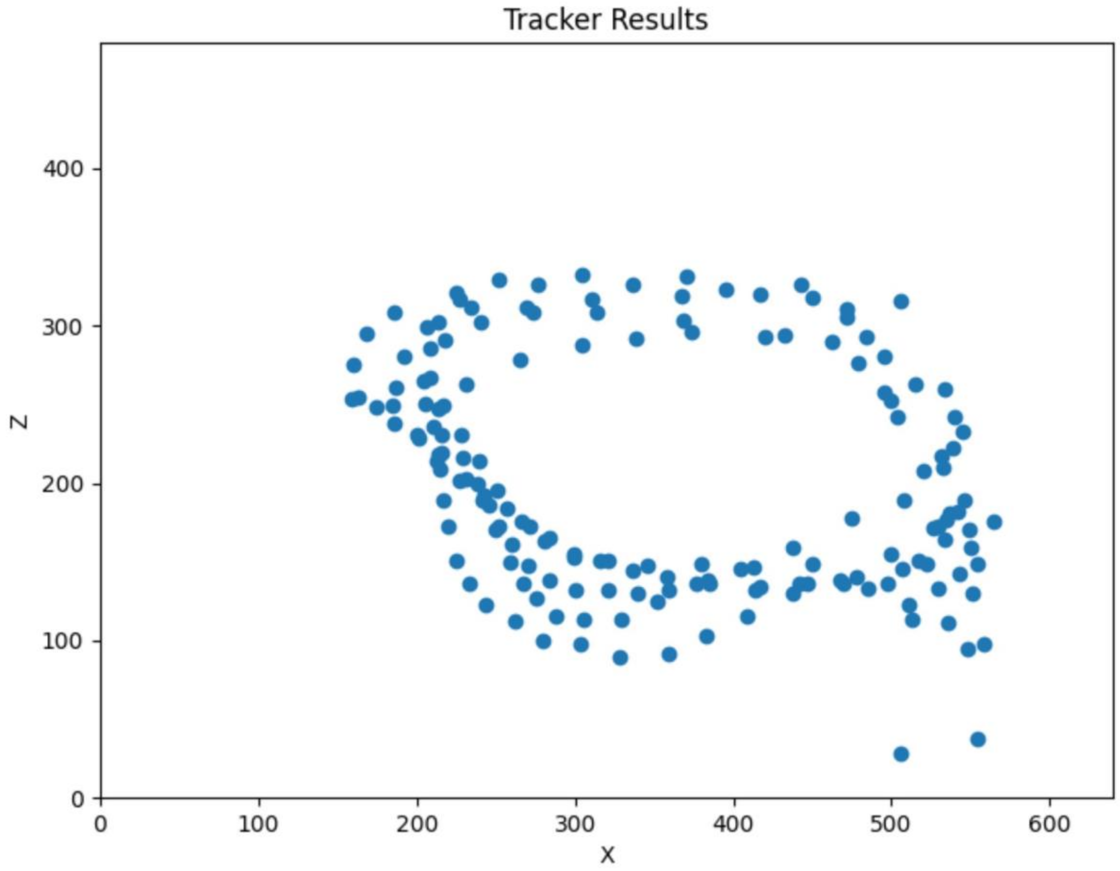
Results

- **Circle in XY Plane**



Results

- **Circle in XZ Plane**



Future Work

- Add HUD style data display using the NIOS II processor
- Support higher quality video stream
- Include additional sensors like gyro that can account for tilted markers
- Improve our coordinate calculation code to reduce the impact of noise.
  - Require continuous green pixels
  - Ignoring smaller regions.