嵌入式汇总only english

Project 1： IGBT And Driver Tester

Devices

Test IGBT(new funciton)

How to test IGBT

Test Driver Card (old function)

Test LCD

Test INA226

can get correct and precise Voltage value

Did not use the Alert\_4 pin for Alert effect before

Test AD5629R

Set the voltage or make up for the difference

It is not successful to write a difference to power supply

Old Board

D TP33(Vout) TP32（after amplifier） TP2(powe source) should be 15.25

64 0.083 0.083 17.42 1.939759036

128 0.161 0.161 17.19 1.968944099

256 0.317 0.317 16.73 1.984227129

479 0.57 0.57 15.99

512 0.629 0.629 15.81 1.988871224

1024 1.252 1.251 13.96 1.996003197

1727 20.89 2.089 11.46

2048 2.498 2.497 10.18 1.498998799

3076 3.744 3.743 6.322 1.075607801

4095 4.026 4.026 5.451 0

Test Fibre Optics

Test Timings

Test Propagation Delay

Test Desaturation

LM73,Temperature tester

Introduction

The temperature resolution is programmable, allowing the host system to select the optimal configuration

between sensitivity and conversion time.

Operation methods

Typical Read from a 2-Byte Register with Preset Pointer

Typical Pointer Set Followed by Immediate Read of a 2-Byte Register

Typical Read from a 1-Byte Register with Preset Pointer

Functional Modes

Shutdown mode

Shutdown Mode is enabled by writing a “1” to the Full Power Down Bit,

Device Functional Modes

The LM73 will always finish a temperature conversion and update the temperature registers before shutting

down.

Writing a “0” to the Full Power Down Bit restores the LM73 to normal mode.

Register Map

Pointer Register

The LM73's internal registers are selected by the Pointer register

Control/Status Register

DS3231

Introduction

The DS3231 is a low-cost, extremely accurate I2C

real-time clock (RTC) with an integrated temperaturecompensated

crystal oscillator (TCXO) and crystal.

The device incorporates a battery input, and maintains

accurate timekeeping when main power to the device

is interrupted.

The integration of the crystal resonator

enhances the long-term accuracy of the device as well

as reduces the piece-part count in a manufacturing line.

A precision temperature-compensated voltage reference

and comparator circuit monitors the status of VCC to

detect power failures, to provide a reset output, and to

automatically switch to the backup supply when necessary.

Address Map

Clock and Calendar

Alarms

The DS3231 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh.

SD Card

Read a File , using sd card. If the file is not there, it will be created;otherwise, it will be opened and written with some data

Operation Command

Commands

SD卡的命令格式

SD卡的指令由6字节(Byte)组成

Byte1:命令号

0 1 x x x x x x(命令号，由指令标志定义，如CMD39为100111即16进制0x27，那么完整的CMD39第一字节为01100111，即0x27+0x40)

Byte2-5

Command Arguments,命令参数，有些命令没有参数

Byte6

前7位为CRC(Cyclic Redundacy Check，循环冗余校验)校验位，最后一位为停止位0

Class0 :(卡的识别、初始化等基本命令集)

CMD0:复位SD 卡.

CMD1:读OCR寄存器.

CMD9:读CSD寄存器.

CMD10:读CID寄存器.

CMD12:停止读多块时的数据传输

CMD13:读 Card\_Status 寄存器

Class2 (读卡命令集):

CMD16:设置块的长度

CMD17:读单块.

CMD18:读多块,直至主机发送CMD12为止 .

Class4(写卡命令集)

CMD24:写单块.

CMD25:写多块.

CMD27:写CSD寄存器

Class5 (擦除卡命令集):

CMD32:设置擦除块的起始地址.

CMD33:设置擦除块的终止地址.

CMD38: 擦除所选择的块.

Class6(写保护命令集):

CMD28:设置写保护块的地址.

CMD29:擦除写保护块的地址.

CMD30: Ask the card for the status of the write protection bits

class7：卡的锁定，解锁功能命令集

class8：申请特定命令集

其中 class1, class3,class9：SPI模式不支持

其中 class1, class3,class9：SPI模式不支持

切换SD卡 SPI模式，从SD模式

其关键的地方就是先上 电延时大于74个时钟周期后发送复位命 令,复位成功(接收到0x01的响应)后,连续发送CMD55和ACMD41,直到响应 0X00为止，此时SD卡已经进入SPI模式。

复位，时序图

本复位分为（1）上电，（2）延时74个周期以上，（3）发送命令CMD0,(4)发送命令参数0X0000,(5)发送CRC校验0X95, (6)等待响应(7)响应0X01此时得到正确响应复位成功,否则重复以上操作直到成功为止。

（1）读CID寄存器时序图

说明：当发送命令并得到响应0X00后就开始准备接收CID寄存器中的内容，此时只要接收到起始标志0XFE后，之后的16个字节的内容即为CID 寄存器的内容。

（2）读CSD寄存器内容时序和读CID的类似，只是此时发送的命令为CMD9

(3) 读SD卡一个块(512字节)时序

(4) 写一个块(512字节)时序图

SD卡初始化过程：

1. 初始化STM32的SPI接口 使用低速模式 2. 延时至少74clock 3. 发送CMD0，需要返回0x01，进入Idle状态 4. 循环发送CMD55+ACMD41，直到返回0x00，进入Ready状态 5. 设置读写block大小为512byte 5. 把STM32的SPI设置为高速模式

读一个block块的过程

1. 发送CMD17（单块）或CMD18（多块）读命令，返回0x00 2. 接收数据开始令牌0xfe + 正式数据512Bytes + CRC 校验2Bytes

写一个block块的过程

1. 发送CMD24（单块）或CMD25（多块）写命令，返回0x00 2. 发送数据开始令牌0xfe + 正式数据512Bytes + CRC校验2Bytes

Controller: Atmel

Intrduction

Memory

The ATmega640/1280/1281/2560/2561 contains 64K/128K/256K bytes On-chip In-System Reprogrammable Flash

memory for program storage,

The ATmega640/1280/1281/2560/2561 contains 4Kbytes of data EEPROM memory

IIC

Button

Timer

Total:

• Twenty independent interrupt sources (TOV1, OCF1A, OCF1B, OCF1C, ICF1, TOV3, OCF3A, OCF3B, OCF3C, ICF3,

TOV4, OCF4A, OCF4B, OCF4C, ICF4, TOV5, OCF5A, OCF5B, OCF5C, and ICF5)

16-bit Timer/Counter (Timer/Counter 1, 3, 4, and 5)

The Timer/Counter (TCNTn), Output Compare Registers (OCRnA/B/C), and Input Capture Register (ICRn) are all

16-bit registers.

The Timer/Counter Control Registers

(TCCRnA/B/C) are 8-bit registers and have no CPU access restrictions.

Interrupt requests (shorten as Int.Req.)

signals are all visible in the Timer Interrupt Flag Register (TIFRn).

All interrupts are individually masked with the

Timer Interrupt Mask Register (TIMSKn)

ICF1/4/5 interruption

The Input Capture Register can capture the Timer/Counter value at a given external (edge triggered) event on either the Input Capture pin (ICPn) or on the Analog Comparator pins

Timer/Counter Clock Sources

The clock source is selected by the

Clock Select logic which is controlled by the Clock Select (CSn2:0) bits located in the Timer/Counter control Register

B (TCCRnB)

When a capture is triggered, the 16-bit value of the counter (TCNTn) is written to the Input Capture Register

(ICRn).

The Input Capture Flag (ICFn) is set at the same system clock as the TCNTn value is copied into ICRn

Register

If enabled (TICIEn = 1), the input capture flag generates an input capture interrupt.

The ICFn flag is automatically

cleared when the interrupt is executed.

the ICFn flag can be cleared by software by writing a

logical one to its I/O bit location.

Reading the 16-bit value in the Input Capture Register (ICRn) is done by first reading the low byte (ICRnL) and

then the high byte (ICRnH).

SPI

When configured as a Master, the SPI interface has no automatic control of the SS line. This must be handled by

user software before communication can start.

If the SPI Interrupt Enable bit (SPIE) in the SPCR

Register is set, an interrupt is requested.

SS Pin Functionality

If SS is configured as an input, it must be held high to ensure Master SPI operation

If SS is configured as an output, the pin is a general output pin which does not affect the SPI system.

Arduino Board

arduino sketch

这是arduino对使用arduino ide编辑出来的程序的专门叫法。

AVR单片机和Arduino的关系？

arduino是基于avr单片机的，只是开发了编译器和各种功能库，用起来比较方便。avr单片机最小系统烧写arduino引导程序后就可以用它的编译环境和各种功能库，当然avr单片机的功能还都是有的

Project 2: AEBI

DS2502

Feature

1k-Bit EPROM with Page-Level Write Protection

Guaranteed Unique 64-Bit ROM ID Chip for Absolute Traceability

1024 Bits Electrically Programmable Read Only Memory (EPROM)

Unique, Factory-Lasered and Tested 64-Bit Registration Number (8-Bit Family Code + 48-Bit Serial Number + 8-Bit CRC Tester)

EPROM Partitioned into Four 256-Bit Pages for Randomly Accessing Packetized Data

Subtopic 2

three main data components

1) 64-bit lasered ROM,

The first 8 bits are a 1-Wire family code.

The next 48 bits are a unique serial number.

The last 8 bits are a CRC of the first 56 bits.

2) 1024-bit EPROM

four pages of 32 bytes each

3) EPROM Status Bytes,64 bits of Status

Protocol

The memory functions required to read and program the EPROM sections of the DS2502 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM functions flow chart (Figure 9). The 1-Wire bus master must first provide one of four ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, or 4) Skip ROM.

After a ROM function sequence has been successfully executed, the bus master may then provide any one of the memory function commands specific to the DS2502

Commands

READ MEMORY [F0h]

The Read Memory command is used to read data from the 1024-bit EPROM data field

READ STATUS [Aah]

The Read Status command is used to read data from the EPROM Status data field

READ DATA/GENERATE 8-BIT CRC [C3h]

The Read Data/Generate 8-bit CRC command is used to read data from the 1024-bit EPROM data field.

WRITE MEMORY [0Fh]

WRITE STATUS [55h]

Project 3： TM4C1294XL LaunchPad

The Connected LaunchPad uses a 25 MHz crystal (Y1) to drive the main TM4C1294NCPDTI internal

clock circuit. Most software examples use the internal PLL to multiply this clock to higher frequencies up to

120 MHz for core and peripheral timing. The 25-MHz crystal is required when using the integrated

Ethernet MAC and PHY.

The Hibernation module is clocked from an external 32.768-KHz crystal (Y3).

TM4C1294NCPDT Microcontroller

ARM Cortex-M4F processor core

120-MHz operation; 150 DMIPS performance

1024 KB Flash memory

System SRAM 256 KB single-cycle System SRAM

EEPROM 6KB of EEPROM

Internal ROM Internal ROM loaded with TivaWare™ for C Series software

System Control and Clocks (see page 220)

– 16-MHz Precision Oscillator (PIOSC)

– Main Oscillator (MOSC): A frequency-accurate clock source by one of two means: an external

single-ended clock source is connected to the OSC0 input pin, or an external crystal is

connected across the OSC0 input and OSC1 output pins.

Subtopic 2

Ethernet

GitHub相关知识记录

General Question Summary

芯片I/O输入端上拉和下拉电阻的作用

数字电路有三种状态：高电平、低电平和高阻状态。但有些场合却不希望出现高阻状态，通过上拉电阻或者下拉电阻就可以使电路处于稳定的状态，

51 AVR PIC ARM

Big/Little Endian

Non-volatile and Volatile memory

Non-volatile 非易挥发性 memory

FLASH EEPROM

a type of computer memory that can retrieve stored information even after having been power cycled (turned off and back on)

Volatile

which needs constant power in order to prevent data from being erased.

SRAM

SRAM EEPROM FLASH ROM

Program memory --- Non-Volatile

ROM (Read only memory)

Once time space, after first time being programmed, cannot be changed

Nand Flash

Reading and writing are both preformed by blocks, not by byte

Erase also by block

Non Flash-- inside microcontroller

read and write by byte

Erase by block

Data Memory

EEPROM --- Non-Volatile

Electrically Erase and Programmable ROM

Only Can be read or written by byte, means can read 1 byte

Erase

can be erase around 100k -- 500k times

SRAM -- Static RAM -- Volatile

Read and Write faster

After power of , the data will lose