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The implement of synchronization and differential demodulation algorithm of GMSK signal

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***Abstract*—GMSK has the advantages of constant envelope, continuous phase, and concentrated power spectral density, and is widely used in the field of digital communication with limited frequency bands. Aiming at the multi-channel receiver system with limited hardware resources, an algorithm for obtaining bit synchronization information based on the phase characteristics and waveform characteristics of the GMSK signal is proposed, which has a simple structure, occupies less hardware resources, has a low sampling rate, and is easy to implement by engineering. And combined with the 2-bit of 10Mpbs, the bit synchronization algorithm can accurately output bit synchronization information at only 5 times the sampling rate, and the demodulation algorithm has only 0.6dB of demodulation loss compared with the theoretical value, which has excellent demodulation performance.**

Keywords-GMSK; 2-bitdifferential demodulation; symbol synchronization; FPGA

I. INTRODUCTION

GMSK signals are widely used in mobile communication and telemetry communication because of their advantages of concentrated power spectral density and good constant envelope characteristics [1]. GMSK demodulation technology is mainly divided into coherent demodulation and incoherent demodulation, coherent demodulation wants to obtain excellent decoding performance is mainly achieved through digital ring + Viterbi and other high-complexity algorithms [2], which needs to occupy a lot of FPGA hardware resources, and is not suitable for FPGA hardware resources limited and need multi-channel receivers and other equipment to receive demodulation data. Therefore, in the face of the demand that the telemetry system needs to receive demodulation data in multiple channels, it is urgent to design a demodulation scheme with less hardware resources and good bit error performance.

Literature [3-5] points out that in the incoherent demodulation method, under the same signal-to-noise ratio, the performance of 2-bit differential decomposition demodulation is better than that of 1-bit difference demodulation, and the complexity of the algorithm is lower than that of coherent demodulation, less resource occupation, and easy to implement. Literature [6] proposes a differential phase demodulation method based on Viterbi, and the simulation results show that the demodulation performance of the method is better than that of 1-bit and 2-bit differential demodulation, but the algorithm is complex, requires a large number of multipliers, and occupies more hardware resources. Literature [7] proposes a simple bit-synchronous open-loop algorithm based on GMSK signals, but it requires a sampling rate of 16 times or more to meet the system performance requirements. Literature [8] proposes a bit-synchronous signal that can be extracted directly from the GMSK signal, which is less complex, but still only suitable for high-power sampling systems. Literature [9] Gardner algorithm is used to synchronize the bit of GMSK signals to achieve the synchronization of high-speed signals with low sampling rate, but the algorithm adjusts the position parameters through the timing loop to find the best interpolation position to complete the bit synchronization, but the method occupies more hardware resources and is not suitable for engineering application environments with limited hardware resources. Through the above analysis, it can be seen that the differential decomposition adjustment algorithm requires less hardware resources; Most bit synchronization algorithms improve the accuracy of bit synchronization by increasing the hardware resources or oversampling, thereby improving the decoding performance of the system.

Based on the above situation, this paper proposes a new bit synchronization algorithm and combines the 2-bit differential demodulation algorithm to realize the incoherent demodulation of GMSK. The bit synchronization algorithm can directly use the phase characteristics and waveform characteristics of the GMSK signal to extract the bit synchronization signal, and the bit synchronization can be well completed through the low sampling rate, and the algorithm is simple and easy to implement. The whole demodulation module has the advantages of less hardware resource occupation and good bit error performance. Finally, by simulating and measuring the demodulation module, the test results of the GMSK signal at 10Mpbs code rate are given.

II. GMSK SIGNAL CHARACTERISTIC ANALYSIS

The modulated GMSK signal can be expressed as [10]:

$$s(t,\boldsymbol{a}) = \sqrt{\frac{2E_a}{T}}\cos\left[2\pi f_c t + \varphi(t,\boldsymbol{a}) + \varphi_0\right] \tag{1}$$

Where E_a is the code element energy, T is the code element period, f_c is the carrier frequency, φ_0 is the initial phase, and $\varphi(t,\boldsymbol{a})$ is the phase information, expressed as follows:

$$\varphi(t,\boldsymbol{a}) = \pi\sum_{i}^{n} a_i q\left(t - iT\right), \mathrm{t} \in \left[nT,(n+1)T\right] \tag{2}$$

where a_n is the sequence of code elements of $+1$ or -1; $q(t)$ is a pulse phase function, the $g(t)$ as an integral of the shock response of a pre modulated Gaussian filter:

$$q(t)=\int_0^t g(t)\mathrm{d}\tau \tag{3}$$

$$g(t)=\frac{1}{2T}\left\{Q\left[\frac{2\pi B}{\sqrt{\ln 2}}(t-\frac{T}{2})\right]-Q\left[\frac{2\pi B}{\sqrt{\ln 2}}(t+\frac{T}{2})\right]\right\} \tag{4}$$

$$Q(t)=\frac{1}{\sqrt{2\pi}}\int_t^{\infty} e^{-\frac{\tau^2}{2}}\mathrm{d}\tau \tag{5}$$

In Equation (4), B is the 3dB bandwidth of the Gaussian filter, and since the t value range of $(-\infty,+\infty)$, which is physically unachievable, it needs to be truncated and approximated in engineering as follows:

$$g_T(t)=\begin{cases} g(t) & t\in[-NT,NT] \\ 0 & other \end{cases} \tag{6}$$

Literature [11] shows through simulation analysis that the power spectral density of GMSK signals is mainly distributed in the range of (-2.5 T ~2.5 T), so the $g(t)$ will intercept the length of 5 T , at this time $N=2$.

Literature [12] points out that the smaller the BT value, the more compact the output power spectrum, but the more severe the inter symbol interference. The power spectral density distribution of the GMSK signal at different BT values, and when BT=0.5, 99.9% of the energy of the GMSK signal is concentrated at 1.33 R_b . By performing MATLAB simulation on the demodulation module designed in this paper at different BT values, the demodulation performance is shown in Table 1, and the bit error rate of the demodulation module is selected as the theoretical bit error rate when the BT value is 0.5.

TABLE I. DEMODULATION PERFORMANCE OF GMSK SIGNAL WITH DIFFERENT BT VALUES

BT	E_b / N_0 at error rate of 9.5×10^{-5}
0.35	14.7dB
0.40	14.2 dB
0.45	13.9 dB
0.50	13.2dB

III. DIFFERENTIAL DECOMPOSITION MODULATION MODULE DESIGN

A. A new bit synchronization algorithm

Obtaining accurate bit-synchronization information before demodulation is the key to achieving ideal demodulation performance for differential demodulation algorithms. The GMSK signal is obtained by the Gaussian filter modulated by the MSK signal, so its phase path becomes smoother than the MSK signal, and the modulation information is included in the $\varphi(t,\boldsymbol{a})$. The phase trajectory plots of the GMSK and MSK signals are shown in Figure 1, from which it can be seen that in each code period, $\varphi(t,\boldsymbol{a})$ is a monotonic function, and the code period changes monotonically in the $[n\pi/2,(n+1)\pi/2]$ interval, where n is an integer.

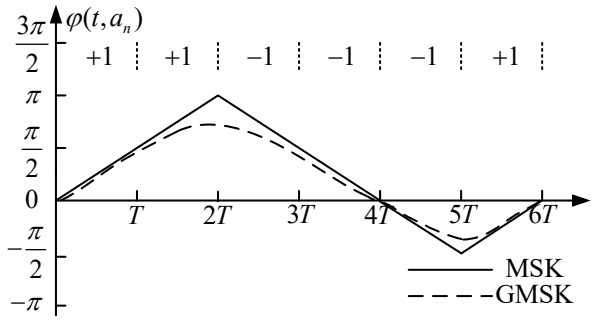

Figure 1. The phase trajectory diagram of GMSK signal

After the modulated GMSK signal is processed by digital down conversion at the receiving end, the carrier phase is restored by the universal digital loop to obtain two baseband signals I and Q:

$$\begin{cases} I(t)=\cos(\varphi(t,\boldsymbol{a})) \\ \mathrm{Q}(t)=\sin(\varphi(t,\boldsymbol{a})) \end{cases} \tag{7}$$

As can be seen from Figure 2, the sine and cosine functions are also monotonic functions in the interval $[n\pi/2,(n+1)\pi/2]$, so it can be deduced that the $I(t)$ and $Q(t)$ two data channels are monotonicity during the code period.

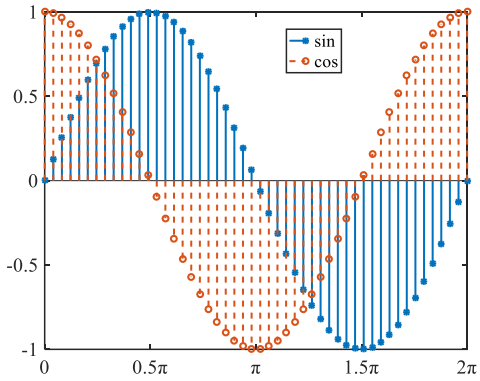

Figure 2. Waveform plot of sin and cos functions

By analyzing the phase characteristics and baseband data waveform characteristics of GMSK signals, and using their monotonicity waveform characteristics in each code cycle, this paper proposes a new bit synchronization algorithm, and the algorithm implementation steps are as follows:

(1) First, pre-sample the baseband data of $I(kT_s)$ and $Q(kT_s)$, T_s is the sampling period, k is the number of sampling points for each code element. The sampled data is judged, and the judgment includes: whether $I(kT_s)$ is an extreme point or a zero crossing point, $Q(kT_s)$ is an extreme point or a zero

crossing point. When the waveform data information meets the following conditions, it is determined to be an extreme point (represented by point P) or a zero crossing point (represented by point Z):

$$\mathrm{P}:\begin{cases}|I((k+1)T_s)|<=|I(kT_s)|>=|I((k-1)T_s)|\\ |Q((k+1)T_s)|<=|Q(kT_s)|>=|Q((k-1)T_s)|\end{cases}$$

$$Z:\begin{cases}I((k-1)T_s)\times I((k+1)T_s)<0\\ Q((k-1)T_s)\times Q((k+1)T_s)<0\end{cases}$$

(2) When the condition of is met for step 1, the sampling point can be used as code element synchronization information. The K sampling points of each code element correspond to K counters, and when the sampling points meet the judgment conditions, the corresponding counters are incremented by 1.

(3) In order to remove the interference of pseudo-extreme points and pseudo-zero crossing points and enhance the anti-interference of the algorithm, it is necessary to design a counter to set the pre sampling time, the longer the pre sampling time, the higher the accuracy of the bit synchronization algorithm. When the pre sampling time is over, the count values of K counters are compared, and the counter with the largest count value corresponds to the first sampling point of the code element, and the bit synchronization pulse is output at this sampling time. The flow of the bit synchronization algorithm is shown in Figure 3.

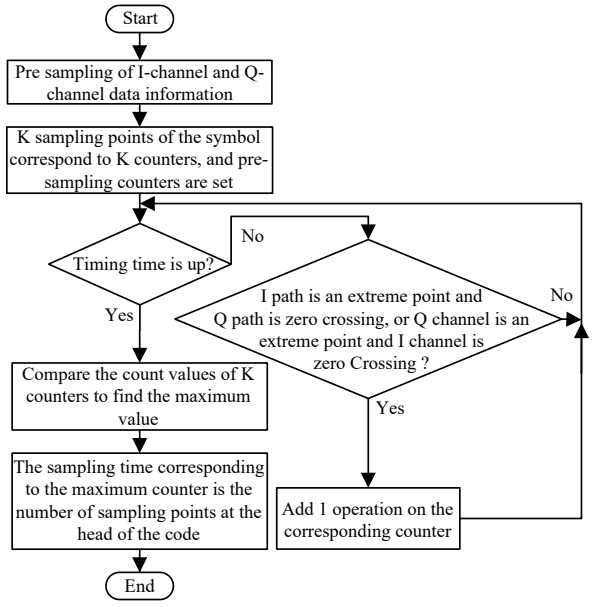

Figure 3. The flowchart of bit synchronization algorithm

Through the analysis that the bit synchronization algorithm proposed in this paper has the advantages of low algorithm complexity and less hardware resource occupation. As can be seen from Figure 1, the MSK signal has the same phase characteristics and waveform characteristics as the GMSK signal, so the bit synchronization algorithm is also suitable for bit synchronization of MSK signals.

B. Design of 2-bit differential decomposition modulation algorithm

The demodulation algorithm used in this paper is 2-bit difference demodulation, and the algorithm implementation process is shown in Figure 4.

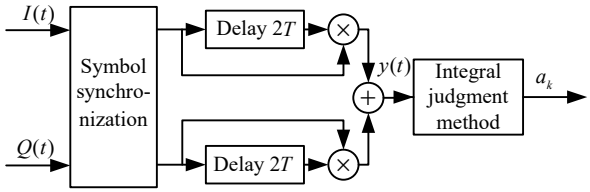

Figure 4. Implement process 2-bit of differential demodulation

As can be seen from Figure 4, the bit-synchronization module can accurately provide the demodulation module with a signal that delays by 2 cycles. The two channels I and Q are multiplied and added with the delay 2 code element periodic signals, respectively, and the output signal obtained is

$$y(t)=\cos\left[\Delta\varphi(2T)\right]+\sin\left[\Delta\varphi(2T)\right] \tag{8}$$

In the formula:

$$\begin{aligned}\Delta\varphi(2T)&=\varphi(t)-\varphi(t-2T)=\varphi(t)-\varphi(t-T)\\&+\varphi(t-T)-\varphi(t-2T)\end{aligned} \tag{9}$$

From equations (8) and (9) we get:

$$\begin{aligned}y(t)&=\cos\left[\varphi(t)-\varphi(t-T)\right]\cos\left[\Delta\varphi(\Delta T)\right]\\&-\sin\left[\varphi(t)-\varphi(t-T)\right]\sin\left[\Delta\varphi(\Delta T)\right]\end{aligned} \tag{10}$$

where $\Delta\varphi(\Delta T)=\left[\varphi(t-T)-\varphi(t-2T)\right]$. By analyzing the first term of the above equation, it can be seen that it is an even function, and the first term is always positive as long as the range of $\Delta\varphi(T)$ changes is within $\pm\pi/2$. It can be seen from the GMSK phase characteristics that the value is less than $\pi/2$, and the sampling value is positive at the kT moment, which is not decisive for the decision, and in order to eliminate its influence on the decision, it can be equivalent to a dc component V. In order to make the decision easier, it is necessary to differentially encode the input data $\{a_k\}$ at the sender, and convert the absolute code $\{a_k\}$ into a relative code $\{b_k\}$, according to the differential coding rule $b_k=a_k\otimes b_{k-1}$.

By analyzing the second term of the above equation, it can be found that if the two adjacent code elements have the same symbol, the value of $\sin\left[\varphi(t)-\varphi(t-T)\right]$ and $\sin\left[\varphi(t-T)-\varphi(t-2T)\right]$ at adjacent sampling time have the same sign, and the sign value of the second term is positive; If two adjacent code elements have different symbols, the sign value of the second term is negative. Therefore, b_k and b_{k-1} can be expressed as follows:

$$\begin{cases}b_k=\mathrm{sgn}\left\{\sin\left[\varphi(kT)-\varphi((k-1)T)\right]\right\}\\ b_{k-1}=\mathrm{sgn}\left\{\sin\left[\varphi((k-1)T)-\varphi((k-2)T)\right]\right\}\end{cases} \tag{11}$$

The Multiplication of b_k and b_{k-1} is equivalent to the modular addition of both, so the demodulated decision data $\hat{a}_k = b_k \otimes b_{k-1}$ can be deduced by the differential coding rule, and the demodulated data obtained by the decision is the data transmitted by the sender, that is $\hat{a}_k = a_k$, .

From the above analysis, it can be concluded that the 2-bit difference decomposition decision rule is expressed as follows:

$$\begin{cases} y(kT) > V & a_k = 1 \\ y(kT) < V & a_k = 0 \end{cases} \tag{12}$$

In order to further improve the accuracy of code element judgment, this paper introduces the integral decision method to process the signal after differentiation. The waveforms of K sampling points in each code element period are superimposed and then the sampling judgment is carried out.

IV. ALGORITHM DESIGN AND EXPERIMENT BASED ON FPGA

A. Algorithm design

According to the algorithm principle described in Section 2, Verilog design is carried out for the newly proposed bit synchronization algorithm and 2-bit differential decomposition debugging algorithm, and the FPGA adopts the XC7K160T chip of the K7 series produced by Xilinx. The top-level design of the GMSK demodulation module is shown in Figure 5.

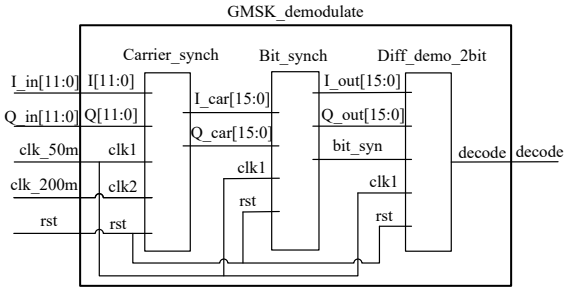

Figure 5. Top-level design of the GMSK demodulation module

It can be seen from Figure 5 that the two data channels of I and Q are first restored by the carrier synchronization module, and then processed by the synchronization module, the bit synchronization pulse corresponding to the data is output, and then the differential decomposition modulation module is demodulated based on the accurate bit synchronization signal, and finally the judgment code element information is output. Among them, the bit synchronization module does not need to use a multiplier during program implementation; The arithmetic operation of dividing by 2 is achieved by adding the shifts, avoiding the use of dividers; The differential decomposition modulation module occupies 2 multipliers and 1 adder, and all registers are designed with the smallest number of bits while ensuring the accuracy of operation, which effectively reduces the occupation of hardware resources.

The algorithm in this paper is compared with the hardware occupation using the Viterbi coherent demodulation algorithm, and the results are shown in Table 2. It can be seen from the table that compared with the latter LUT resources and DSP48E resources, the algorithm in this paper saves 92.48% and 98.46%, respectively. The entire demodulation algorithm consumes very little hardware resources, providing an engineering basis for designing multi-channel receivers (32 channel counts) with limited hardware resources.

TABLE II. COMPARISON OF HARDWARE RESOURCE USAGE

Hardware resource types	Algorithm in this article		Viterbi algorithm	
	Number	Occupancy rate	Number	Occupancy rate
LUT	1910	0.75%	25399	9.99%
I/O	28	7.00%	103	25.00%
DSP48E	5	0.32%	325	21.10%

B. Algorithm experiment

This design is tested on a software defined radio platform based on the AD9361+FPGA with an engineering test block diagram shown in Figure 6. The GMSK modulation signal is generated by RS's SMBV100A signal generator. After demodulation, the output code element is compared with the test code element using real-time processing software, and the demodulation performance is evaluated by calculating the bit error rate. The signal source output has a signal code rate of 10Mpbs, an intermediate frequency carrier of 390MHz. The test environment is shown in Figure 7.

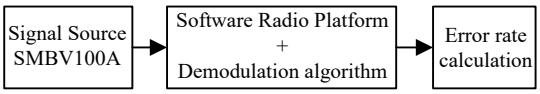

Figure 6. Block diagram of GMSK engineering test

Figure 7. AD9361+FPGA software defined radio test platform

Burn the demodulation software into the test board, and capture the key signals of the demodulation module through the online Logic analyzer to verify whether it works normally. The bit synchronization test is shown in Figure 8, when the bit_ syn_flag When the flag signal is valid, the bit_syn signal can accurately output the corrected synchronization pulse, enabling the differential demodulation module to accurately find the optimal sampling time of the symbol, thereby obtaining the best demodulation performance. As shown in Figure 9, when the signal-to-noise ratio is 15dB, the error rate of the differential demodulation module is 4.96×10^{-5} .

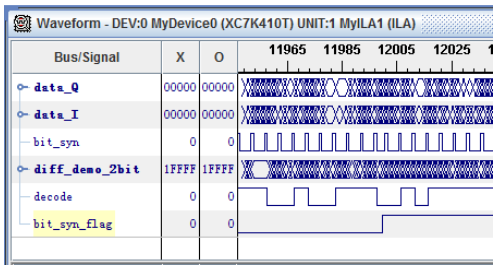

Figure 8. The bit synchronization module working result

Finally, the bit error rate test of the designed differential demodulation algorithm is carried out, and the demodulation performance is verified by comparing it with the test results of the Viterbi coherent demodulation algorithm, and the test results are shown in Figure 9. It can be seen from the figure that the engineering implementation value of the algorithm in this paper and the theoretical value of demodulation are only 0.6dB loss, indicating that the bit synchronization algorithm proposed in this paper accurately finds the best sampling moment of almost all code elements under the condition of low sampling. When the bit error rate is 9.5×10^{-5}, the demodulation performance of the proposed algorithm is only about 4.3dB lower than that of the Viterbi algorithm when the hardware resources are saved by 92%.

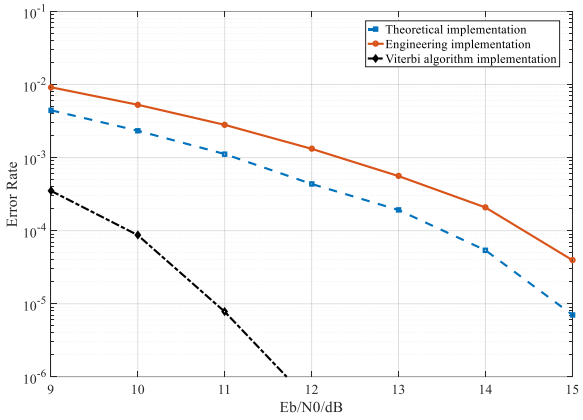

Figure 9. Demodulation algorition error rate test results

V. CONCLUSIONS

This article solves the engineering application problem that the receiver needs multi-channel GMSK demodulation and hardware resources are limited. A new bit synchronization algorithm for GMSK signals is proposed, and a demodulation system with less hardware resources and good bit error performance is designed by using the general digital ring and 2-bit difference decomposition debugging algorithm. The bit synchronization algorithm can directly obtain bit synchronization information based on the phase characteristics and waveform characteristics of the GMSK signal. Simulation and test results show that the new bit synchronization algorithm can accurately output bit synchronization information with only 5 times the sampling rate, and has the advantages of high synchronization accuracy, minimal hardware resource occupation, and easy engineering implementation. In addition, the algorithm is also suitable for bit synchronization of MSK signals. The bit error rate performance of the algorithm based on this paper is only 0.6dB lower than the theoretical value, and the demodulation performance is good. When the hardware resources are 92% less efficient than the Viter demodulation algorithm, when the bit error rate is 9.5×10^{-5}, the performance is only about 4.3dB lower than the latter, which fully meets the demodulation performance requirements of the multi-channel receiver (number of channels greater than or equal 32) of the telemetry system with limited hardware resources.

REFERENCES

[1] ZHANG J R, WU L. Interference cancellation of telemetry and ranging for GMSK+PN technique[J]. Systems Engineering and Electronics, 2018, 40(8):1708-1712.

[2] SONG D, YAO R, MA H, et al. One-Step Backtracking Algorithm Based on Viterbi Algorithm in GMSK Demodulation[C]// 2020 IEEE International Conference on Signal Processing, Communications and Computing (ICSPCC). IEEE, 2020.

[3] XONG Y S, Study on Modulation and Demodulation Technique of GMSK[D]. Chongqing University . 2007:38-40.

[4] YANG S S, SONG X G. Performance analysis and simulation of n-bit combined differential demodulation for GMSK signal[J]. Aerospace Electronic Warfare, 2016, 32(4):44-46+51.

[5] WU T F. Demodulation Algorithm Based on Two Bit Differential Detection for GMSK Signals[J]. Journal of Military Communication Technology, 2002, 23(01): 35-40.

[6] YANG Z K, Jin D L, WANG Y. Research and Simulation Implementation of GMSK Modulation and Noncoherent Demodulation Algorithm[J]. Radio Engineering, 2017, 47(12):61-66+82.

[7] ZHAO Q M, GONG J Z, CHEN Q L. Symbol Synchronization Algorithm of GMSK Modulation Based on Software Radio[J]. Video Engineering, 2013 37(09):146-148+156.

[8] DAI Y C, ZHANG M D. study of bit synchronizer for digital receiver[J].Electronic Engineering, 2016, 23(09):46-48+56.

[9] GU S M, CHEN L T, CHEN J B. Application of Gardner Synchronization Algorithm in High Speed GMSK Signal Transmission[J]. Radio Engineering, 2019, 49(06):527-533.

[10] LUI G L. Threshold detection performance of GMSK signal with BT=0.5[J]. IEEE, 2002.

[11] Chen L, Kang C,Gu S, et al. Synchronization and Coherent Demodulation Algorithm of GMSK Signal[J]. Radio Engineering, 2021, 51(05):346-351.

[12] Chen L, Kang C,Gu S, et al. Synchronization and Coherent Demodulation Algorithm of GMSK Signal[J]. Radio Engineering, 2021, 51(05):346-351.