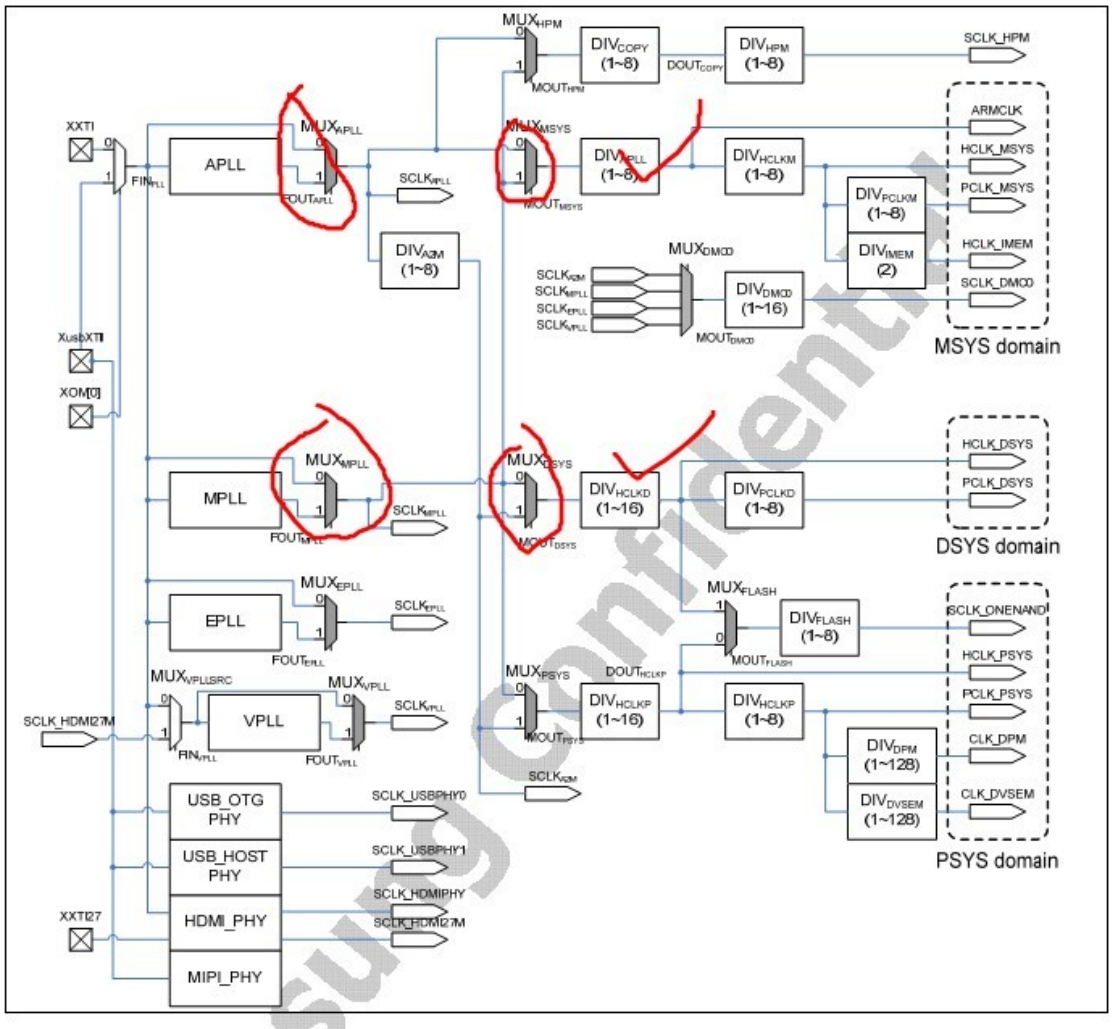
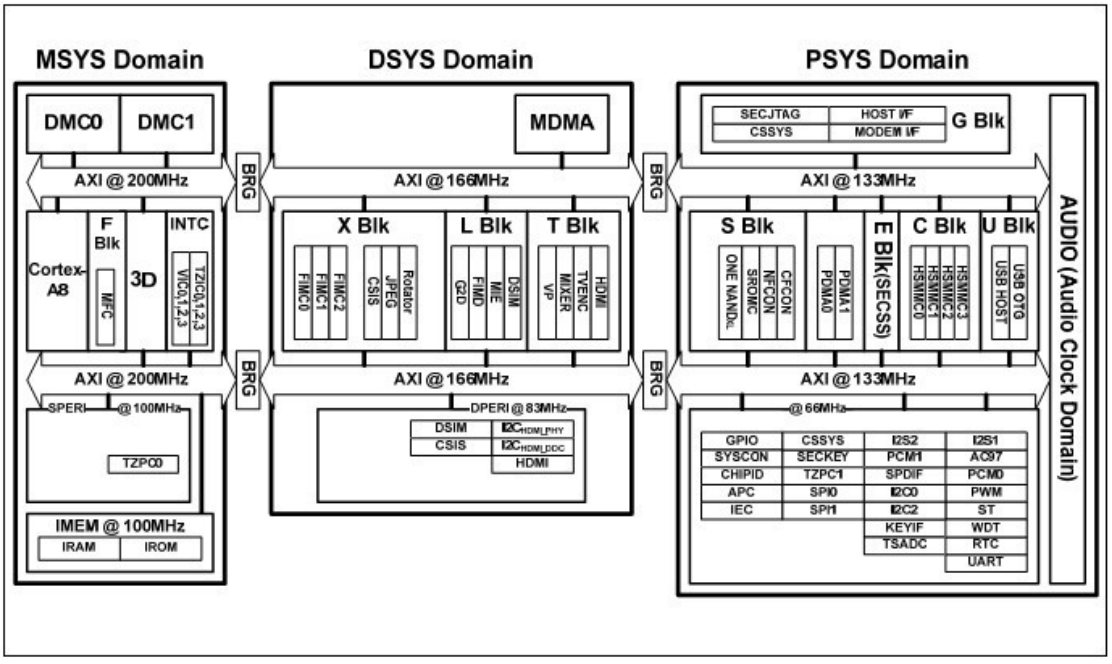
Qt210时钟学习笔记



1.首先看下图



从这幅图就可知到210的时钟分为三个域，分别为MSYS Domain, DSYS Domain , PSYS Domain.每个域一般又分几部等如下2.每个域的分频关系

- MSYS clock domain
  - freq(ARMCLK) = freq(MOUT_MSYS) / n, where n = 1 ~ 8
  - freq(HCLK_MSYS) = freq(ARMCLK) / n, where n = 1 ~ 8
  - freq(PCLK_MSYS) = freq(HCLK_MSYS) / n, where n = 1 ~ 8
  - freq(HCLK_IMEM) = freq(HCLK_MSYS) / 2

• DSYS clock domain
– freq(HCLK_DSYS) = freq(MOUT_DSYS) / n, where n = 1 ~ 16
– freq(PCLK_DSYS) = freq(HCLK_DSYS) / n, where n = 1 ~ 8

• PSYS clock domain
– freq(HCLK_PSYS) = freq(MOUT_PSYS) / n, where n = 1 ~ 16
– freq(PCLK_PSYS) = freq(HCLK_PSYS) / n, where n = 1 ~ 8
– freq(SCLK_ONENAND) = freq(HCLK_PSYS) / n, where n = 1 ~ 8

3.配置时钟我们一般要以下的频率的值配出来
• freq(ARMCLK) = 1000 MHz
• freq(HCLK_MSYS) = 200 MHz
• freq(HCLK_IMEM) = 100 MHz
• freq(PCLK_MSYS) = 100 MHz
• freq(HCLK_DSYS) = 166 MHz
• freq(PCLK_DSYS) = 83 MHz
• freq(HCLK_PSYS) = 133 MHz
• freq(PCLK_PSYS) = 66 MHz
• freq(SCLK_ONENAND) = 133 MHz, 166 MHz

4.首先我们要把每个域的最大的频率配置出来，然后根据他的分频关系在分频配置出其他值。但是每个域的最大哪个分频源头是哪个呢，那就要下面那幅图找了，

上图画出了两个域的具体路线，其中圆圈代表选择那路勾代表分频下面就举个例子是怎么配置时钟的

5.ARMCLK的实例配置

最源头是XXTI(这是硬件原理图OM0决定的)→FINpll （24M）→APLL(在这会变频)→（经过MUXapll选择是FINpll还是变频后的FOUTapll）→（MUXmsys选择）→（DIVapll分频）→ARMCLK（然后由ARMCLK分频配置MSYS domain的个频率），其他域的配置也类似这个（其中每个域的PCLK一等于HCLK除2），然后把各域的值配置成3的值就行了

6.具体寄存器配置

APLL_CON0 =(1<<0)|(0x06<<8)|(0xfa<<16)|(1<<29)|(1<<31);//这是APLL变频的
CLK_SRC0 =(1<<0)|(1<<4)|(1<<12)|(1<<8)|(0<<16)|(0<<20)|(1<<28);//这是管理MUX的
MPLL_CON =(1<<0)|(0x0c<<8)|(0x29b<<16)|(1<<29)|(1<<31);//这是MPLL变频的
CLK_DIV0 =(0<<0)|(0x4<<8)|(0x1<<12)|(0x03<<16)|(0x1<<20)|(0x04<<24)|(0x1<<28);//这是分频

7.变频参考例子

APLL的

Table 3-1 APLL PMS Value

FIN (MHz)	Target FOUT (MHz)	P	M	S	AFC_ENB	AFC	FVCO (MHz)	FOUT (MHz)
24	800	6	200	1	0	0	1600.000	800.000
24	1000	6	250	1	0	0	2000.000	1000.000

MPLL的

Table 3-2 MPLL PMS Value

FIN (MHz)	Target FOUT (MHz)	VSEL	P	M	S	FVCO (MHz)	FOUT (MHz)
24	133	0	6	266	3	1064.000	133.000
24	166	0	6	332	3	1328.000	166.000
24	266	0	6	266	2	1064.000	266.000
24	333	0	6	333	2	1332.000	333.000
24	667	0	12	667	1	1334.000	667.000

```cpp
#define APLL_CON0  (*(volatile unsigned int *)0xE0100100)
#define MPLL_CON   (*(volatile unsigned int *)0xE0100108)
#define CLK_SRC0   (*(volatile unsigned int *)0xE0100200)
#define CLK_DIV0   (*(volatile unsigned int *)0xE0100300)

void clock_init()
{
    APLL_CON0 =(1<<0)|(0x06<<8)|(0xfa<<16)|(1<<29)|(1<<31);
    CLK_SRC0  =(1<<0)|(1<<4)|(1<<12)|(1<<8)|(0<<16)|(0<<20)|(1<<28);
    MPLL_CON  =(1<<0)|(0x0c<<8)|(0x29b<<16)|(1<<29)|(1<<31);
    CLK_DIV0  =(0<<0)|(0x4<<8)|(0x1<<12)|(0x03<<16)|(0x1<<20)|(0x04<<24)|(0x1<<28);
    return ;
}
```