Research Gap

- In the conventional two transistors and one capacitor (2T1C) pixel circuit shown in the figure-1, the brightness uniformity is always deteriorated by the variations in threshold voltage and mobility of the driving TFTs as well as the current-resistance (I-R) voltage drop in the power line.

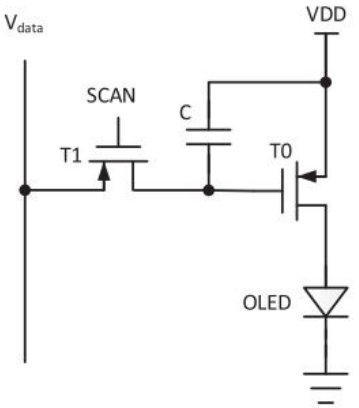


Figure 1: Conventional 2T1C Pixel Circuit

- To overcome these weaknesses, many driving methods have been investigated. According to the diversity of input signal, the driving methods could be commonly divided into voltage programming and current programming.
- For voltage programming, in order to take all of the non-idealities (i.e., threshold, mobility, parasitic resistors, etc.) into account, a number of additional TFTs and capacitors are indispensable, which would lead to low aperture ratio (AR). problem.
- Moreover, for the reason that the TFTs usually work close to sub- threshold region during compensation period, threshold voltage sampling may consume most of the row time, which limits the display resolution.
- For current programming method, although it could effectively improve the display luminance uniformity, a long programming time is required for low data current (<100nA).
- In 2007, a hybrid driving method called current-biased voltage-programmed (CBVP) pixel circuit was proposed to achieve both the accurate compensation and short settling time. However, the complexity of its 5T2C structure results in a small AR.

We are trying to reduce the number of TFTs used in pixel driving circuit as it will improve the pixel aperture ratio, power efficiency, higher refreshing rates etc.

5T-2C Pixel Circuit

- The pixel circuit consisting of one driving TFT (Q5), four switching TFTs (Q1, Q2, Q3, Q4), two storage capacitors (C1, C2), one OLED. The OLED model consists of two junction diodes (D1, D2) and one capacitor (COLED) in parallel. VSCAN is the signal for selecting data input, VDATA refers to input data voltage and VREF refers to constant DC voltage.
- The operation phase of the proposed circuit is divided into three phases:
  - VTH (threshold voltage) detection phase
  - Data input phase
  - Emission phase

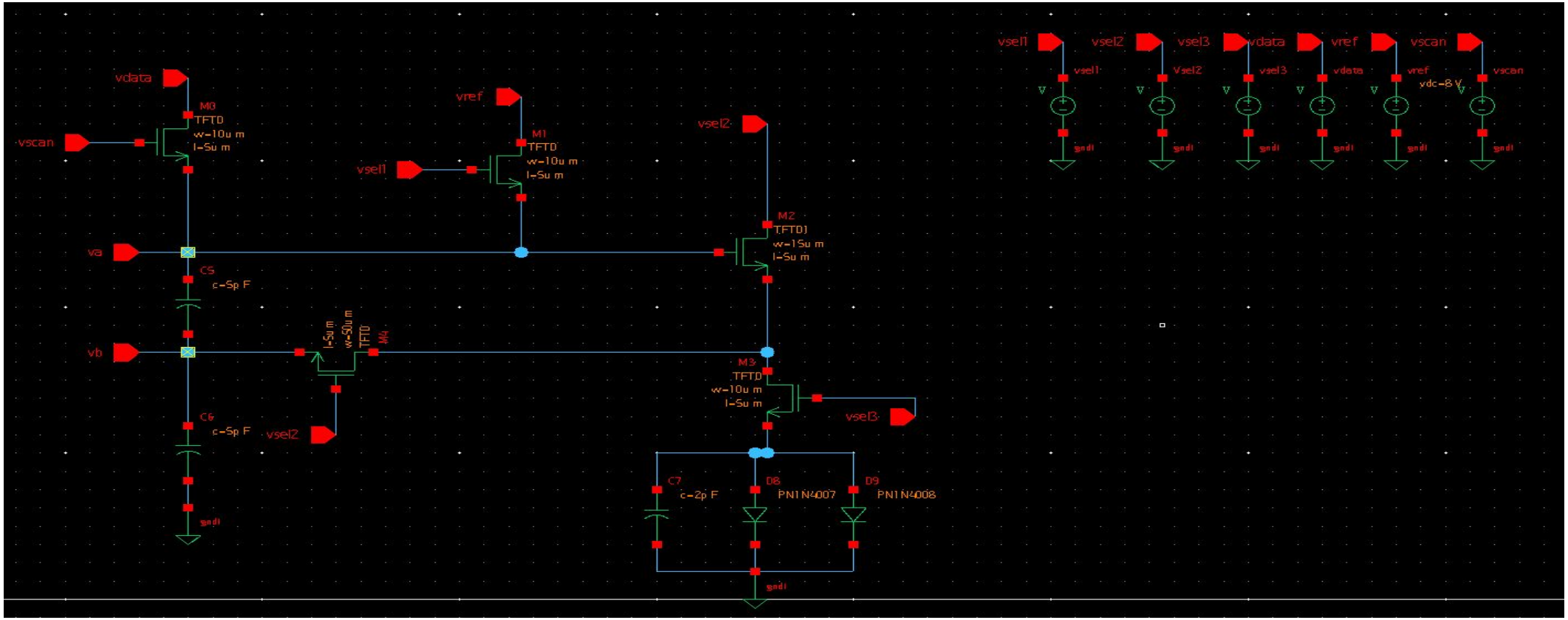
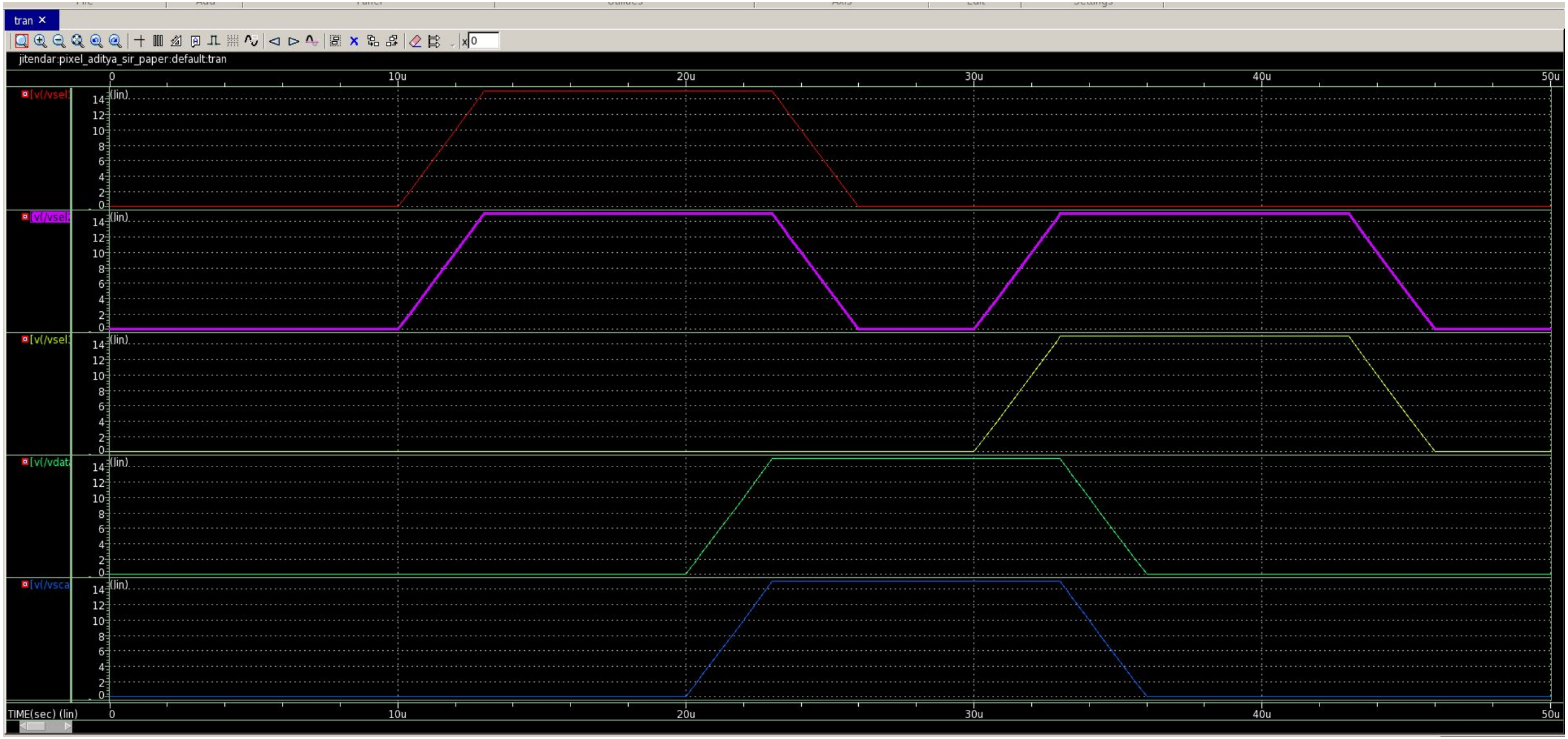


Figure 2: 5T-2C Pixel Circuit

5T-2C Pixel Circuit

Programmed Voltage input lines:



5T-2C Pixel Circuit

Threshold voltage detection phase:

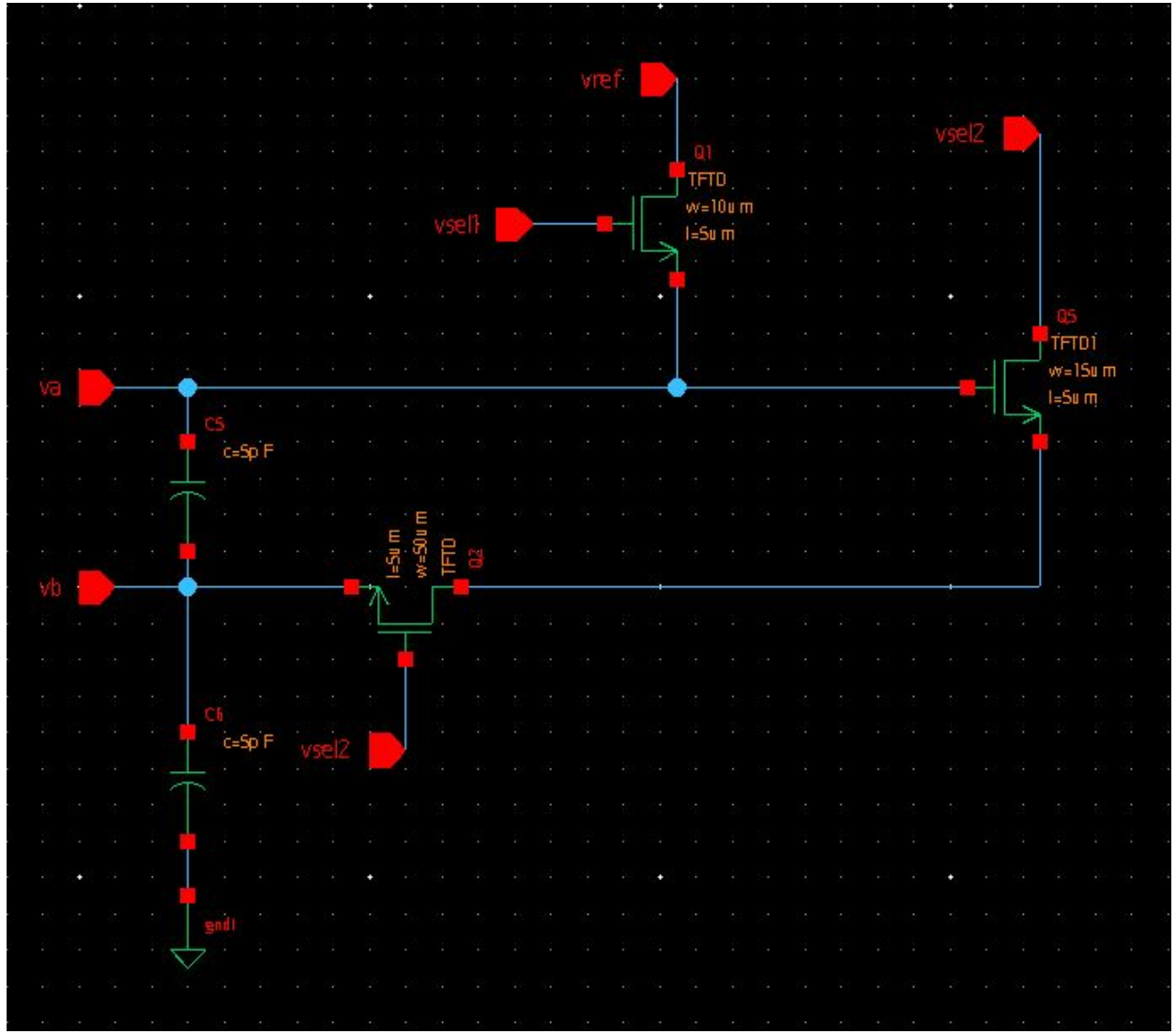


Figure 3: V_{th} detection phase for 5T-2C Pixel Circuit

- **Vsel1, Vsel2 are high => Q1, Q2 and Q5 are turned ON**
- **Vsel3, Vdata, Vscan are low =>Q3 and Q4 are turned OFF.**
- **Q5 will be ON upto**

$$Vgs_{Q5} <= Vth_{Q5} \text{ (OFF Condition)}$$

$$Va - V_c <= Vth_{Q5}$$

$$V_c <= V_{ref} - Vth_{Q5}$$

$$V_b <= V_{ref} - Vth_{Q5}$$

5T-2C Pixel Circuit

Data input phase:

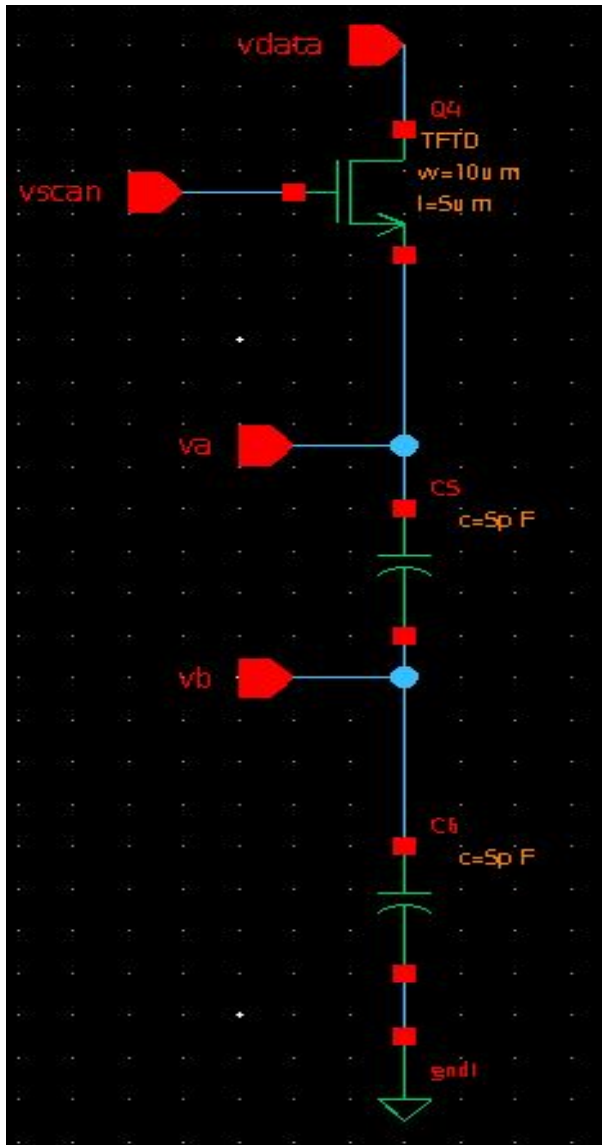


Figure 4: Data input phase for 5T-2C Pixel Circuit

- **Vsel1, Vsel2 and Vsel 3 -> Low**
- **Vscan and Vdata -> High**
- **Initially,**

$$V_a = V_{ref}$$

$$V_b = V_{ref} - Vth_{Q5}$$

- **So, now the Q4 is ON, it will change upto Vdata**

$$V_a = V_{data}$$

$$= V_b - (V_{ref} - Vth_{Q5}) + \frac{C1}{C1+C2})(V_{data} - V_{ref})$$

- **Voltage across the capacitor C1**

$$V_g = V_a - V_b$$

$$= (-V_{ref} + Vth_{M5} - \frac{C1}{C1+C2}(V_{data} - V_{ref})$$

$$= Vth_{M5} + \frac{C1}{C1+C2}(V_{data} - V_{ref})$$

5T-2C Pixel Circuit

Emission phase:

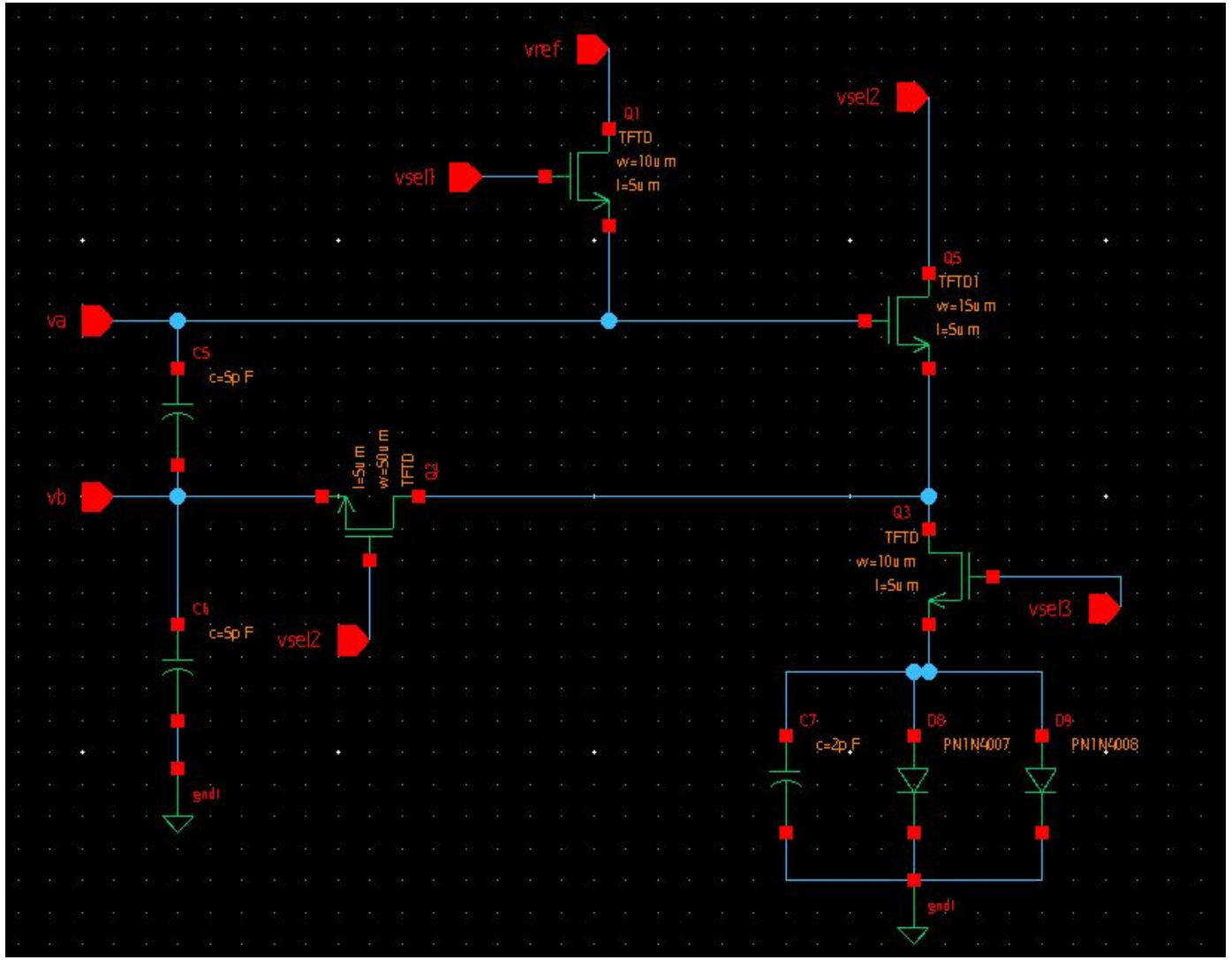


Figure 5: Emission phase for 5T-2C Pixel Circuit

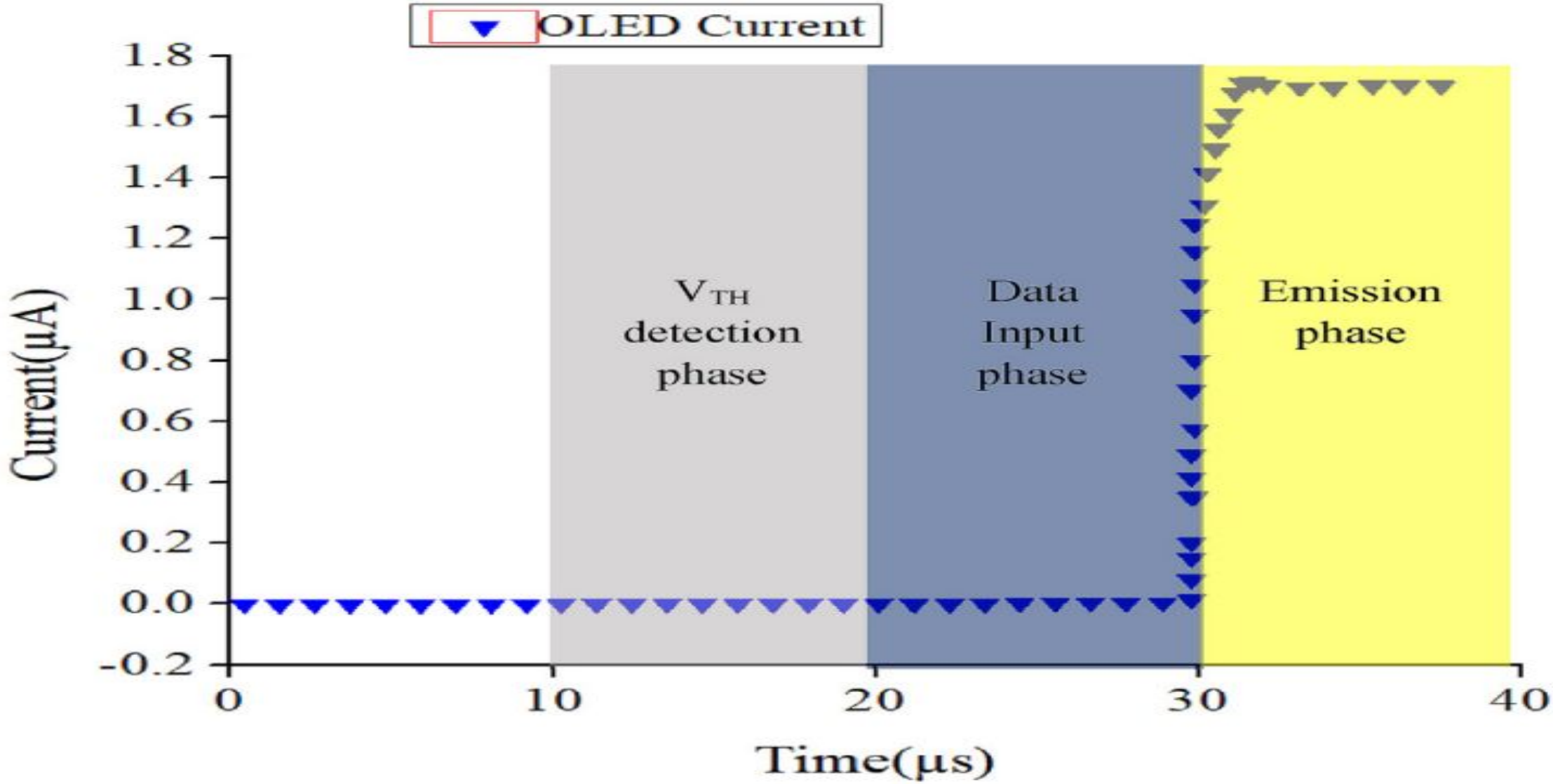
$$I = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (Vgs_{Q5} - Vth)^2$$

$$= \frac{K}{2}((V_{data} - V_{ref})(\frac{C1}{C1+C2}) + Vth_{Q5} - Vth)^2$$

$$= \frac{K}{2}((V_{data} - V_{ref})(\frac{C1}{C1+C2}))^2$$

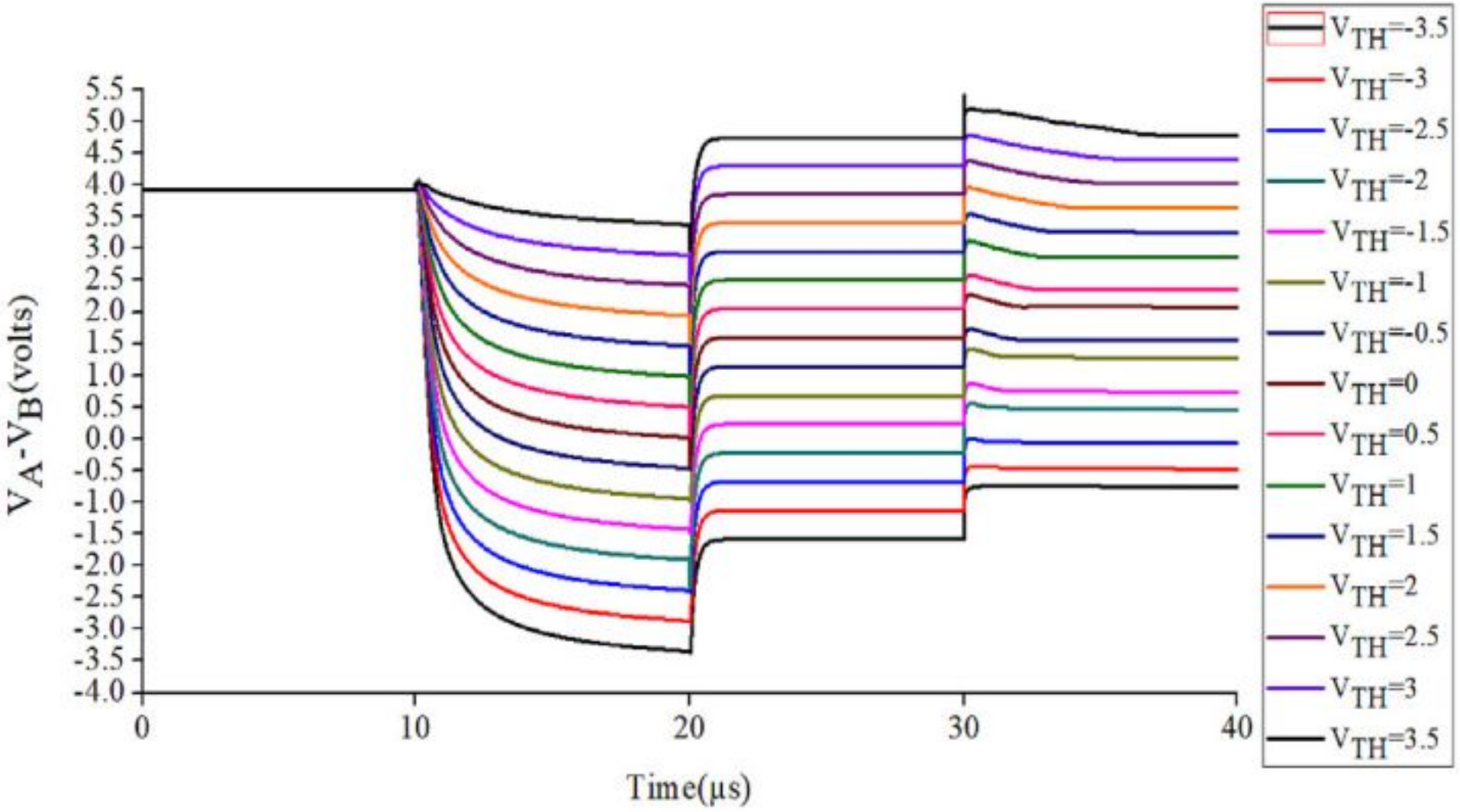
5T-2C Pixel Circuit

RESULTS:



5T-2C Pixel Circuit

RESULTS:



Proposed Pixel Circuit

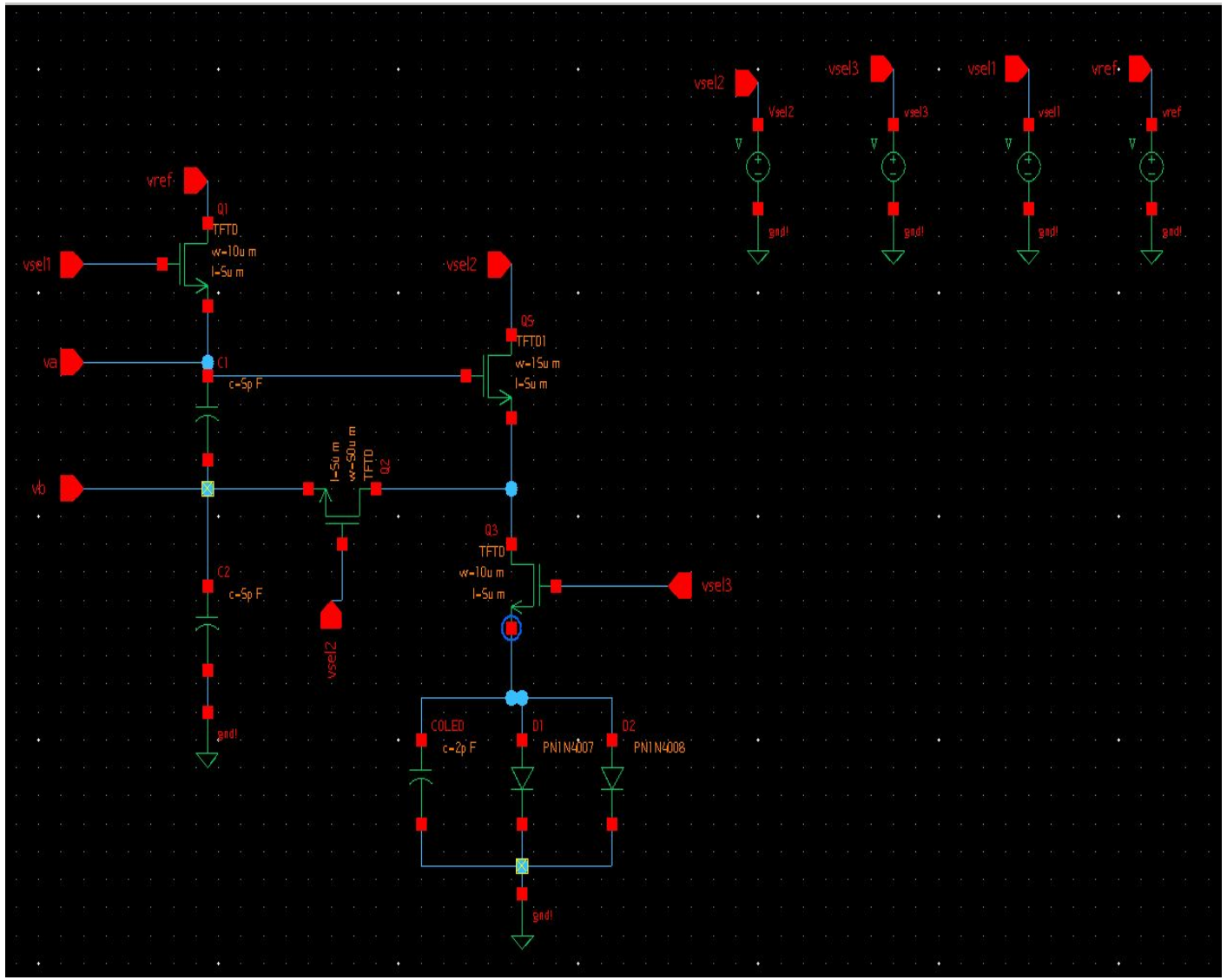


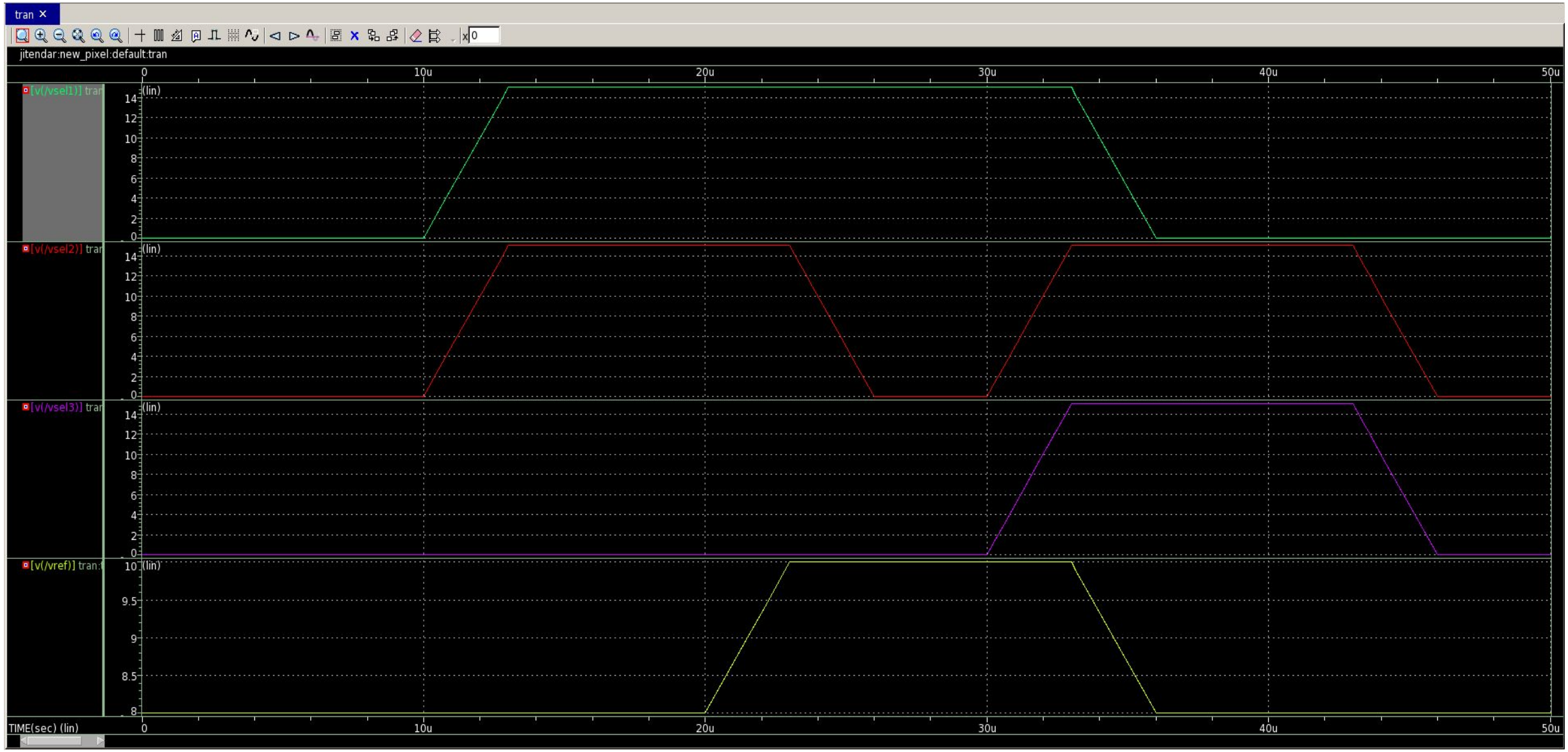
Figure 6: Proposed 4T-2C Pixel Circuit

CHANGES MADE:

- **Removed Q_4 (1 Transistor was less).**
- **Here V'_{ref} was initially v_{ref} at the time of v_{th} detection phase and v_{data} at data input phase.**
- **Here V_{ref} was DC voltage in previous circuit but it was not present in 2 and 3 stage, so we make it pulse instead of DC voltage.**

Proposed Pixel Circuit

Programmed Voltage input lines:



Proposed Pixel Circuit

Threshold voltage detection phase:

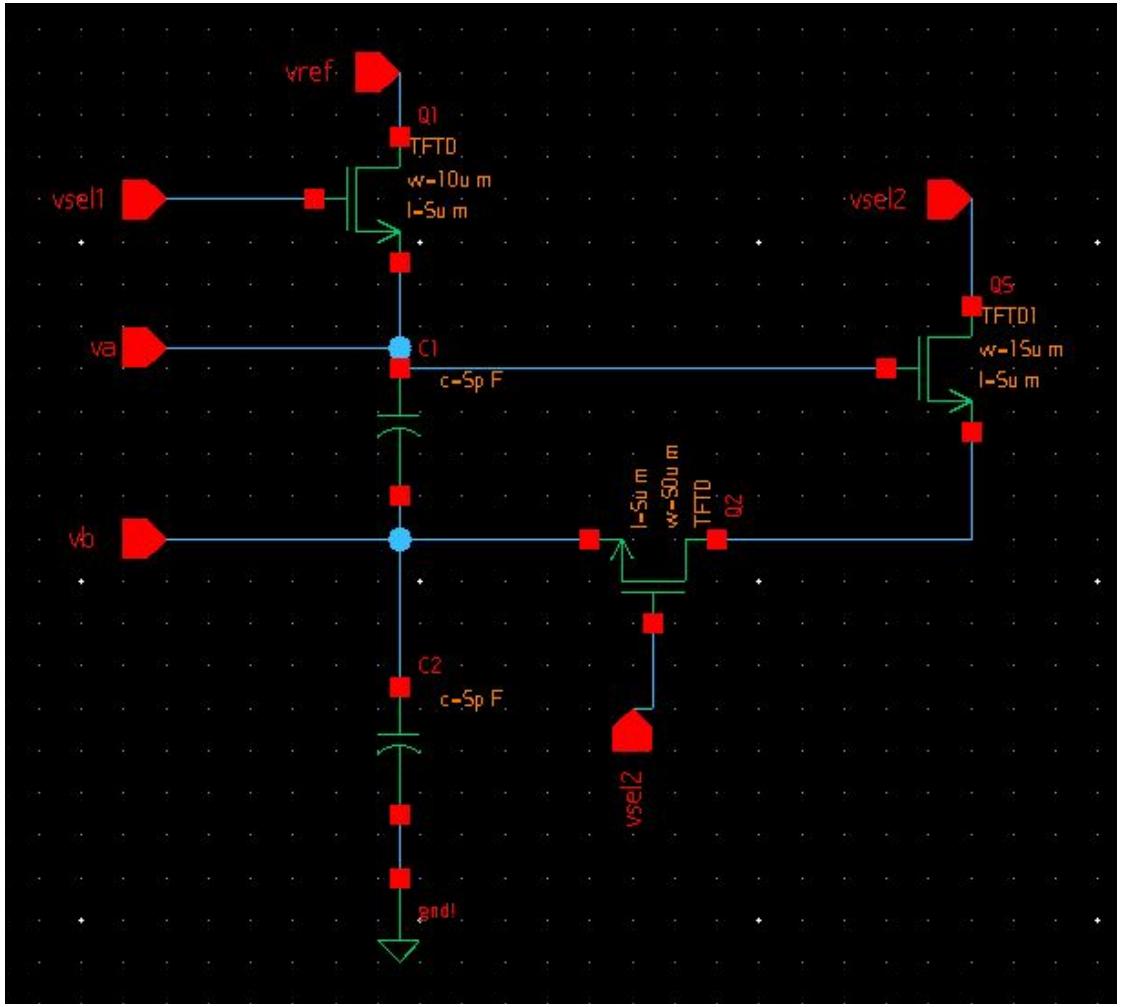


Figure 7: V_{th} detection phase for 4T-2C Pixel Circuit

- **Here Q5 will be ON upto**

$$V_a - V_b > Vth_{Q5}$$

- **Node A will be Vref**
- **Until Q5 will ON the node C will charge upto somewhat until it was OFF**

$$Vgs_{Q5} <= Vth_{Q5} \text{ (OFF Condition)}$$

$$Va - V_c <= Vth_{Q5}$$

$$V_c <= V_{ref} - Vth_{Q5}$$

$$V_b <= V_{ref} - Vth_{Q5}$$

Proposed Pixel Circuit

Data input phase:

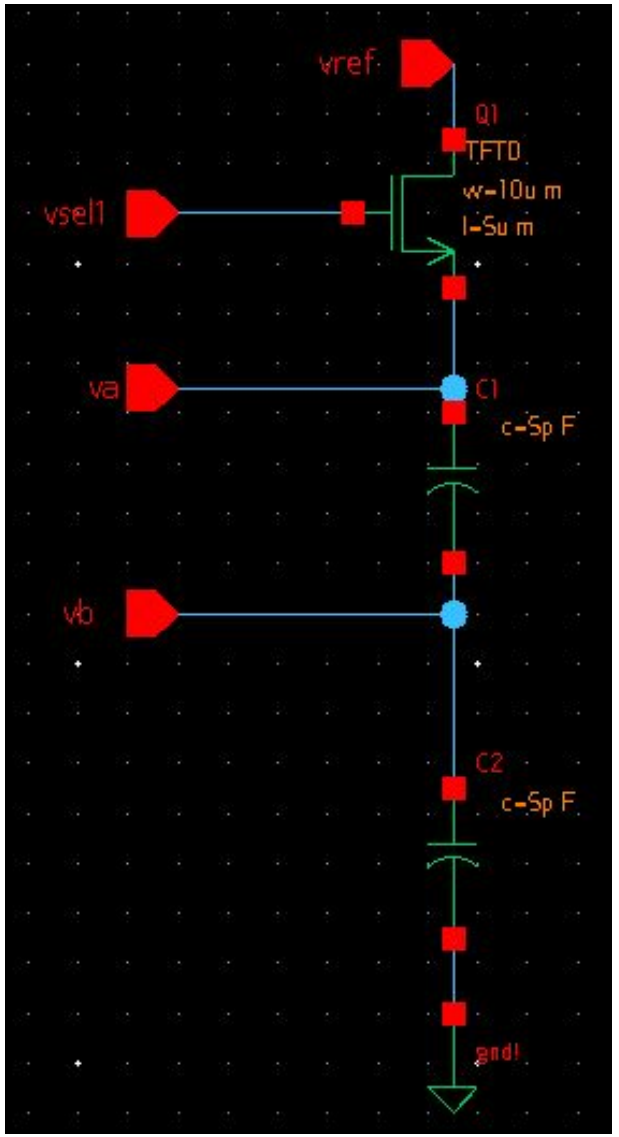


Figure 8: Data input phase for 4T-2C Pixel Circuit

- **Initial Conditions**

$$V_a = V_{ref}$$

$$V_b = V_{ref} - Vth_{Q5}$$

- **Now Q1 was still ON**
- **Node A it will charge upto Vdata**

$$V_a = V_{data}$$

$$V_b = (V_{ref} - Vth_{Q5}) + \left(\frac{C1}{C1+C2}\right)(V_{data} - V_{ref})$$

Proposed Pixel Circuit

Emission phase:

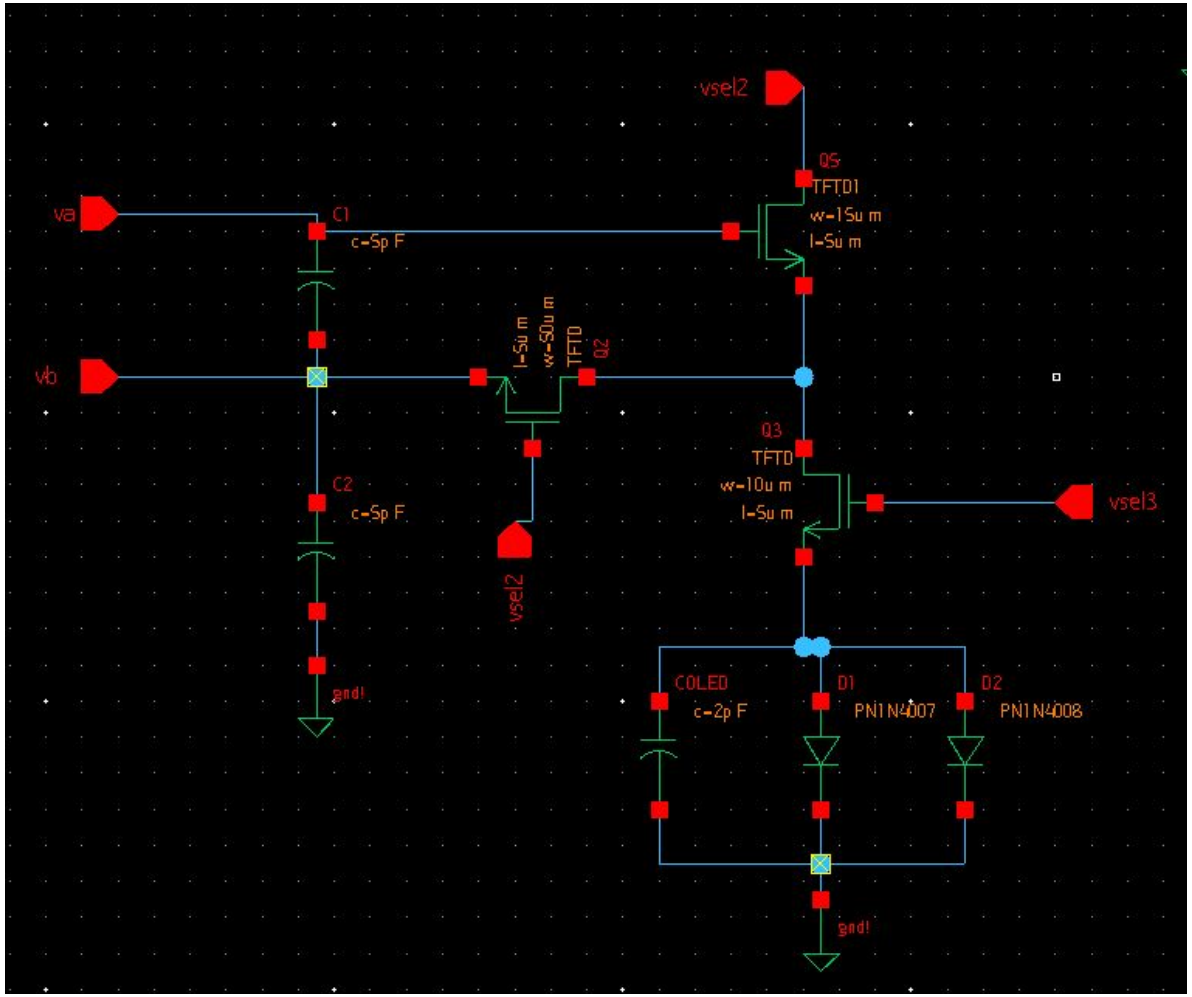


Figure 9: Emission phase for 4T-2C Pixel Circuit

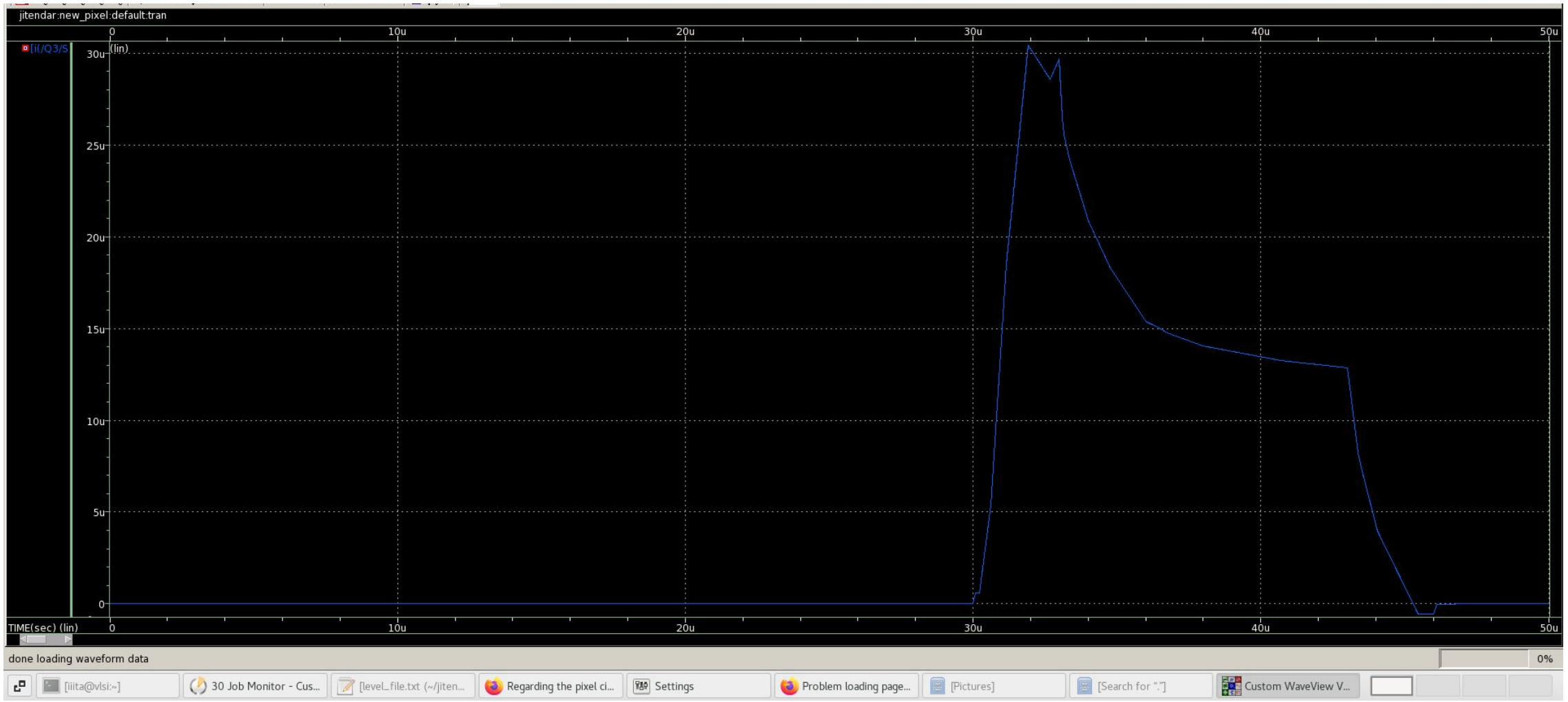
$$I = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_a - V_b - Vth_{Q5})^2$$

$$= \frac{K}{2}((V_{data} - V_{ref} + Vth_{Q5}) - (V_{data} - V_{ref})(\frac{C1}{C1+C2}) - Vth_{Q5})^2$$

$$= \frac{K}{2}((V_{data} - V_{ref})(\frac{C1}{C1+C2}))^2$$

Proposed Pixel Circuit

RESULTS:



PROPOSED PIXEL CIRCUIT

RESULTS: