MATLAB 8-Bit ADC Simulation & Characterization

ELEC 5705

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1 Objective

In this assignment, an 8-bit 10 GS/s ADC is simulated in MATLAB and then characterized via FFT analysis. The purpose is to understand the FFT analysis and how non-ideal factors (non-linearity, random noise, jitter) impact the performance of an ADC.

2 Ideal 8-Bit ADC

This section details the signal definition, sampling strategy and quantization logic used to characterize the device.

2.1 System Definition & Input Signal

The simulation characterizes a high-speed ADC with sampling rate, f_s, of 10 GS/s and a resolution, N, of 8 bits. The input signal was defined as a pure sinusoid with a peak-to-peak voltage, V_{pp}, of 2V.

To simulate the continuous nature of the analog input before sampling, the signal was defined as:

$$x[n] = A\sin(2\pi f_{in}t + \phi)$$

where amplitude A was set to 0.98 to prevent hard clipping.

2.2 Coherent Sampling

The coherent sampling strategy, as opposed to using windowing functions, was used for the FFT analysis. Coherent sampling ensures that the input signal completes an integer number of cycles exactly within the sampled data record.

The input frequency, f_{in}, was calculated based on the number of samples, M, and a chosen prime number. f_{in} is thus:

$$f_{in} = \frac{prime}{M} f_s$$

Where M is set to 8192 FFT points, the prime number is chosen to be 211 corresponding to an input sinusoid signal that is ≈ 257 MHz.

A prime number ensures that the sampling phases are mutually prime to the input frequency, preventing quantization errors from repeating periodically and ensuring a white spectrum for the quantization noise.

This ensures that the fundamental signal energy is exactly in a single FFT bin, eliminating spectral leakage.

2.3 Ideal Quantization Process

The quantization process, continuous voltage signal into discrete digital codes, was implemented as a uniform staircase function.

The step size, which is the LSB, was calculated as follows:

$$\Delta_{LSB} = \frac{V_{pp}}{2^N}$$

This is the same as the smallest detectable voltage change.

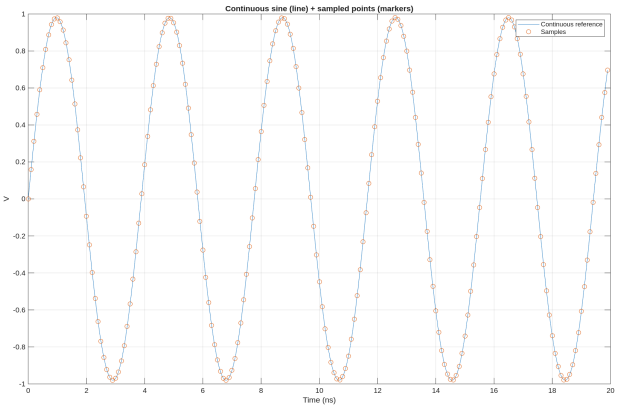
The continuous samples were then mapped to integer codes using the floor function:

$$Code = floor(\frac{x[n]+\frac{V_{pp}}{2}}{\Delta_{LSB}})$$

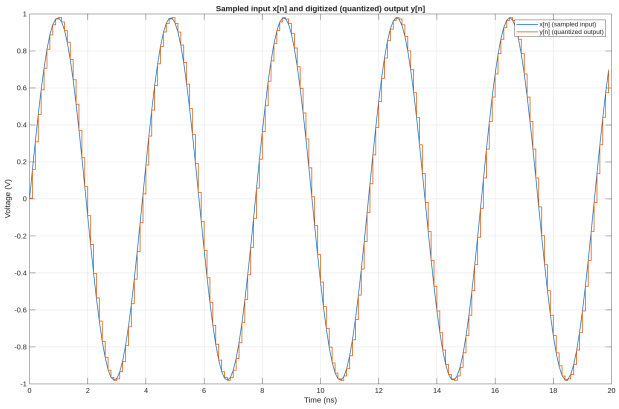
The should replicate the truncation in a flash ADC and this quantization also therefore introduces the error signal, ϵ, forming the theoretical noise floor.

The input signal overlaid with the samples and quantized output along with the digitized ADC output codes can be seen in Figure 1.

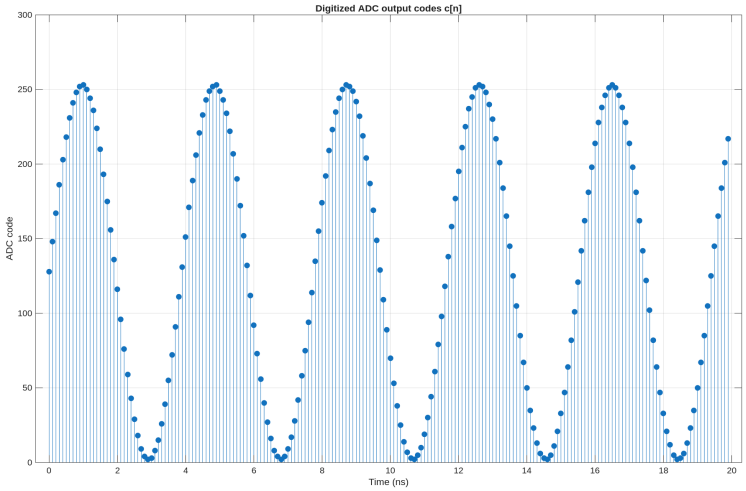
Fig. 1a shows the continuous-time sinusoid together with the discrete-time samples taken at f_s, illustrating the sampling operation. Fig. 1b overlays the sampled values with the quantized (staircase) output, highlighting how an 8-bit uniform quantizer maps each sample to the nearest discrete level and introduces quantization error. Finally, Fig. 1c presents the corresponding integer output codes $c[n]$, showing the same waveform represented purely in the ADC's digital output domain.



(a) Continuous reference sine with sampled points.



(b) Sampled input $x[n]$ and quantized output $y[n]$.



(c) Digitized ADC output codes $c[n]$.

Figure 1: ADC sampling and quantization process.

2.4 Ideal FFT Analysis & Metrics

Once the time-domain data was quantized, MATLAB's FFT function was used to transform it to the frequency domain.

2.4.1 SINAD

SINAD is the primary metric for the overall dynamic performance of the ADC. It is defined as as the ratio of the RMS signal amplitude to the mean value of the root-sum-square of all other spectral components excluding DC.

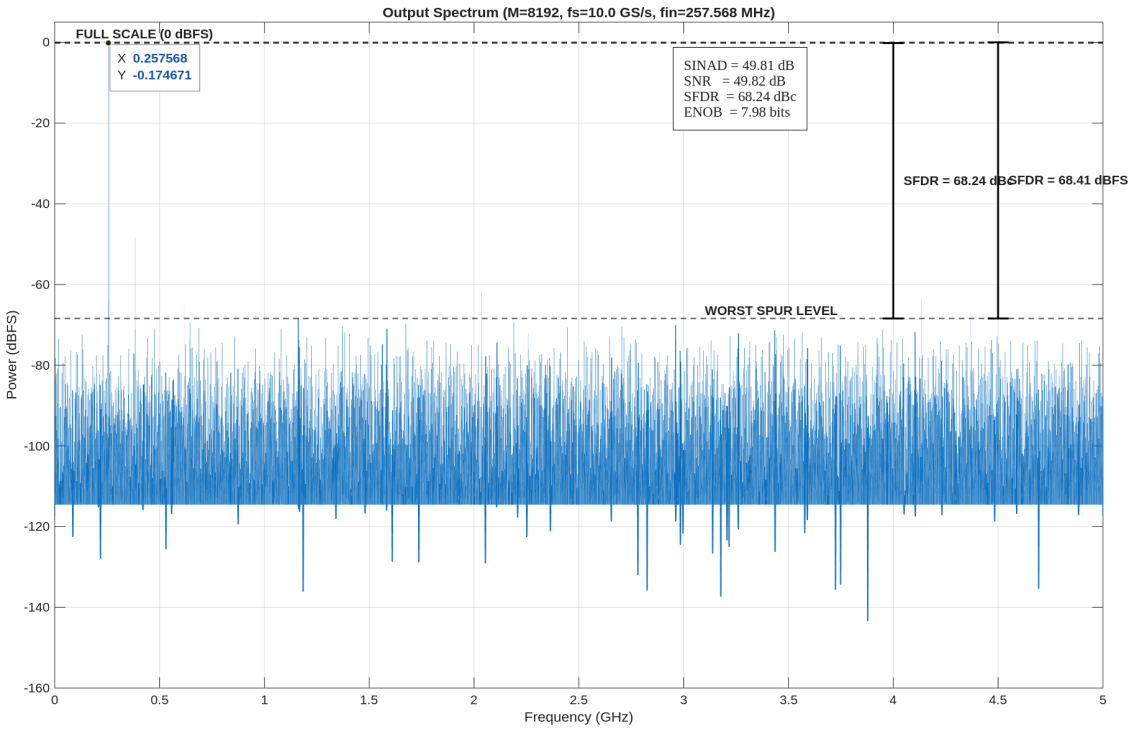


Figure 2: Ideal FFT & Performance Metrics for Ideal 8-bit ADC

SINAD can be expressed as:

$$SINAD = 20\log(\frac{S}{N+D})$$

In the simulation, SINAD was calculated by summing the power of all frequency bins in the Nyquist zone (DC to $\frac{f_s}{2}$), excluding the fundamental signal bin and DC bin.

For an ideal 8-bit ADC, SINAD should be equal to the ideal SNR case (which will be discussed next) which is 49.92 dB.

2.4.2 SNR

While SINAD includes all spectral impurities, SNR isolates the random noise floor from harmonic distortion; signal harmonics are explicitly excluded:

$$SNR = 20\log(\frac{S}{N})$$

In my implementation, the first 5 harmonics are masked out of the noise calculation and for an ideal ADC the theoretial SNR is given by:

$$SNR = 6.02N + 1.76 \text{ dB}$$
$$= 6.02(8) + 1.76$$
$$= 49.92 \text{ dB}$$

2.4.3 SFDR

SFDR is the ratio of the RMS value of the carrier frequency to the RMS value of the next largest noise or distortion component or rather largest spur.

In the simulation, this was found by identifying the maximum power peak in the spectrum outside of the fundamental signal bin.

2.4.4 ENOB

ENOB expresses the performance of the ADC in terms of bits rather than dB. ENOB is derived as such:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

ENOB for an 8-bit ideal ADC should therefore be nearly exactly 8 bits.

2.4.5 Ideal Results

Figure 2 presents the output spectrum of the simulated ideal 8-bit DC. The input signal is a 257 MHz tone sampled at 10 GS/s.

The simulation yielded the following performance metrics:

- **SINAD:** 49.81 dB
- **SNR:** 49.82 dB
- **SFDR:** 68.24 dBc
- **ENOB:** 7.98 bits

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These results align closely with the theoretical limits of an ideal 8-bit quantizer.

- **SINAD & SNR:** The simulated values of 49.81 dB and 49.82 dB are within 0.1 dB of the theoretical maximum, confirming the accuracy of the quantization model and the coherent sampling setup. The near-identical values for SINAD and SNR indicate that harmonic distortion is negligible. This is expected for an ideal quantizer, where the error is dominated by broad-spectrum quantization noise rather than specific non-linearities.

- **ENOB:** The effective number of bits (7.98) is virtually identical to the physical resolution (8 bits), demonstrating that quantization noise is the sole limiting factor in this ideal scenario.

- **SFDR:** The spurious-free dynamic range is 68.24 dBc. Since there are no non-linearities in the ideal model to generate harmonic spurs, the "spur" identified by the SFDR metric is simply the highest peak within the random quantization noise floor. The noise floor itself is pushed down by the FFT process gain ($10\log_{10}(M/2) \approx 36$ dB) placing the visual floor near -86 dBFS relative to the quantization noise level, consistent with the plot.

This has established a verified baseline for the subsequent sections, where non-ideal behaviors will be introduced.

3 Front-End Non-Linearity

To characterize the impact of analog imperfections, non-linearity was introduced to the ADC. In the real world, components such as buffers and amplifiers introduce harmonic distortion. As such, the simulated non-linearity should have the effect of increasing the harmonic distortions.

To simulate this, a cubic nonlinearity term was added to the ideal input signal $x[n]$ before quantization is done. The distorted signal signal x_{nl} is therefore defined as:

$$x_{nl} = x[n] + a_3 x[n]^3$$

where a_3 is the third-order non-linearity coefficient. This term compresses or expands the signal peaks, generating odd-order harmonics (3rd, 5th,...) in the frequency spectrum. The even-order coefficient (a_2) was omitted for this simulation in order to focus on symmetrical distortion typical of differential circuits.

3.1 Maximum Tolerable Non-Linearity

The objective was to identify the maximum non-linearity coefficient a_3 that the system could tolerate before the ENOB is degraded by more than 1.5 bits from the ideal baseline (7.98).

To determine this specific value, a binary search was implemented.

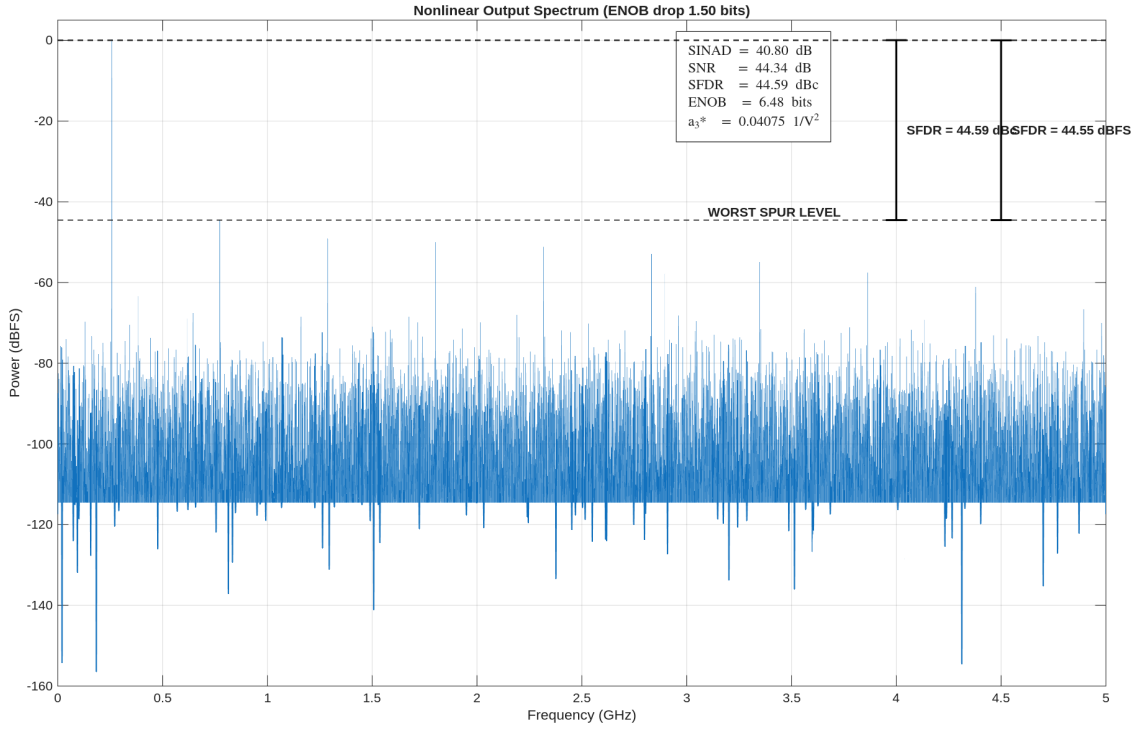


Figure 3: FFT of Non-Ideal ADC w/ Third Order Non-Linearity

The simulation converged to a maximum tolerable non-linearity coefficient of $a_3 =$

0.04075 V^{-2}. At this level of distortion, ENOB was degraded exactly by 1.5 bits, from the baseline 7.98 to 6.48 bits.

Figure 3 shows the output spectrum with the determined cubic non-linearity applied. The resulting dynamic performance metrics are:

- **Max Tolerable a_3:** 0.04075 V^{-2}
- **ENOB:** 6.48 bits
- **SINAD:** 40.80 dB
- **SNR:** 44.34 dB
- **SFDR:** 44.59 dBc

The spectrum shows reveals a distinct harmonic signature characteristic of symmetrical distortion.

The cubic term (x^3) affects the positive and negative signal excursions symmetrically, so the distortion it introduces is dominated by odd-order harmonics. In this result, the 3rd harmonic (H3) at 772.7 MHz is the dominant spur at -44.59 dBc, making it the limiting tone for SFDR, while the 5th harmonic (H5) at 1.28 GHz is the next most significant component at -49.34 dBc.

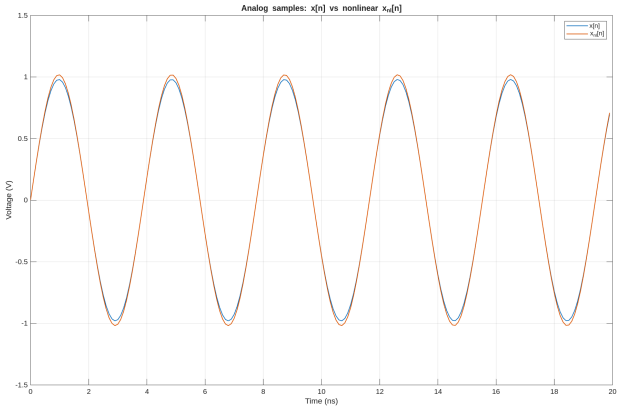
As expected from the model, even-order harmonics are negligible. The 2nd harmonic (H2) is measured at -91.63 dBc, which is buried near the quantization noise floor. This confirms that the simulated non-linearity is purely compressive/expansive and does not introduce DC offsets or asymmetries typical of quadratic (x^2) distortion.

The presence of these high-power harmonics degrades the SINAD significantly (down to 40.80 dB) compared to the SNR (44.34 dB). This gap of ≈ 3.5 dB indicates that the system's performance is now distortion-limited rather than noise-limited.

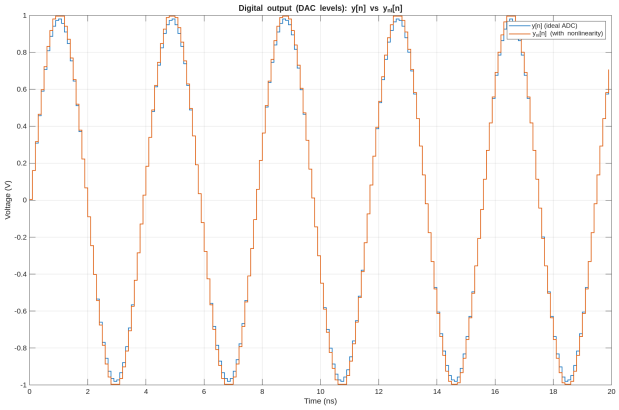
The calculated non-linearity coefficient of $a_3 = 0.04075\ V^{-2}$ implies that the ADC's linearity is highly dependent on the input signal amplitude. Because the distortion term

scales with the cibe of the voltage, the error is negligible at low signal levels but grows rapidly as the signal approaches full scale. Essentially, the ADC should perform nearly ideally for small signals, but the effective resolution degrades at the rails.

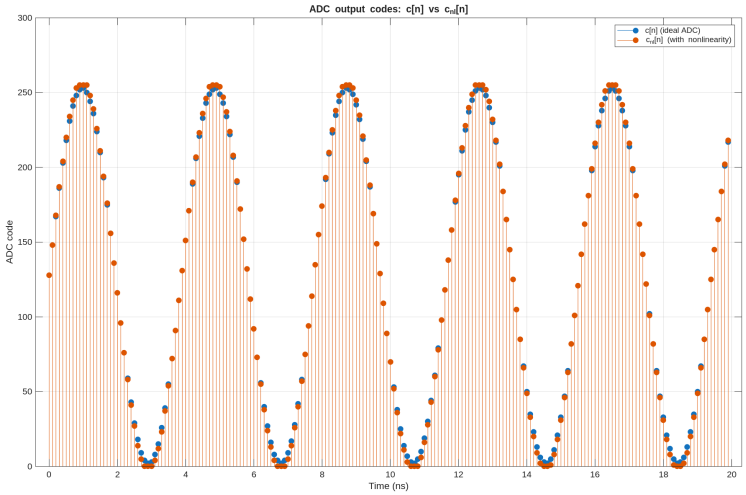
This is shown in Figure 4:



(a) Comparison of ideal input $x[n]$ and distorted input $x_{nl}[n]$. Note the amplitude expansion at signal peaks.



(b) Quantized voltage levels ($y[n]$ vs $y_{nl}[n]$) showing the shift in effective values.



(c) Deviation in digital output codes ($c[n]$ vs $c_{nl}[n]$) due to cubic non-linearity.

Figure 4: Time-domain impact of cubic non-linearity ($a_3 \approx 0.041$ V^{-2}) on signal integrity and quantization.

4 Random Noise

In this section, the impact of random fluctuations typical of thermal noise, or electromagnetic interference in the analog front-end on the ADC was examined. To do so, I determined the maximum RMS noise voltage, σ, the system could withstand while maintaining an ENOB drop of no more than 1 bit (ENOB ≈ 6.98).

4.1 Modelling Random Noise

Random noise was modelled as an Additive White Gaussian Noise source introduced prior to quantization. The noisy input signal, $x_{noisy}[n]$, is thus:

$$x_{noisy} = x[n] + \sigma w[n]$$

where $w[n]$ is a standard normal variable ($\mu = 0, \sigma^2 = 1$) and σ represents the RMS noise voltage.

4.2 Noise Simulation Results

The simulation converged to a maximum tolerable RMS noise voltage of $\sigma = 3.88$ mV. At this noise level, ENOB dropped to 6.97 bits. The FFT can be shown in Figure 5.

- **Max Tolerable Noise:** 3.88 mV
- **ENOB:** 6.97 bits
- **SNR:** 43.71 dB
- **SINAD:** 43.69 dB
- **SFDR:** 71.09 dBc

Furthermore, From Figure 5, we can clearly see that the spectral signature of random noise is fundamentally different from non-linearity. In Section 3, we saw that non-linearity

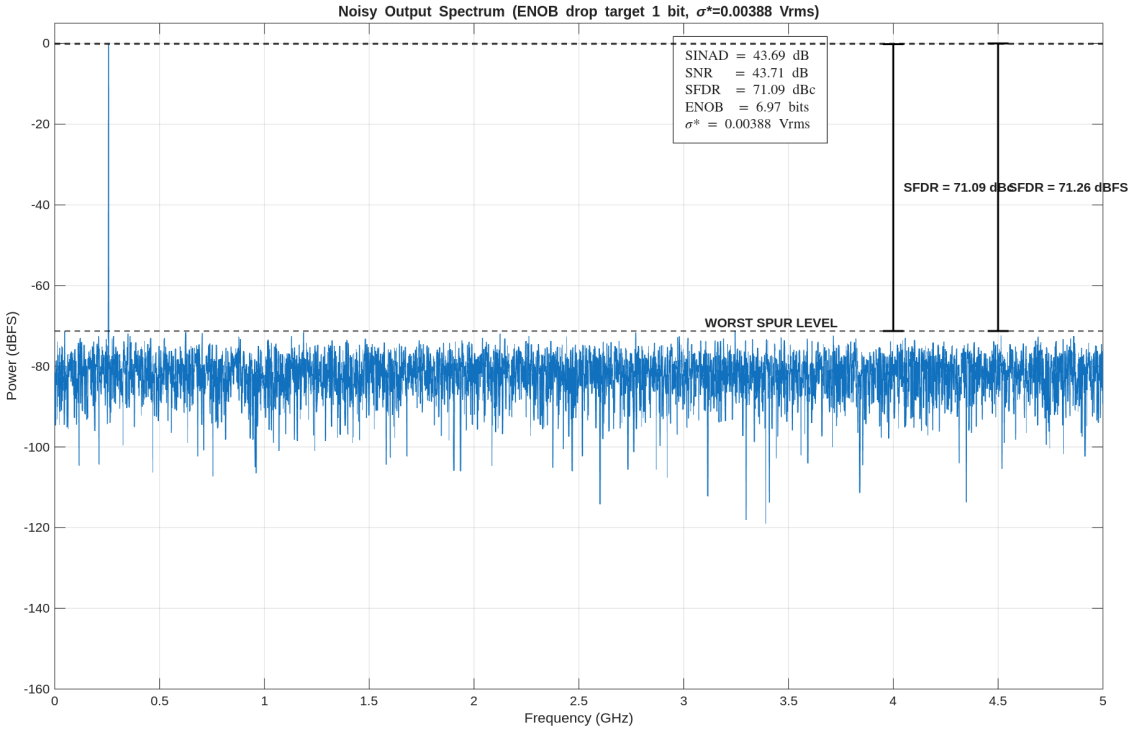


Figure 5: FFT spectrum with maximum tolerable random noise ($\sigma \approx 3.88\ \mathrm{mV}_{rms}$). Note the elevated noise floor but lack of harmonic spurs.

generated specific harmonic spurs, whereas here, the added Gaussian noise distributes its energy evenly across all frequencies, resulting in a uniform elevation of the noise floor.

SFDR remains high (71.09 dBc) while SNR and SINAD degrade. Interestingly, SINAD remains nearly identical to SNR in this case, again because random noise only elevates the noise floor, and not spurs are created.

Also, the determined threshold of 3.88 mV (RMS) corresponds to approximately half LSB ($\sigma \approx \frac{\Delta_{LSB}}{2}$). meaning an RMS noise level of just half LSB is sufficient to degrade the ADC's effective resolution by one full bit.

5 Jitter

Jitter is critical in high-speed converters, as timing errors directly result into voltage errors proportional to the input slew rate. Here, the effect of jitter on the ADC is investigated.

5.1 Modelling Jitter

Jitter was modelled as a random Gaussian perturbation applied to the time vector before the sampling of the input sinousoid. Unlike additive noise, Section 4, which adds error to the voltage vertically, here, jitter adds error horizontally in time. The jittered sample instants, t_j, were defined as:

$$t_j[n] = nT_s + \delta t[n]$$

where $\delta t[n]$ is a zero-mean gaussian random variable with standard deviation, σ_t. The sampled input signal then becomes:

$$x_j[n] = A\sin(2\pi f_{in} t_j[n] + \phi)$$

Essentially, phase noise is simulated where the error magnitude depends on the derivative of the input signal.

5.2 Jitter Performance Analysis

A parametric sweep of RMS jitter (σ_t) was performed from 0 fs to 4500 fs to observe the transition from a quantization-limited regime to a jitter-limited regime.

Furthermore, the theoretical SNR limited by jitter ($\text{SNR}_{j,th}$) was calculated for each point in the sweep. This metric represents the machimum achievable SNR if the ADC were limited solely by sampling uncertainty. It is calculated by:

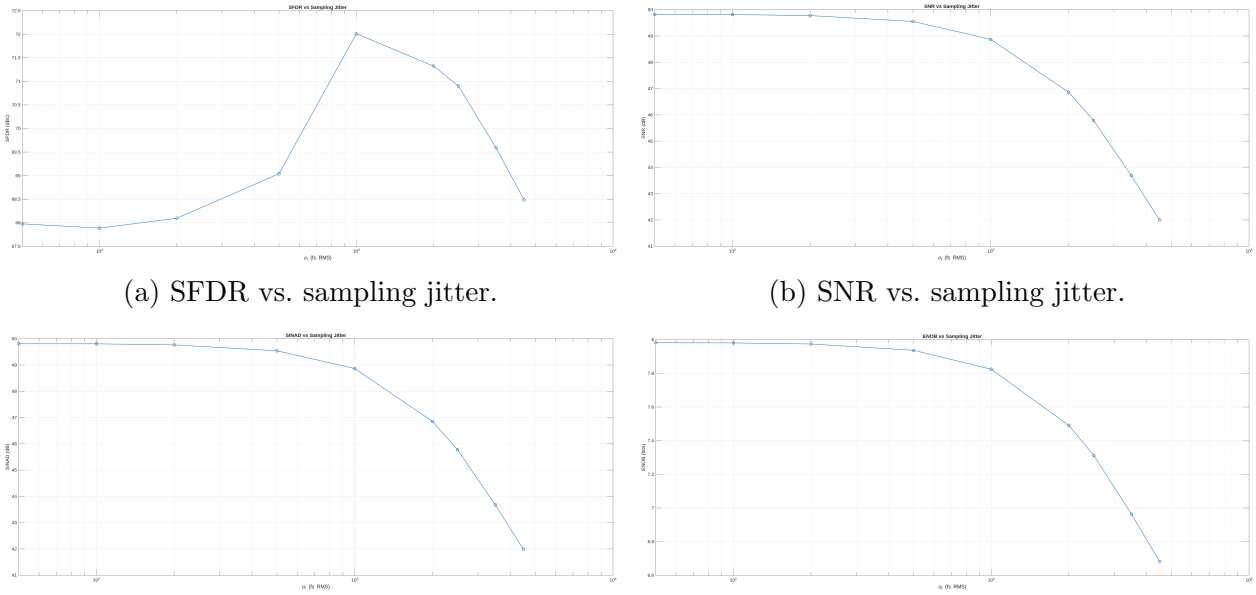
$$SNR_{j,th} = -20\log_{10}(2\pi f_{in}\sigma_t)$$

From Figure 6, the simulation results reveal two distinct operating regimes.

In the quantization-limited region (0 - 500 fs), the system performance is dominated entirely by the 8-bit quantization noise. SNR, SINAD and ENOB remain flat in that region. Within this region $SNR_{j,th}$ ranged from near infintiy to 61.48 dB, far superior to the ADC's intrinsic 49.81 dB quantization limi (as determined in Section 2); in effect the jitter contribution is negligible.

Past 500 fs, the jitter-limited region, the phase noise floor rises sufficiently to cross the quantization noise floor. Particularly, at $\sigma_t = 2500$ fs, $SNR_{j,th}$ drops to 47.86 dB, and the performance metrics begin to roll off.

By $\sigma_t = 3500$ fs, roughly 1-bit in resolution has been lost.



(a) SFDR vs. sampling jitter.

(b) SNR vs. sampling jitter.

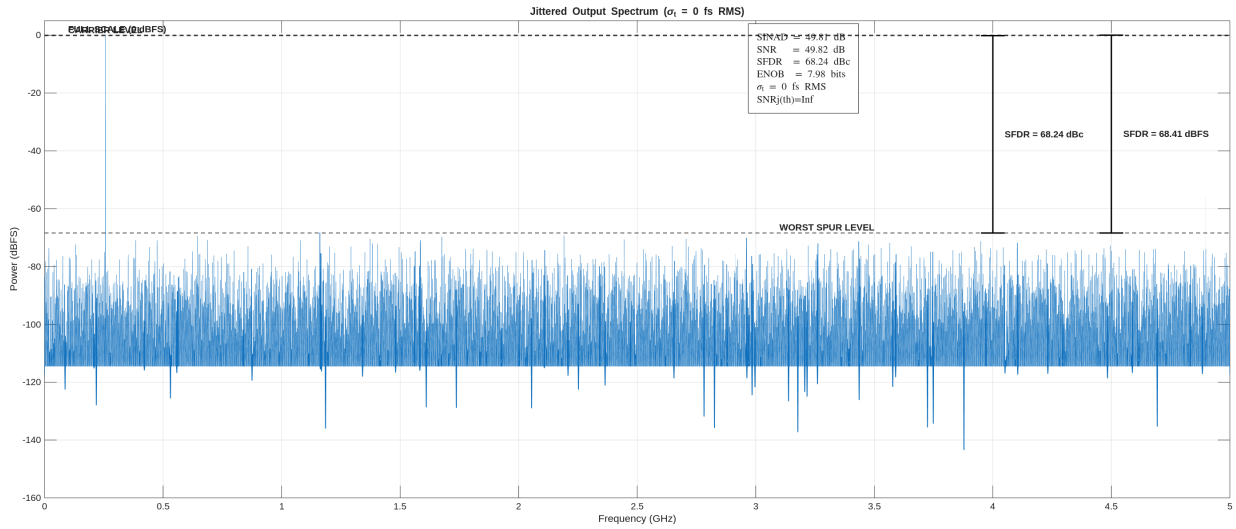
(c) SINAD vs. sampling jitter.

(d) ENOB vs. sampling jitter.

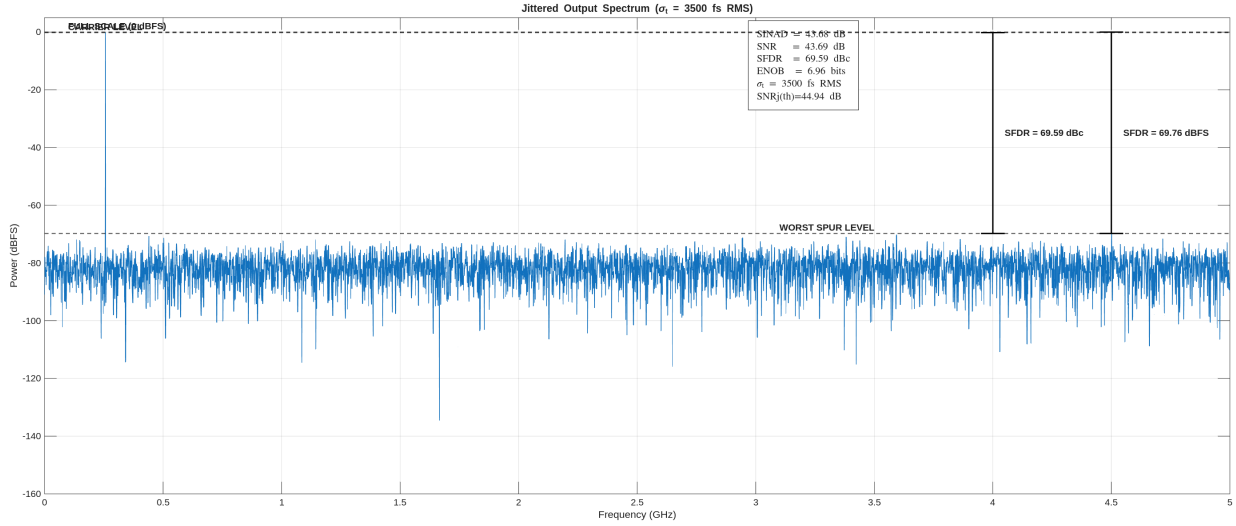
Figure 6: Effect of sampling jitter σ_t on ADC dynamic performance metrics.

Essentially, jitter introduces a new source of noise, phase noise. Phase noise sits on top or is buried within the quantization noise. The total noise floor is thus what we see in the FFT. With perfect sampling timing, no phase noise the floor is purely quantization noise. With jitter, the floor is now both phase noise and quantization noise.

This can be seen in the following Figure 7:



(a) Output spectrum with no sampling jitter ($\sigma_t = 0$ fs RMS).



(b) Output spectrum with sampling jitter ($\sigma_t = 3500$ fs RMS).

Figure 7: ADC output spectra illustrating the impact of sampling jitter on the noise floor and dynamic metrics.

6 Conclusion

This characterization demonstrates that realizable ADC performance is constrained by three distinct error mechanisms beyond ideal quantization. Front-end non-linearity introduces harmonic distortion, degrading SFDR and SINAD without affecting the broadband noise floor. Conversely, both additive random noise and aperture jitter elevate the total noise

floor—the former via vertical voltage errors and the latter via horizontal phase noise. The jitter sweep specifically highlights a critical transition where timing uncertainty overrides bit resolution, proving that for high-speed systems, minimizing clock jitter is just as essential as maintaining linearity and thermal noise margins to achieve the theoretical dynamic range.