BINARY CODE c b a	CIRCULAR CODE d c b a
0 0 0	0 0 0 0
0 0 1	0 0 0 1
0 1 0	0 0 1 1
0 1 1	0 1 1 1
1 0 0	1 1 1 1
1 0 1	1 1 1 0
1 1 0	1 1 0 0
1 1 1	1 0 0 0

Table 3.3: Binary-circular code implementation

tions for circular codes. Such a code appears in "folding" analog-to-digital converters, too.

3.4 Full-flash converters

In an N-bit flash A/D converter, $2^N - 1$ reference voltages and comparator stages are used to convert the analog input signal into a thermometer-like digital output code (see Figure 3.1). This code is converted into a binary output code using a ROM structure. In today's technologies, 8-bit converters having a reasonable die size and consuming moderate power are available. Increasing the resolution to 10 bits increases the die size and power dissipation roughly four times. In practice, however, there is a limit to the power dissipation that can be handled in IC packages. Therefore, the power per comparator stage must be drastically reduced to keep the overall power dissipation at the same level as the 8-bit unit. As a result, the bandwidth of the comparators has to be reduced, resulting in a much lower effective analog bandwidth for the converter. The bandwidth of a system is mostly related to biasing current, which in turn results in power dissipation. Because of the increase in size, it is more difficult to distribute clock and input signal lines without introducing delay-induced errors exceeding $\pm \frac{1}{2}$ LSB, and to match the properties of all these comparators within the same specification. The input capacitance of the system increases linearly with the number of comparators, making it impractical to incorporate an input signal buffer on the chip. Even external buffers are difficult to design and need a large power-driving capability at high frequencies. The large number of compara-

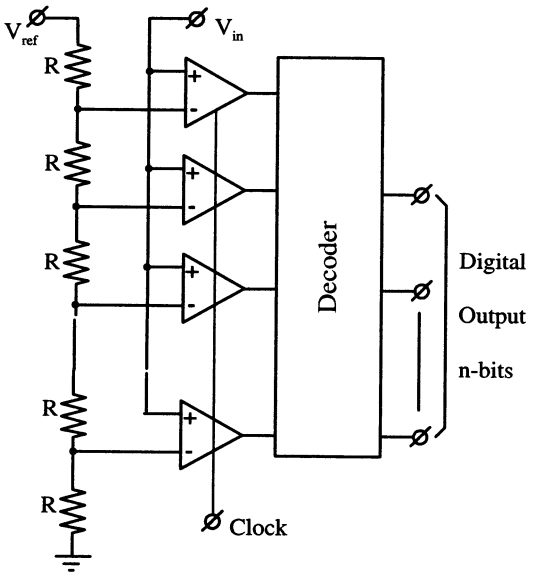

Figure 3.1: Full-flash A/D converter structure

tors results in a heavy loading of the clock driving circuits. Small rise and fall times of the clock signals are difficult to obtain and therefore external clock drivers are often required.

3.4.1 Comparator input amplifier

The continues time comparator input amplifier circuit diagram is shown in Figure 3.2. The circuit consists of a differential amplifier M_1, M_2 which compares the analog input signal with the reference voltage generated across a tapped resistor. The input signal is amplified and appears across the drain resistors R. Because of finite matching properties of MOS devices it is important to know the offset voltage of the input amplifier. This offset voltage is defined as the difference in gate voltage required to give a zero differential output voltage as shown in Figure 3.2. As will be shown in a separate chapter offset voltage of CMOS transistors depends on the technology used. Furthermore the designer has the ability to change the size of devices M_1 and M_2 to tailor the offset voltage. In practice this can be done only over a limited range. Having a reference voltage of 1 V and needing an 8-bit resolution, the reference step size becomes $\frac{1}{2^N} \approx 4$ mV. Suppose we use a 0.5 μm technology, then the *unit* offset voltage (a_{vth}) is about 10 mV. To

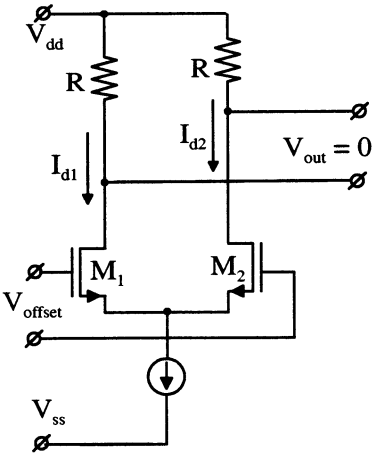

Figure 3.2: Comparator Input Amplifier

get a 1 σ offset of 1 mV we have to increase the device size according to:

$$V_{offset} = \frac{a_{vth}}{\sqrt{WL}}. \tag{3.1}$$

Using equation 3.1 we obtain for WL = 100. This means with W = 100 μm and L = 1 μm this requirement is fulfilled. Such a big size device has a large input capacitance. With C_{unit} = 2 fF ($1\mu^2$) we obtain per differential pair an input capacitance of:

$$C_{inputpair} = \frac{1}{2}WL.2fF = 100fF. \tag{3.2}$$

In an 8-bit full flash converter we have about $2^N = 256$ comparator input amplifiers so the total input capacitance of the 8-bit converter becomes:

$$256.100fF \approx 26pf. \tag{3.3}$$

This input capacitance is non-linear because always a limited number of input pairs are only active and contributing to the decision signals. To drive such a large input capacitance a buffer amplifier is needed. Such a buffer amplifier is difficult to design and consumes a lot of power. It is therefore important to reduce the number of input amplifier pairs and at the same time to reduce the offset voltage. Two useful techniques will be described now.