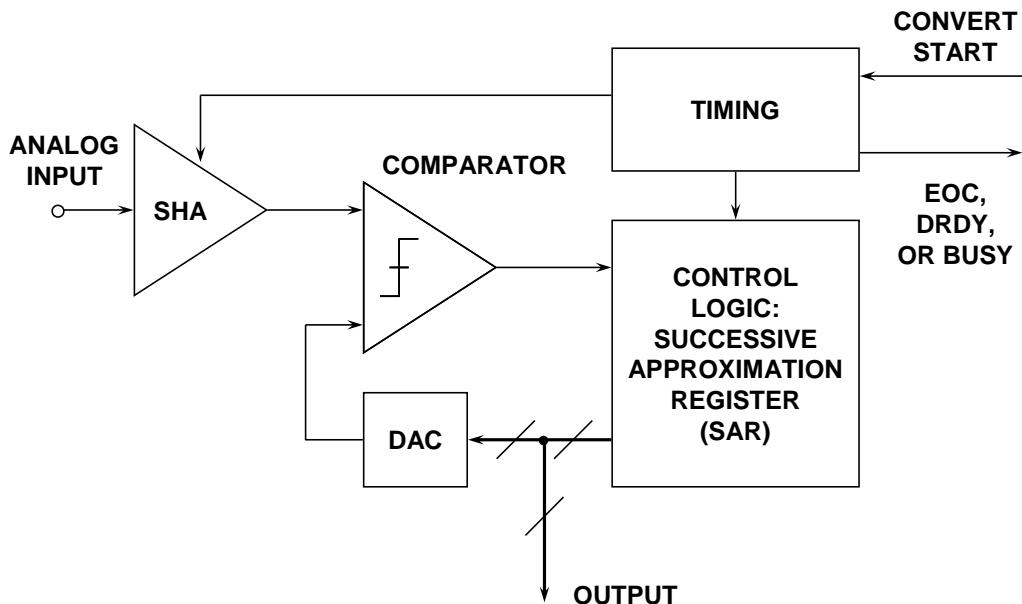# ADC Architectures II: Successive Approximation ADCs

by Walt Kester

INTRODUCTION

The successive approximation ADC has been the mainstay of data acquisition systems for many years. Recent design improvements have extended the sampling frequency of these ADCs into the megahertz region with 18-bit resolution. The Analog Devices PulSAR® family of SAR ADCs uses internal switched capacitor techniques along with auto calibration and offers 18-bits at 2 MSPS (AD7641) on CMOS processes without the need for expensive thin-film laser trimming. At the 16-bit level, the AD7625 (6 MSPS) and AD7626 (10 MSPS) also represent breakthrough technology.

The basic successive approximation ADC is shown in Figure 1. It performs conversions on command. In order to process ac signals, SAR ADCs must have an input sample-and-hold (SHA) to keep the signal constant during the conversion cycle.
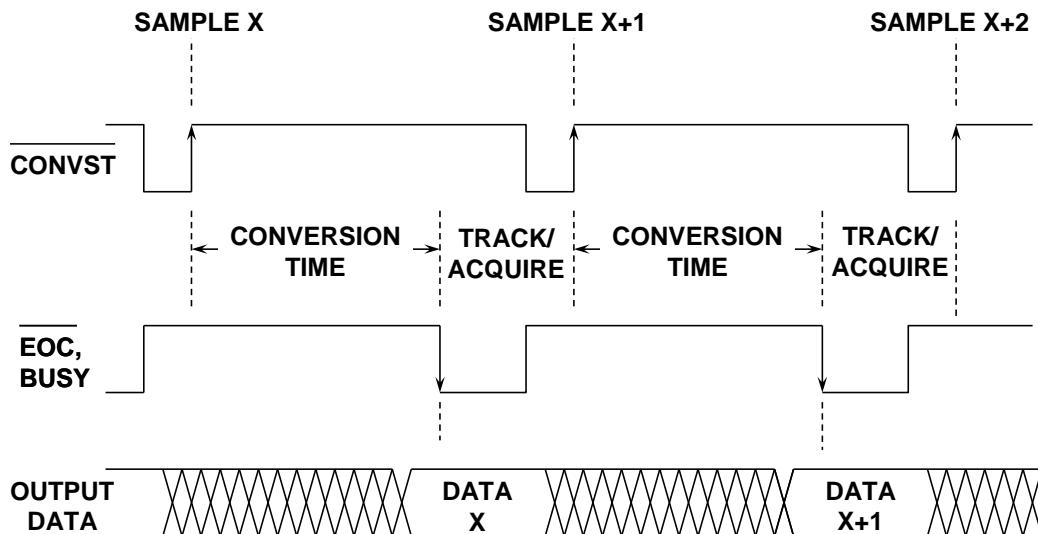

*Figure 1: Basic Successive Approximation ADC
(Feedback Subtraction ADC)*

On the assertion of the CONVERT START command, the sample-and-hold (SHA) is placed in the *hold* mode, and the internal DAC is set to midscale. The comparator determines whether the SHA output is above or below the DAC output, and the result (bit 1, the most significant bit of the conversion) is stored in the successive approximation register (SAR). The DAC is then set either to ¼ scale or ¾ scale (depending on the value of bit 1), and the comparator makes the decision for bit 2 of the conversion. The result is stored in the register, and the process continues

until all of the bit values have been determined. When all the bits have been set, tested, and reset or not as appropriate, the contents of the SAR correspond to the value of the analog input, and the conversion is complete. These bit "tests" form the basis of a serial output version SAR-based ADC. Note that the acronym "SAR" actually stands for Successive Approximation Register (the logic block that controls the conversion process), but is universally accepted as the acronym for the architecture itself.

SAR ADC TIMING

The fundamental timing diagram for a typical SAR ADC is shown in Figure 2. The end of conversion is generally indicated by an end-of-convert (EOC), data-ready (DRDY), or a busy signal (actually, *not*-BUSY indicates end of conversion). The polarities and name of this signal may be different for different SAR ADCs, but the fundamental concept is the same. At the beginning of the conversion interval, the signal goes high (or low) and remains in that state until the conversion is completed, at which time it goes low (or high). The trailing edge is generally an indication of valid output data, but the data sheet should be carefully studied—in some ADCs additional delay is required before the output data is valid.

Figure 2: Typical SAR ADC Timing

An N-bit conversion takes N steps. It would seem on superficial examination that a 16-bit converter would have twice the conversion time of an 8-bit one, but this is not the case. In an 8-bit converter, the DAC must settle to 8-bit accuracy before the bit decision is made, whereas in a 16-bit converter, it must settle to 16-bit accuracy, which takes a lot longer. In practice, 8-bit successive approximation ADCs can convert in a few hundred nanoseconds, while 16-bit ones will generally take several microseconds.

While there are some variations, the fundamental timing of most SAR ADCs is similar and relatively straightforward. The conversion process is generally initiated by asserting a

CONVERT START signal. The $\overline{\text{CONVST}}$ signal is a negative-going pulse whose positive-going edge actually initiates the conversion. The internal sample-and-hold (SHA) amplifier is placed in the hold mode on this edge, and the various bits are determined using the SAR algorithm. The negative-going edge of the $\overline{\text{CONVST}}$ pulse causes the $\overline{\text{EOC}}$ or BUSY line to go high. When the conversion is complete, the BUSY line goes low, indicating the completion of the conversion process. In most cases the trailing edge of the BUSY line can be used as an indication that the output data is valid and can be used to strobe the output data into an external register. However, because of the many variations in terminology and design, the individual data sheet should always be consulted when using a specific ADC. An important characteristic of a SAR ADC is that at the end of the conversion time, the data corresponding to the sampling clock edge is available with no "pipeline" delay. This makes the SAR ADC especially easy to use in "single-shot" and multiplexed applications.
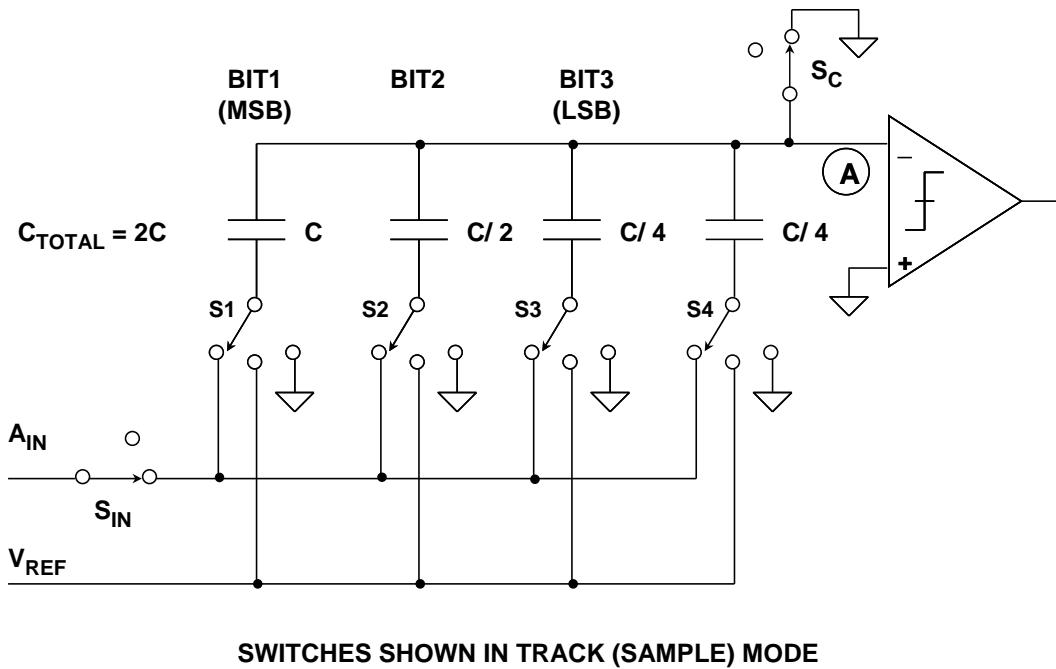
It should also be noted that some SAR ADCs require an external high frequency clock in addition to the CONVERT START command. In most cases there is no need to synchronize the CONVERT START command to the high frequency clock. The frequency of the external clock, if required, generally falls in the range of 1 MHz to 30 MHz depending on the conversion time and resolution of the ADC. Other SAR ADCs have an internal oscillator which is used to perform the conversions and only require the CONVERT START command. Because of their architecture, SAR ADCs generally allow single-shot conversion at any repetition rate from dc to the converter's maximum conversion rate—however, there are some exceptions, so the data sheet should always be consulted.

Notice that the overall accuracy and linearity of the SAR ADC is determined primarily by the internal DAC. Until recently, most precision SAR ADCs used laser-trimmed thin-film DACs to achieve the desired accuracy and linearity. The thin-film resistor trimming process adds cost, and the thin-film resistor values may be affected when subjected to the mechanical stresses of packaging.

For these reasons, switched capacitor (or charge-redistribution) DACs have become popular in newer SAR ADCs. The advantage of the switched capacitor DAC is that the accuracy and linearity is primarily determined by high-accuracy photolithography, which in turn controls the capacitor plate area and the capacitance as well as matching. In addition, small capacitors can be placed in parallel with the main capacitors which can be switched in and out under control of autocalibration routines to achieve high accuracy and linearity without the need for thin-film laser trimming. Temperature tracking between the switched capacitors can be better than 1 ppm/°C, thereby offering a high degree of temperature stability. Modern fine-line CMOS processes are ideal for the switched capacitor SAR ADC, and the cost is therefore low.

A simple 3-bit capacitor DAC is shown in Figure 3. The switches are shown in the *track*, or *sample* mode where the analog input voltage, A_{IN}, is constantly charging and discharging the parallel combination of all the capacitors. The *hold* mode is initiated by opening S_{IN}, leaving the sampled analog input voltage on the capacitor array. Switch S_C is then opened allowing the voltage at node A to move as the bit switches are manipulated. If S1, S2, S3, and S4 are all connected to ground, a voltage equal to $-A_{IN}$ appears at node A. Connecting S1 to V_{REF} adds a voltage equal to $V_{REF}/2$ to $-A_{IN}$. The comparator then makes the MSB bit decision, and the SAR

either leaves S1 connected to V_{REF} or connects it to ground depending on the comparator output (which is high or low depending on whether the voltage at node A is negative or positive, respectively). A similar process is followed for the remaining two bits. At the end of the conversion interval, S1, S2, S3, S4, and S_{IN} are connected to A_{IN}, S_C is connected to ground, and the converter is ready for another cycle.

SWITCHES SHOWN IN TRACK (SAMPLE) MODE
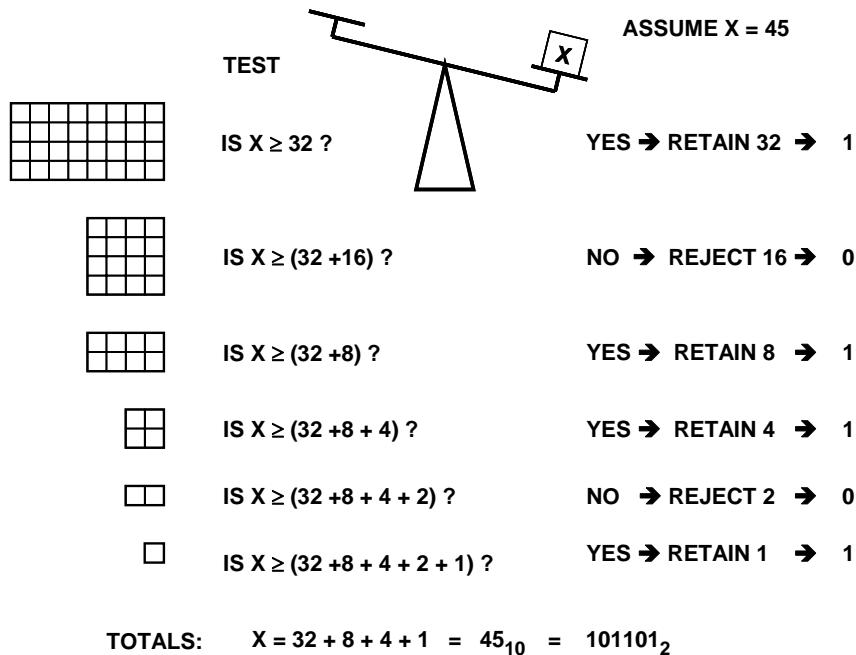
Figure 3: 3-Bit Switched Capacitor DAC

Note that the extra LSB capacitor (C/4 in the case of the 3-bit DAC) is required to make the total value of the capacitor array equal to 2C so that binary division is accomplished when the individual bit capacitors are manipulated.

The operation of the capacitor DAC (cap DAC) is similar to an R-2R resistive DAC. When a particular bit capacitor is switched to V_{REF}, the voltage divider created by the bit capacitor and the total array capacitance (2C) adds a voltage to node A equal to the weight of that bit. When the bit capacitor is switched to ground, the same voltage is subtracted from node A.

HISTORICAL PERSPECTIVES ON SAR ADCS

The basic algorithm used in the successive approximation (initially called *feedback subtraction*) ADC conversion process can be traced back to the 1500s relating to the solution of a certain mathematical puzzle regarding the determination of an unknown weight by a minimal sequence of weighing operations (Reference 1). In this problem, as stated, the object is to determine the least number of weights which would serve to weigh an integral number of pounds from 1 lb to 40 lb using a balance scale. One solution put forth by the mathematician Tartaglia in 1556, was to use the series of weights 1 lb, 2 lb, 4 lb, 8 lb, 16 lb, and 32 lb. The proposed weighing algorithm is the same as used in modern successive approximation ADCs. (It should be noted

that this solution will actually measure unknown weights up to 63 lb rather than 40 lb as stated in the problem). The algorithm is shown in Figure 4 where the unknown weight is 45 lbs. The balance scale analogy is used to demonstrate the algorithm.

TEST   ASSUME X = 45

IS X ≥ 32 ?   YES ➔ RETAIN 32 ➔ 1

IS X ≥ (32 +16) ?   NO ➔ REJECT 16 ➔ 0

IS X ≥ (32 +8) ?   YES ➔ RETAIN 8 ➔ 1

IS X ≥ (32 +8 + 4) ?   YES ➔ RETAIN 4 ➔ 1

IS X ≥ (32 +8 + 4 + 2) ?   NO ➔ REJECT 2 ➔ 0

IS X ≥ (32 +8 + 4 + 2 + 1) ?   YES ➔ RETAIN 1 ➔ 1

TOTALS: $X = 32 + 8 + 4 + 1 = 45_{10} = 101101_2$

Figure 4: Successive Approximation ADC Algorithm

Early implementations of the successive approximation ADC did not use either DACs or successive approximation registers but implemented similar functions in a variety of ways. In fact, early SAR ADCs were referred to as *sequential coders*, *feedback coders*, or *feedback subtractor coders*. The term *SAR ADC* came about in the 1970s when commercial successive approximation register logic ICs such as the 2503 and 2504 became available from National Semiconductor and Advanced Micro Devices. These devices were designed specifically to perform the register and control functions in successive approximation ADCs and were standard building blocks in many modular and hybrid data converters.

From a data conversion standpoint, the successive approximation ADC architecture formed the building block for the T1 PCM carrier system and is still a popular architecture today, but the exact origin of this architecture is not clear. Although countless patents have been granted relating to refinements and variations on the successive approximation architecture, they do not claim the fundamental principle.

The first mention of the successive approximation ADC architecture (actually a *sequential coder*) in the context of PCM was by J. C. Schelleng of Bell Telephone Laboratories in a patent filed in 1946 (Reference 2). The design does not use an internal DAC, but implements the approximation process in a somewhat novel manner involving the addition of binary weighted reference voltages. Details of this vacuum tube design are discussed in the patent.

A much more elegant implementation of the successive approximation ADC is described by Goodall of Bell Telephone Labs in a 1947 article (Reference 3). This ADC has 5-bit resolution and samples the voice channel at a rate of 8 kSPS. The voice signal is first sampled, and the corresponding voltage stored on a capacitor. It is then compared to a reference voltage which is equal to ½ the full-scale voltage. If it is greater than the reference voltage, the MSB is registered as a "1," and an amount of charge equal to ½ scale is subtracted from the storage capacitor. If the voltage on the capacitor is less than ½ scale, then no charge is removed, and the bit is registered as a "0". After the MSB decision is completed, the cycle continues for the second bit, but with the reference voltage now equal to ¼ scale. The process continues until all bit decisions are completed. This concept of charge redistribution is similar to modern switched-capacitor DACs.

Both the Schelleng and the Goodall ADCs use a process of addition/subtraction of binary weighted reference voltages to perform the SAR algorithm. Although the DAC function is there, it is not performed using a traditional binary weighted DAC. The ADCs described by H. R. Kaiser et. al. (Reference 4) and B. D. Smith (Reference 5) in 1953 use an actual binary weighted DAC to generate the analog approximation to the input signal, similar to modern SAR ADCs. Smith also points out that non-linear ADC transfer functions can be achieved by using a non-uniformly weighted DAC. This technique formed the basis of companding voiceband codecs used in early PCM systems. (See Tutorial MT-018, "Intentionally Nonlinear DACs.") Before this non-linear ADC technique was developed, linear ADCs were used, and the compression and expansion functions were performed by diode/resistor networks which had to be individually calibrated and held at a constant temperature to prevent drift errors (Reference 6).

Of course, no discussion on ADC history would be complete without crediting the truly groundbreaking work of Bernard M. Gordon at EPSCO (now Analogic, Incorporated). Gordon's 1955 patent application (Reference 7) describes an all-vacuum tube 11-bit, 50-kSPS successive approximation ADC—representing the first commercial offering of a complete converter (see Figure 5). The DATRAC was offered in a 19" × 26" × 15" housing, dissipated several hundred watts, and sold for approximately $8000.00.

In a later patent (Reference 8), Gordon describes the details of the logic block required to perform the successive approximation algorithm. The SAR logic function was later implemented in the 1970s by National Semiconductor and Advanced Micro Devices—the popular 2502/2503/2504 family of IC logic chips. These chips were to become an integral building block of practically all modular and hybrid successive approximation ADCs of the 1970s and 1980s.

◆ 19" × 15" × 26"

◆ 150 lbs

◆ $8,500.00

Courtesy,
Analogic Corporation
8 Centennial Drive
Peabody, MA 01960

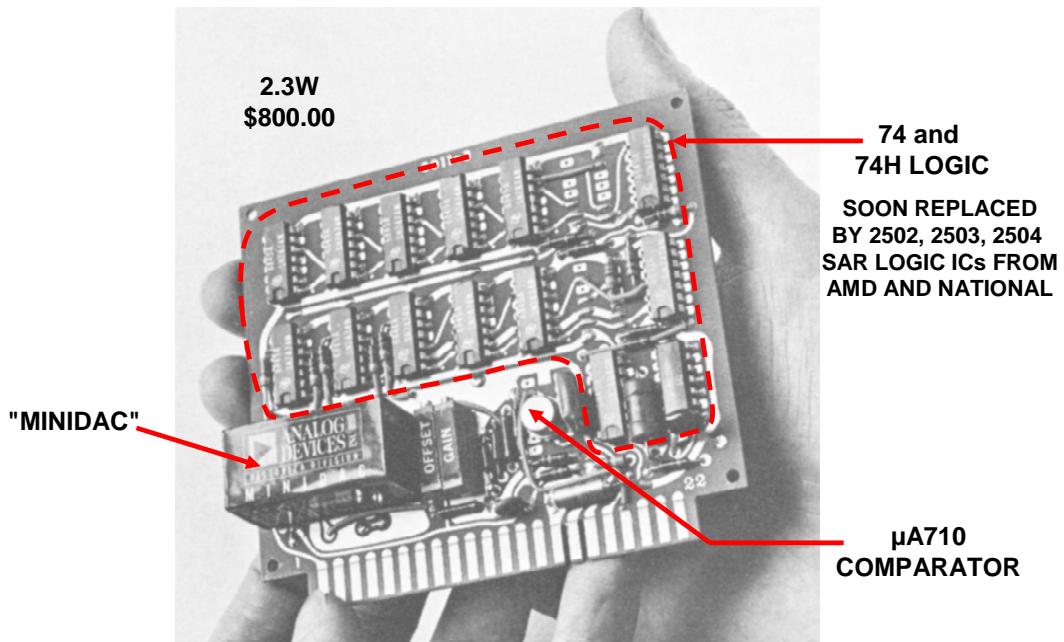http://www.analogic.com

Figure 5: 1954 "DATRAC" 11-Bit, 50-kSPS SAR ADC
Designed by Bernard M. Gordon at EPSCO

ANALOG DEVICES ENTERS THE DATA CONVERTER ARENA IN 1969

In 1965, Ray Stata and Matt Lorber founded Analog Devices, Inc. (ADI) in Cambridge, MA. The initial product offerings were high performance modular op amps, but in 1969 ADI acquired Pastoriza Electronics, a leader in data converter products, thereby making a solid commitment to both data acquisition and linear products.

Pastoriza had a line of data acquisition products, and Figure 6 shows a photograph of a 1969 12-bit, 10-µs general purpose successive approximation ADC, the ADC-12U, that sold for approximately $800.00. The architecture was successive approximation, and the ADC-12U utilized a µA710 comparator, a modular 12-bit "Minidac," and 14 7400-series logic packages to perform the successive approximation conversion algorithm.

2.3W
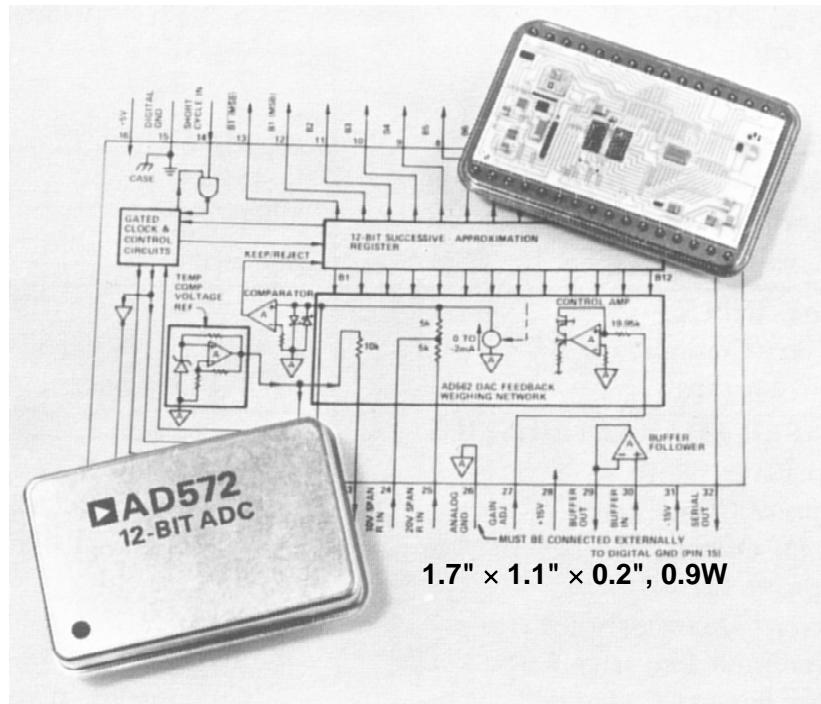$800.00

74 and
74H LOGIC

SOON REPLACED
BY 2502, 2503, 2504
SAR LOGIC ICs FROM
AMD AND NATIONAL

"MINIDAC"

µA710
COMPARATOR

*Figure 6: ADC-12U 12-Bit, 10-µs SAR ADC from Pastoriza Division of
Analog Devices, 1969*

The "Minidac" module was actually constructed from "quad switch" ICs (AD550) and a thin film network (AD850). These early DAC building blocks are discussed further in Tutorial MT-015, "DAC Architectures II: Binary DACs."

Notice that in the ADC-12U, the implementation of the successive approximation algorithm required 14 logic packages. In 1958, Bernard M. Gordon had filed a patent on the logic to perform the successive approximation algorithm (Reference 19), and in the early 1970s, Advanced Micro Devices and National Semiconductor introduced commercial *successive approximation register* logic ICs: the 2502 (8-bit, serial, not expandable), 2503 (8-bit, expandable) and 2504 (12-bit, serial, expandable). These were designed specifically to perform the register and control functions in successive approximation ADCs. These became standard building blocks in many modular and hybrid data converters.
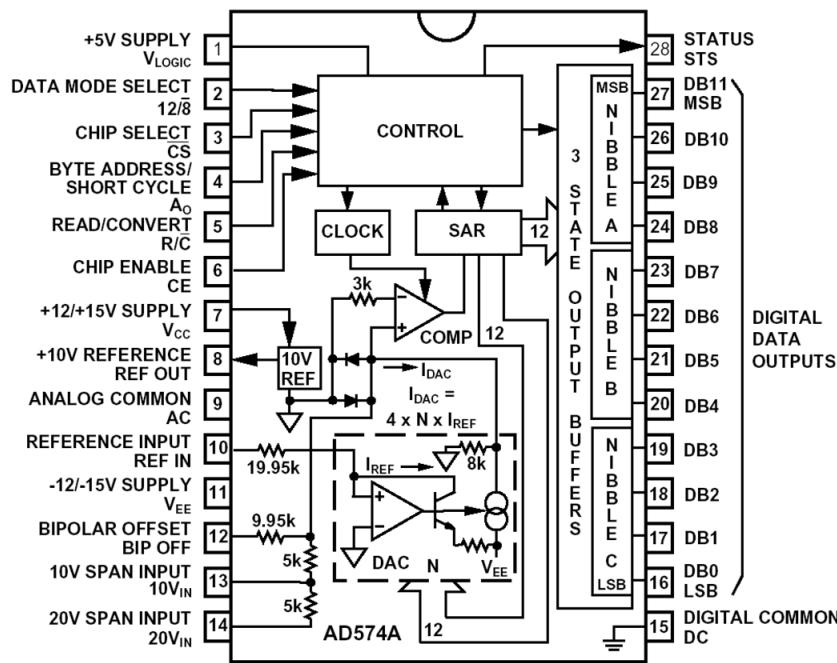
Analog Devices continued to pioneer in data conversion after 1969. Modules gradually evolved into hybrid circuits during the 1970s. Hybrids generally utilize ceramic substrates with either thick or thin film conductors. Individual die are bonded to the substrate (usually with epoxy), and wire bonds make the connections between the bond pads and the conductors. The hybrid is usually hermetically sealed in some sort of ceramic or metal package. Accuracy was achieved by trimming thick or thin film resistors after assembly and interconnection, but before sealing. Manufacturers used thin film networks, discrete thin film resistors, deposited thick or thin film resistors, or some combination of the above.

An excellent example of hybrid technology was the AD572 12-bit, 25-µs SAR ADC introduced by Analog Devices in 1977. The AD572 was complete with internal clock, voltage reference, comparator, and input buffer amplifier. The SAR register was the popular 2504. The internal DAC was comprised of a 12-bit switch chip and an actively trimmed thin film ladder network (separately packaged as the two-chip AD562 DAC). The AD572 was the first military-approved 12-bit ADC processed to MIL-STD-883B, and specified over the full operating temperature range of –55°C to +125°C. A photograph of the AD572 is shown in Figure 7.

Figure 7: AD572 12-Bit, 25-µs Mil-Approved Hybrid ADC, 1977

Analog Devices also pioneered in monolithic data converters. Probably the most significant SAR ADC ever introduced was the 12-bit, 35-µs AD574 in 1978. The AD574 represents a complete solution, including buried Zener reference, timing circuits, and three-state output buffers for direct interfacing to an 8-, 12-, or 16-bit microprocessor bus. In its introductory form, the AD574 was manufactured using compound monolithic construction, based on two chips—one an AD565 12-bit current-output DAC, including reference and thin film scaling resistors; and the other containing the successive approximation register (SAR) and microprocessor interface logic functions as well as a precision latching comparator. The AD574 soon emerged as the industry-standard 12-bit ADC in the early 1980s. In 1985, the device became available in single-chip monolithic form for the first time; thereby making low-cost commercial plastic packaging possible. A simplified block diagram of the AD574 is shown in Figure 8.
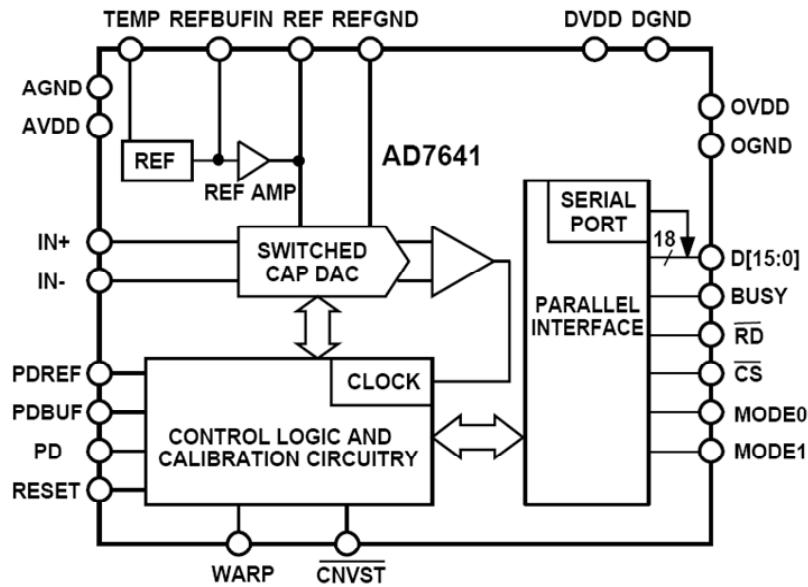
Figure 8: The Industry-Standard [AD574](#) 12-Bit, 35-µs IC ADC, 1978

MODERN SAR ADCs

Because of their popularity, successive approximation ADCs are available in a wide variety of resolutions, sampling rates, input and output options, package styles, and costs. Many SAR ADCs now offer on-chip input multiplexers, making them the ideal choice for multichannel data acquisition systems. It would be impossible to attempt to discuss all types of SAR ADCs in this tutorial, so we will only give a few highlights of modern breakthrough products.
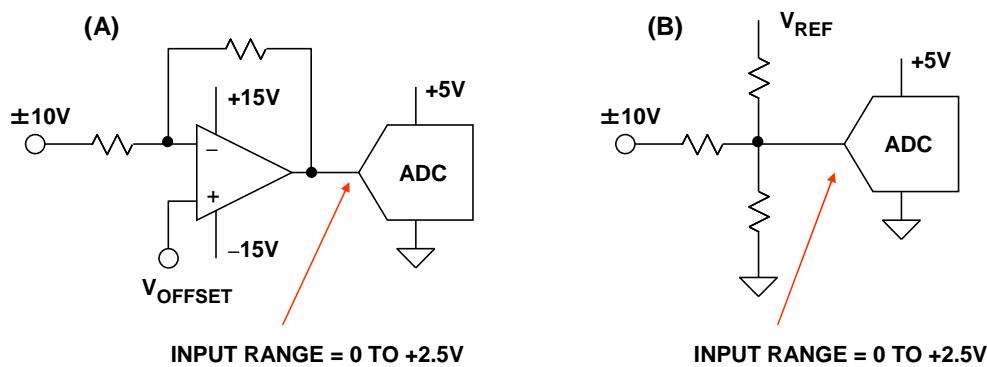
An example of modern charge redistribution successive approximation ADCs is Analog Devices' PulSAR® series. The [AD7641](#) is a 18-bit, 2-MSPS, fully differential, ADC that operates from a single 2.5 V power supply (see Figure 9). The part contains a high-speed 18-bit sampling ADC, an internal conversion clock, error correction circuits, internal reference, and both serial and parallel system interface ports. The AD7641 is hardware factory calibrated and comprehensively tested to ensure such ac parameters as signal-to-noise ratio (SNR) and total harmonic distortion (THD), in addition to the more traditional dc parameters of gain, offset, and linearity.

Figure 9: AD7641 18-Bit 2-MSPS Switched Capacitor PulSAR® ADC
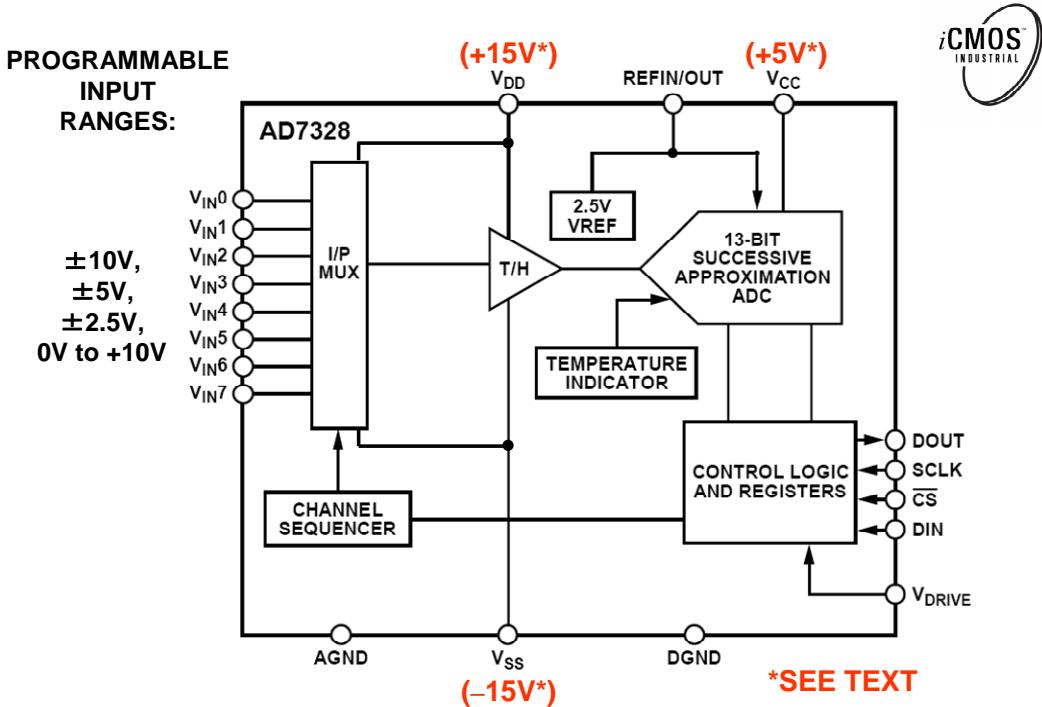
PROCESSING INDUSTRIAL-LEVEL SIGNALS

Many low voltage single-supply SAR ADCs have been introduced over the last few years, however their input range is usually limited to less than or equal to the supply voltage. In many situations this is not a problem; but there still exist many industrial applications which require digitization of bipolar signals (for example, ±5 V or ±10 V). This requires external circuitry when interfacing to single-supply ADCs. Figure 10 shows two possible approaches. An external op amp can be used to perform the level shifting and attenuation required to match the ±10 V signal to the 0 to +2.5 V input range of the ADC (Figure 10A). An alternative is to utilize a resistor network to perform the attenuation and level shifting (Figure 10B). Both methods require external components.

Figure 10: Interfacing Industrial-Level Bipolar Signals to Low-Voltage ADCs

A much better solution available from Analog Devices uses a proprietary industrial CMOS (*i*CMOS™) process which allows the input circuitry to operate on standard industrial ± 15 V supplies, while operating the ADC core on the low voltage supply (5 V or less). Figure 11 shows the AD7328 13-bit 8-channel input ADC.

Figure 11: AD7328 13-Bit, 1MSPS iCMOS™ ADC with True Bipolar Inputs

The AD7328 is designed on the *i*CMOS (industrial CMOS) process. *i*CMOS is a process combining high voltage CMOS and low voltage CMOS. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts could achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can accept bipolar input signals while providing increased performance, dramatically reducing power consumption, and having a reduced package size. The AD7328 can accept true bipolar analog input signals. The AD7328 has four software-selectable input ranges, ±10 V, ±5 V, ±2.5 V, and 0 V to 10 V. Each analog input channel can be independently programmed to one of the four input ranges. The analog input channels on the AD7328 can be programmed to be single-ended, true differential, or pseudo differential. The ADC contains a 2.5 V internal reference. The AD7328 also allows for external reference operation. If a 3 V external reference is applied to the REFIN/OUT pin, the AD7328 can accept a true bipolar ±12 V analog input. Minimum ±12 V V_{DD} and V_{SS} supplies are required for the ±12 V input range.

The low voltage core of the AD7328 operates on the V_{CC} supply which should be 5 V nominal (4.75 V to 5.5 V) for specified performance. For V_{CC} between 2.7 V and 4.75 V, the AD7328 will meet its typical specifications. The AD7328 has a separate V_{DRIVE} pin which sets the I/O logic interface voltage (2.7 V to 5.5 V). The V_{DRIVE} voltage should not exceed V_{CC} by more than 0.3 V.

The AD7328 has a high speed serial interface that can operate at throughput rates up to 1 MSPS.

SUMMARY

The SAR ADC architecture is elegant, efficient, easy to understand, and ideally suited to modern fine-line CMOS processes. The lack of "pipeline" delay (or latency) makes it ideal for single-shot and multiplexed data acquisition applications. CMOS processes allows the addition of a variety of digital functions, such as automatic channel sequencing, auto-calibration, etc. In addition, many SAR ADCs have on-chip temperature sensors and voltage references. Although the SAR ADC had its origins in mathematical puzzles of the 1500s, it is still the converter of choice for modern multichannel data acquisition systems.

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2. John C. Schelleng, "Code Modulation Communication System," *U.S. Patent 2,453,461*, filed June 19, 1946, issued November 9, 1948. *(an interesting description of a rather cumbersome successive approximation ADC based on vacuum tube technology. This converter was not very practical, but did illustrate the concept. Also in the patent is a description of a corresponding binary DAC).*

3. W. M. Goodall, "Telephony by Pulse Code Modulation," *Bell System Technical Journal*, Vol. 26, pp. 395-409, July 1947. *(describes an experimental PCM system using a 5-bit, 8KSPS successive approximation ADC based on the subtraction of binary weighted charges from a capacitor to implement the internal subtraction/DAC function. It required 5 internal reference voltages).*

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5. B. D. Smith, "Coding by Feedback Methods," *Proceedings of the I. R. E.*, Vol. 41, August 1953, pp. 1053-1058. *(Smith uses an internal DAC and also points out that a non-linear transfer function can be achieved by using a DAC with non-uniform bit weights, a technique which is widely used in today's voiceband ADCs with built-in companding).*

6. L.A. Meacham and E. Peterson, "An Experimental Multichannel Pulse Code Modulation System of Toll Quality," *Bell System Technical Journal*, Vol. 27, No. 1, January 1948, pp. 1-43. *(describes non-linear diode-based compressors and expanders for generating a non-linear ADC/DAC transfer function).*

7. Bernard M. Gordon and Robert P. Talambiras, "Signal Conversion Apparatus," *U.S. Patent 3,108,266*, filed July 22, 1955, issued October 22, 1963. *(classic patent describing Gordon's 11-bit, 20kSPS vacuum tube successive approximation ADC done at Epsco. The internal DAC represents the first known use of equal currents switched into an R/2R ladder network.)*

8. Bernard M. Gordon and Evan T. Colton, "Signal Conversion Apparatus," *U.S. Patent 2,997,704*, filed February 24, 1958, issued August 22, 1961. *(classic patent describes the logic to perform the successive approximation algorithm in a SAR ADC).*

9. Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN 0-916550-27-3, Chapter 1 and 3. Also available as *The Data Conversion Handbook,* Elsevier/Newnes, 2005, ISBN 0-7506-7841-0, Chapter 1 and 3.