The StrongArm Latch

ELEC 5705

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1 Objective

The objective of this assignment is to design and evaluate a clocked StrongARM latch comparator for use in a 5-bit asynchronous successive-approximation-register (SAR) ADC operating at 500 MS/s with a 450 mV dynamic input range. The comparator must reliably resolve differential input signals on the order of 0.5 LSB while satisfying the stringent timing requirements imposed by high-speed SAR conversion.

To achieve this, device-level characterization was first performed using gm/Id methodology to determine suitable operating regions and transistor sizing for high transconductance and fast regeneration. A classical StrongARM latch topology was then implemented using the derived sizing parameters and simulated in Cadence using the gpdk045 process with a 1 V supply.

2 Comparator Specifications

The Target ADC will be a 5-bit async SAR ADC, 500 MS/s, with a 450mV dynamic range (full scale), using a V_{DD} of 1V.

The required resolution is thus:

$$LSB = \frac{DynamicRange}{2^5}$$
$$= \frac{450mV}{2^5} \approx 14mV$$

The comparator must resolve at least 0.5LSB or 7mV; which will be used as the minimum differential input.

The timing required is thus:

$$t_{ideal} = \frac{T_s}{5}$$
$$\frac{2ns}{5} = 400ps$$

However accounting for CDAC and practicallities, t_{ideal} is reduced to $\approx 200 - 300$ ps.

Decision time is measured from the clock enabling evaluation (e.g. CLK @ 50%) to a digital-valid output level (e.g. output crossing $0.5\mathrm{V}_{DD}$).

3 Transistor Characterization

Device characterization was performed using minimum channel length devices ($L = 45\,\mathrm{nm}$) with an initial width of $W = 1\,\mu\mathrm{m}$. The objective was to identify an operating region providing high transconductance for rapid regenerative action while maintaining proper saturation.

Figure 1 shows the extracted device characteristics. An I_D–V_{GS} sweep was first performed with $V_{DS} = 1\,\mathrm{V}$ to evaluate transconductance and operating region. As shown in Fig. 1a, biasing near $V_{GS} \approx 0.7\,\mathrm{V}$ yields strong conduction with approximately

$$I_D \approx 70\,\mu\mathrm{A}, \qquad g_m \approx 640\,\mu\mathrm{S},$$

corresponding to

$$\frac{g_m}{I_D} \approx 9\,\mathrm{V}^{-1},$$

which places the device in moderate-to-strong inversion, suitable for high-speed regenerative comparator operation.

To verify saturation and evaluate intrinsic gain, a V_{DS} sweep was performed at fixed $V_{GS} = 0.7\,\mathrm{V}$, shown in Fig. 1b. At $V_{DS} = 1\,\mathrm{V}$, the device exhibits

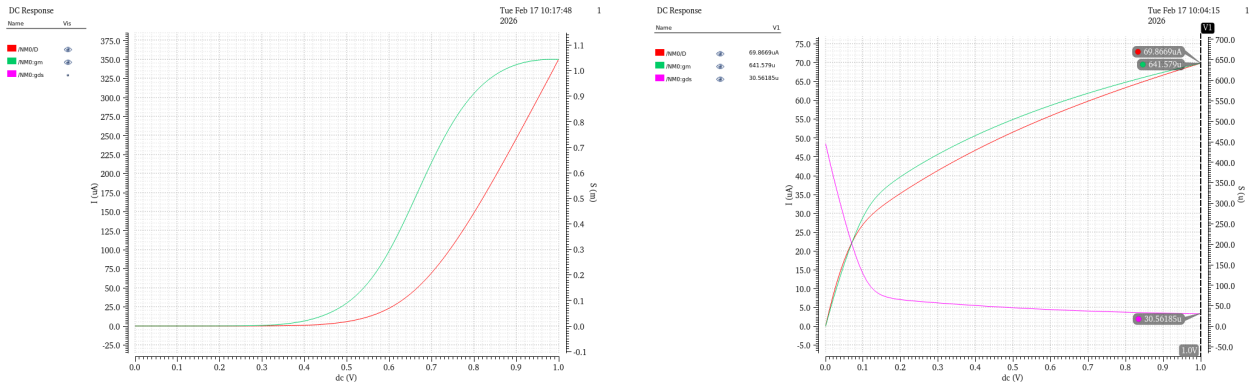
$$g_{ds} \approx 30\,\mu\mathrm{S}, \qquad r_o \approx 33\,\mathrm{k}\Omega,$$

yielding an intrinsic gain of approximately

$$A_{int} = \frac{g_m}{g_{ds}} \approx 20.$$

These results confirm proper saturation and sufficient transconductance for rapid expo-

nential regeneration in the StrongARM latch. The characterized operating point therefore served as the basis for subsequent comparator transistor sizing.



(a) g_m, I_D vs V_{GS} (b) g_m, I_D and g_{ds} vs V_{DS}

Figure 1: g_m/I_D characterization used for transistor operating region analysis.

Based on the characterized operating point, all comparator transistors were implemented using minimum channel length devices ($L = 45\,\text{nm}$) to maximize speed and reduce parasitic capacitance.

To achieve sufficient transconductance for rapid regenerative operation, the device width was increased from the characterization value to

$$W = 8\,\mu\text{m}.$$

Since transconductance scales approximately linearly with device width,

$$g_m \propto W,$$

this sizing provides a substantial increase in regeneration strength while maintaining the desired inversion region identified during characterization. Symmetric sizing was used across the latch to preserve matching and minimize systematic offset, while the increased width ensures adequate current drive for sub-nanosecond decision times required by the SAR conversion rate.

4 StrongARM Latch Simulation

A classical StrongARM latch topology was implemented using the previously characterized transistor sizing ($L = 45\,\text{nm}$, $W = 8\,\mu\text{m}$). The comparator consists of a differential NMOS input pair, a clocked tail current device, cross-coupled regenerative devices, and PMOS precharge transistors enabling dynamic reset and evaluation operation, as shown below in Figure 2.

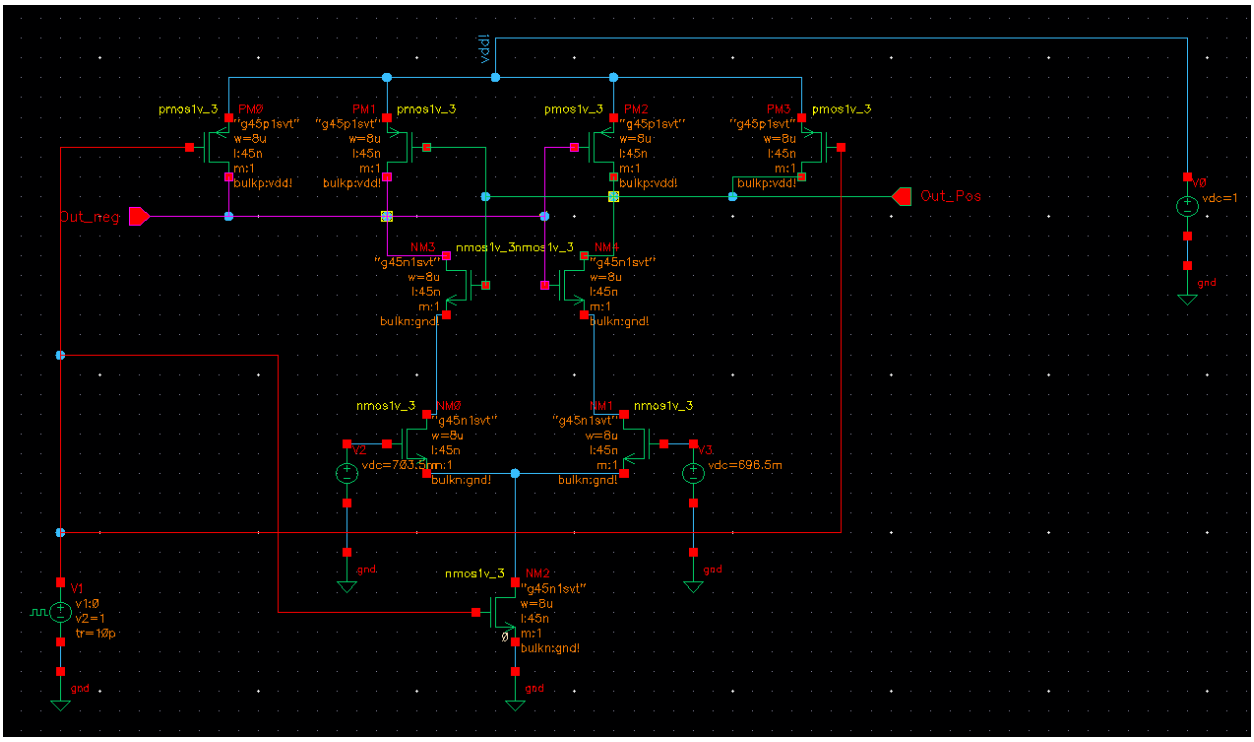


Figure 2: Strong Arm Latch Topology

The circuit was simulated using a 1 V supply. A rail-to-rail clock was applied using a pulse source with amplitude 0–1 V, 10 ps rise/fall time, and 2 ns period corresponding to the 500 MS/s sampling rate. During the reset phase (CLK low), the PMOS precharge devices equalize the output nodes near V_{DD}. When the clock transitions high, the tail transistor activates, allowing the differential pair to discharge the internal nodes and initiate regenerative amplification.

To evaluate comparator sensitivity at the minimum required resolution, a differential

input corresponding to 0.5 LSB was applied. With $\Delta V = 7\,\text{mV}$,

$$V_{in+} = 0.7035\ \text{V}, \qquad V_{in-} = 0.6965\ \text{V}.$$

The resulting transient response is shown in Fig. 3. During the reset phase, both outputs are precharged to approximately V_{DD}. Upon the rising clock edge, both nodes initially experience a small discharge due to charge redistribution and differential pair conduction. The branch receiving the larger input voltage discharges more slowly, after which the cross-coupled regenerative network amplifies the small voltage imbalance exponentially. This positive feedback drives one output rapidly toward ground while the opposite node is restored toward V_{DD}, producing a full rail-to-rail decision.

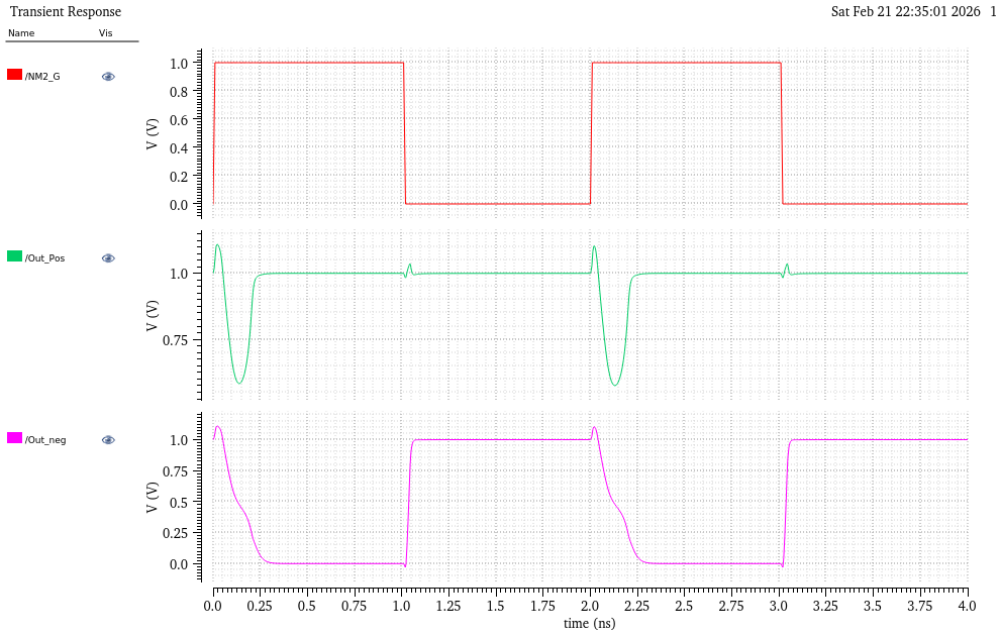


Figure 3: Caption

The comparator decision time was measured as the interval between the clock rising transition and the moment the losing output crosses $0.5\,V_{DD}$. For the applied 0.5 LSB input, the measured decision time was approximately 124 ps, satisfying the $\sim$ 200–300 ps timing budget required for the 500 MS/s SAR conversion.

These results confirm correct dynamic operation of the StrongARM latch and demon-

strate that the comparator can reliably resolve differential inputs at the minimum required resolution within the available decision time.