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<u>EXPERIMENT-4</u> <u>Title: Studies on Small Signal CE Amplifier</u>

Objective

- Explain structure of Bipolar Junction Transistor
- Explain Operation of Bipolar Junction Transistor
- Explain Common Emitter characteristics of a BJT

Apparatus

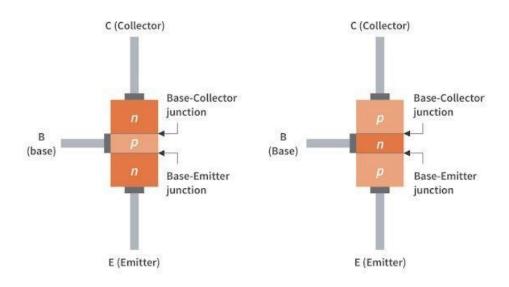
S. No.	Apparatus	Range	Туре	Quantity
1	Resistance	1Ω-100Ω	-	2
2	Voltmeter	0-2V 0-10V 0-40V	MC MC MC	1 1 1
3	Ammeter	0-100μA 0-40μA 0-4μA	MC MC MC	1 1 1
4	Voltage Source	-	DC	2
5	BJT		NPN	1

Theory

Structure

Bipolar Junction Transistors contain three doped extrinsic semiconductor regions each connected to a circuit. The transistor is not symmetrical due to the different doping ratios of the emitter, collector and base regions. The base region consists of lightly doped materials that exhibit high resistivity. The base is located between the heavily doped emitter region and the lightly doped collector region. The collector engulfs the emitter region which eliminates the ability for electrons injected into the base region to escape the base region without being collected. The emitter region is heavily doped to increase the current gain of the transistor.

For high current gain, a high ratio of carriers injected by the emitter to those injected by the base is needed. Increasing the emitter injection efficiency results in the majority of the carriers injected into the emitter-base junction coming from the emitter region. The high doping ratio of the emitter and collector regions, also means the collector-base junction is reverse biased. The collector-base junction can therefore have a high magnitude reverse bias voltage applied before the junction breaks down. For the transistor as a whole, the fundamental difference between the NPN Transistor and the PNP Transistor is current directions and voltage polarities of the transistor junctions.



NPN and PNP BJT Physical Representation

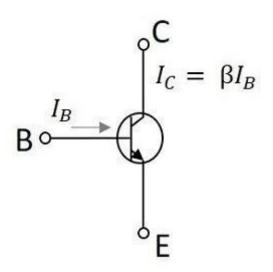
The supply of suitable external dc voltage is called biasing. Either forward or reverse biasing is done to the emitter and collector junctions of the transistor. These biasing methods make the transistor circuit work in four kinds of regions such as Active region, Saturation region, Cutoff region and Inverse active region. This is understood by having a look at the below table.

Among these regions, the Inverse active region, which is just the inverse of active region, is not suitable for any applications and hence not used.

EMITTER JUNCTION	COLLECTOR JUNCTION	REGION OF OPERATION
Forward biased	Forward biased	Saturation region
Forward biased	Reverse biased	Active region
Reverse biased	Forward biased	Inverse active region
Reverse biased	Reverse biased	Cutoff region

Active region

This is the region in which transistors have many applications. This is also called a linear region. A transistor while in this region, acts better as an Amplifier.



This region lies between saturation and cutoff. The transistor operates in active region when the emitter junction is forward biased and collector junction is reverse biased. In the active state, collector current is β times the base current.

Saturation region

This is the region in which the transistor tends to behave as a closed switch. The transistor has the effect of its collector and Emitter being shorted. The collector and Emitter currents are maximum in this mode of operation.

The figure below shows a transistor working in a saturation region.

B o
$$I_C = I_E$$

Collector and emitter are shorted

The transistor operates in a saturation region when both the emitter and collector junctions are forward biased. As it is understood that, in the saturation region the transistor tends to behave as a closed

Cut-off Region

This is the region in which the transistor tends to behave as an open switch. The transistor has the effect of its collector and base being opened. The collector, emitter and base currents are all zero in this mode of operation.

The following figure shows a transistor working in the cutoff region.

$$\begin{array}{c} \mathsf{C} \\ \downarrow I_c = 0 \\ I_B = 0 \end{array} \begin{array}{c} \mathsf{C} \\ \downarrow I_c = 0 \\ & \text{Open between} \\ & \text{emitter and} \\ & \text{collector} \\ \downarrow I_E = 0 \\ \mathsf{E} \end{array}$$

The transistor operates in the cutoff region when both the emitter and collector junctions are reverse biased. As in the cutoff region, the collector current, emitter current and base currents are nil.

$$I_F = I_{ES} imes (exp^{rac{v_{BE}}{v_T}} - 1)$$

$$I_R = I_{CS} imes (exp^{rac{V_{CB}}{V_T}} - 1)$$

where.

 I_{ES} is base-emitter saturation currents, I_{CS} is base-collector saturation currents

$$V_T = rac{k imes T}{q}$$

where,

k is the Boltzmann's constant ($k=1.381\ e-23\ V.C/\ K$), T is the absolute temperature in degrees Kelvin, and q is the charge of an electron (q = 1.602 e-19 C).

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F}$$

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R}$$

where,

 eta_F is large signal forward current gain of common-emitter configuration, eta_R is the large signal reverse current gain of the common-emitter configuration

$$\alpha_F = \frac{\beta_F}{1 + \beta_F}$$

$$\alpha_R = \frac{\beta_R}{1 + \beta_R}$$

where,

 α_R is large signal reverse current gain of a common-base configuration, α_F is large signal forward current gain of the common-base configuration.

$$I_C = \alpha_F \times I_F - I_R$$

$$I_E = -I_F + \alpha_R * I_R$$

$$I_B = (1 - lpha_F) imes I_F + (1 - lpha_R) imes I_R$$

The forward and reverse current gains are related by the expression

$$\alpha_R \times I_{CS} = \alpha_F \times I_{ES} = I_S$$

where,

 I_S is the BJT transport saturation current.

The parameters $lpha_R$ and $lpha_F$ are influenced by impurity concentrations and junction depths.

The saturation current, I_S , can be expressed as

$$I_S = J_S \times A$$

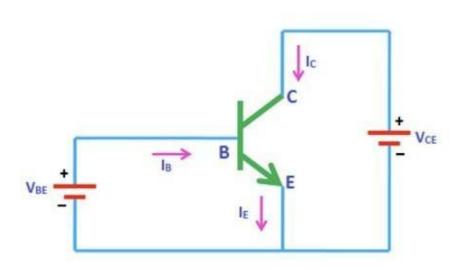
where,

A is the area of the emitter and

 J_S is the transport saturation current density

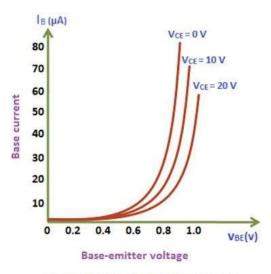
The DC behavior of the BJT can be described by the Ebers-Moll Model. The equations for the model are:

Input and Output Characteristics



The most important characteristic of the BJT is the plot of the base current, I_B , versus the base-emitter voltage, V_{BE} , for various values of the collector-emitter voltage, V_{CE}

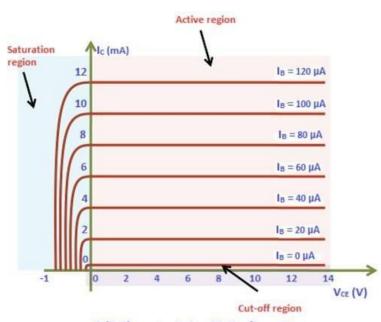
$$I_B = \Phi(V_{BE}, V_{CE})$$
 for constant V_{CE}



I/P characteristics CE configuration

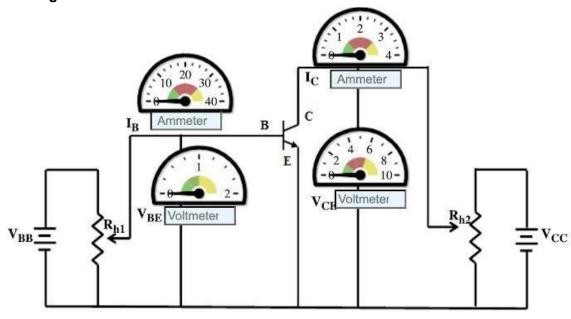
The most important characteristic of the BJT is the plot of the collector current, I_C , versus the collector-emitter voltage, V_{CE} , for various values of the base current, I_B as shown on the circuit.

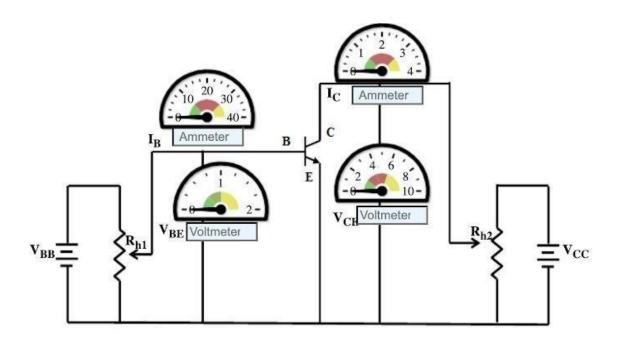
$$I_C = \Phi(V_{CE}, I_B)$$
 for constant I_B



O/P Characteristics CE Configuration

Circuit Diagram





Observations:

Input Characteristics

Table 1

Serial	Collector-Emitter Voltage(1 V)
--------	--------------------------------

Number	Base-Emitter Voltage (in V)	Base Current (µA)
1	0.02000	2.058
2	0.2000	2.661
3	0.4000	3.542
4	0.6000	4.713
5	0.8000	6.271
6	1.000	8.345
7	1.200	11.11
8	1.400	14.78
9	1.600	19.67
10	1.800	26.17
11	2.000	34.82

Table 2

Serial	Collector-Emitter Voltage(4 V)	
Number	Base-Emitter Voltage (in V)	Base Current(µA)
1	0.02000	2.058
2	0.2000	2.661
3	0.4000	3.542
4	0.6000	4.713
5	0.8000	6.271
6	1.000	8.345
7	1.200	11.11

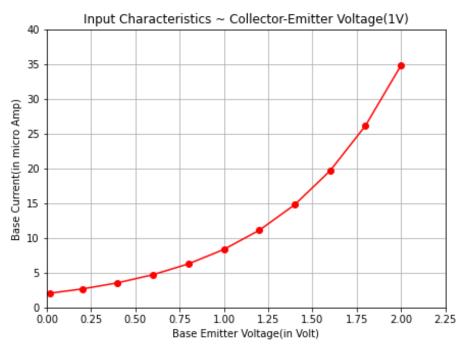
8	1.400	14.78
9	1.600	19.67
10	1.800	26.17
11	2.000	34.82

Table 3

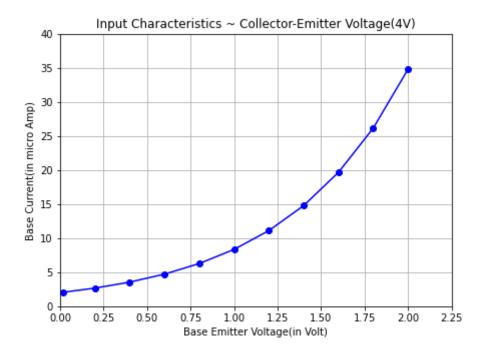
Serial	Collector-Emitter Voltage(8V)
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Number	Base-Emitter Voltage (in V)	Base Current(µA)
1	0.02000	2.058
2	0.2000	2.661
3	0.4000	3.542
4	0.6000	4.713
5	0.8000	6.271
6	1.000	8.345
7	1.200	11.11
8	1.400	14.78
9	1.600	19.67
10	1.800	26.17
11	2.000	34.82

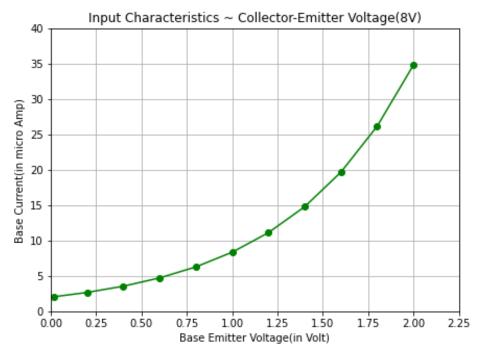
Graphs Graph for Table-1



Graph for Table-2



Graph for Table-3



<u>Output</u>

Characteristics

Table-4

Serial	Base-Current(15.35 μA)	
Number	Collector-Emitter Voltage(V)	Collector Current (mA)
1	0.1000	5.994
2	0.2000	11.87
3	0.4000	22.85
4	0.5000	27.79
5	0.8000	39.94
3	1.000	45.81
4	1.200	50.14
5	1.700	56.26
6	1.500	54.44
7	2.000	57.98

8	2.500	59.34
9	3.000	59.85
10	4.000	60.10
11	5.000	60.14
12	6.000	60.14
13	7.000	60.14

Table-5

Serial Base-Current(41.73 μA)	
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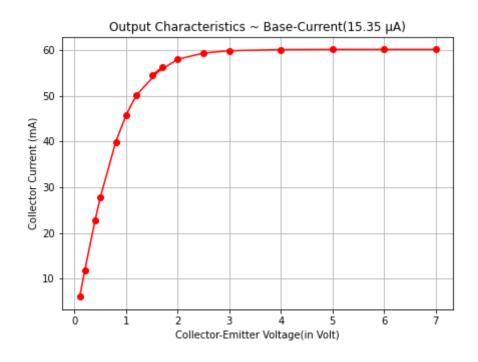
Number	Collector-Emitter Voltage(V)	Collector Current (mA)
1	0.1000	26.86
2	0.2000	53.20
3	0.4000	102.4
4	0.5000	124.6
5	0.7000	162.9
6	0.9000	193.1
7	1.000	205.3
8	1.200	224.7
9	1.500	244.0
10	1.700	252.1
11	2.000	259.8
12	2.500	265.9
13	3.000	268.2
14	4.000	269.4
15	5.000	269.5
16	6.000	269.5

Table-6

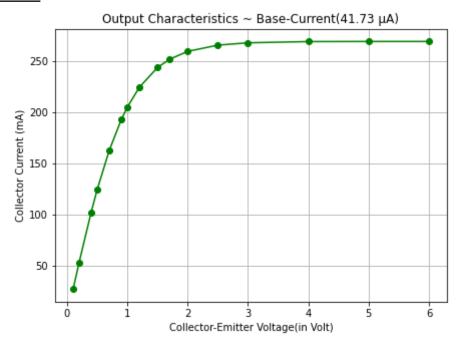
Serial	Base-Current(81.42 μA)

Number	Collector-Emitter Voltage(V)	Collector Current (mA)
1	0.1000	78.43
2	0.2000	155.3
3	0.3000	229.2
4	0.5000	363.7
5	0.7000	475.6
6	1.000	599.3
7	1.300	678.1
8	1.500	712.3
9	1.800	745.1
10	2.000	758.6
11	2.500	776.4
12	3.000	783.1
13	4.000	786.4
14	5.000	786.9
15	6.000	786.9
16	7.000	786.9

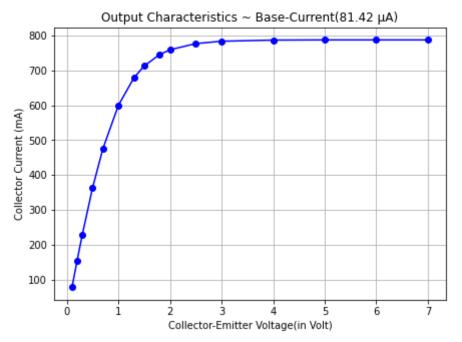
Graphs Graph for Table-4

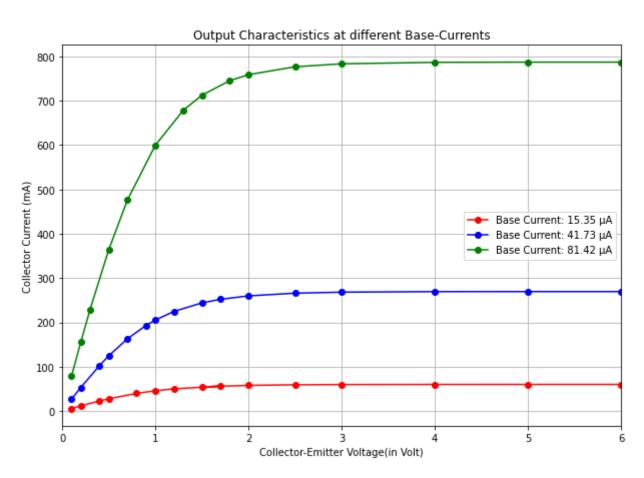


Graph for Table-5



Graph for Table-6





Discussion:

• <u>CE configuration:</u> Transistor is said to be in common emitter configuration if the emitter of the transistor is common between input and output terminal.

Input characteristic:

The curve plotted between base current I_b and the base-emitter voltage V_{BE} is called Input characteristics curve.

The curve for common base configuration is similar to a forward diode characteristic. The base current $\rm I_b$ increases with the increases in the emitter-base voltage $\rm V_{BE}$.

The effect of CE voltage does not cause the large divergence on the I_b - V_{BE} curves, and hence the effect of a change in V_{CE} (collector emitter voltage) on the input characteristic can be ignored.

Output Characteristics:

In the active region, the collector current increases slightly as collector-emitter V. CE current increases. The slope of the curve is quite more than the output characteristic of CB configuration. The output resistance of the common base connection is more than that of CE connection.

The value of the collector current I_C increases with the increase in V_{CE} at constant voltage I_b , the value β of also increases. When the V_{CE} falls, the I_C also decreases rapidly. The collector-base junction of the transistor is always in forward bias and saturates. In the saturation region, the collector current becomes independent and free from the input current I_B . In the active region $I_C = \beta I_B$, a small current I_C is not zero, and it is equal to reverse leakage current I_{CEO} .

Conclusion:

- For input characteristics of BJT CE, keeping the collector- emitter (V_{CE}) voltage constant, the base- emitter (V_{BE}) voltage is increased from 0 and the corresponding base current (I_b) values are noted. This is repeated for increasing values of V_{CE}. The family of curves obtained by plotting I_b against V_{BE} for each V_{CE} value is called input characteristics. With increase in V_{CE} the graph also shifts upward.
- For output characteristics,keeping the base current (I_B) constant, collector- emitter (V_{CE}) voltage is varied and the corresponding Ic values are obtained. This is repeated for increasing values of I_B . The family of curves obtained by plotting I_C against V_{CE} for each value of I_B is called output characteristics. With increase in IB the graph also shifts upward. The curve starts from origin goes to saturation region on increase of V_{CE} , on further increase in V_{CE} we see no further change in the characteristics(i.e I remains constant with increase in V_{CE}), implies we are in the forward active region , and if V_{CE} is further increase , we see breakdown region.
- Thus, we can clearly see that transistor is a non-linear device from the curve.

CE Amplifier

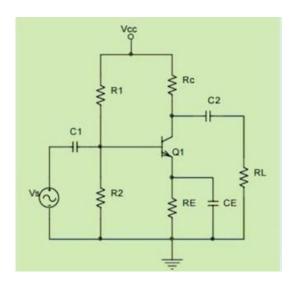
Objective

To investigate the operation of a common-emitter NPN transistor amplifier.

Apparatus

S. No.	Apparatus	Range	Туре	Quantity
1	Resistor	i) 100Ω -1000Ω ii)100Ω - 4000Ω iii)100Ω-47kΩ iv)100Ω-15kΩ	-	1 2 1 1
2	Voltage Source	50Hz-50MHz	i)AC ii)DC	1
3	Capacitor	1μF-10μF	-	3
4	BJT	-	NPN	1

Theory



The common emitter configuration is widely used as a basic amplifier as it has both voltage and current amplification.

Resistors $R_{\rm B1}$ and $R_{\rm B2}$ form a voltage divider across the base of the transistor. The function of this network is to provide necessary bias conditions and ensure that the emitter-base junction is operating in the proper region.

In order to operate a transistor as an amplifier, biasing is done in such a way that the operating point is in the active region. For an amplifier the Q-point is placed so that the load line is bisected. Therefore, in practical design V_{CE} is always set to $\frac{V_{cc}}{2}$. This will confirm that the Q-point always swings within the active region. This limitation can be explained by maximum signal handling capacity. For the maximum input signal, output is produced without any distortion and clipping.

Input Capacitor (C₁)

The capacitor C_1 is used to couple the signal to the base terminal of the BJT. If it is not there, the signal source resistance, R_s will come across R_2 and hence, it will change the bias. C_1 allows only the AC signal to flow but isolates the signal source from R_2

Emitter Bypass Capacitor (CE)

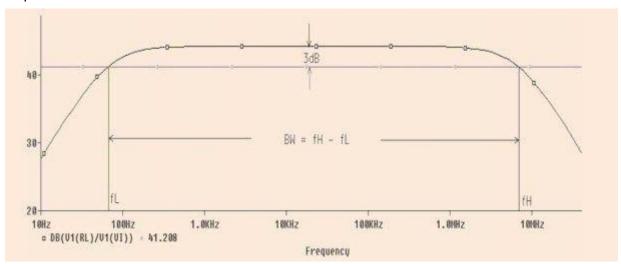
An Emitter bypass capacitor CE is used parallel with $R_{\rm E}$ to provide a low reactance path to the amplified AC signal. If it is not used, then the amplified AC signal following through $R_{\rm E}$ will cause a voltage drop across it, thereby dropping the output voltage.

Coupling Capacitor (C₂)

The coupling capacitor C_2 couples one stage of amplification to the next stage. This technique is used to isolate the DC bias settings of the two coupled circuits.

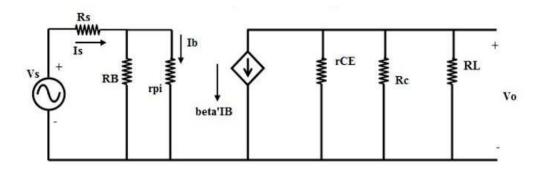
CE Amplifier Frequency Response

The voltage gain of a CE amplifier varies with signal frequency. It is because reactances of the capacitors in the circuit changes with signal frequency and hence affects the output voltage. The curve drawn between voltage gain and the signal frequency of an amplifier is known as frequency response. Below figure shows the frequency response of a typical CE amplifier.



Frequency Response of Common Emitter Amplifier

The midband gain is obtained by short circuiting all the external capacitors and open circuiting the internal capacitors. Figure 2 shows the equivalent for calculating the midband gain.



$$A_{m} = \frac{V_{o}}{V_{s}} = -\beta[r_{CE}||R_{C}||R_{L}][\frac{R_{B}}{R_{B} + r_{pi}}][\frac{1}{R_{S} + (R_{B}||r_{pi})}]$$

It can be shown that the low frequency poles, w_{L1} , w_{L2} , w_{L3} can be obtained by the following equations:

$$\tau_1 = \frac{1}{w_{L1}} = C_{C1} \times R_{IN}$$

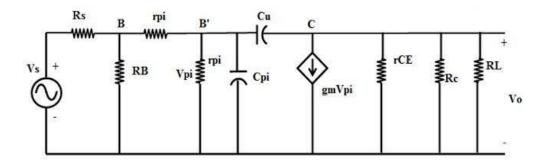
where,

$$egin{aligned} R_{IN} &= R_S + [R_B || r_{pi}] \ & au_2 = rac{1}{w_{L2}} = C_{C2} imes [R_L + (R_C || r_{CE})] \ & au_3 = rac{1}{w_{L3}} = C_E imes R_E' \ & R_E' = R_E || [rac{r_{pi}}{eta_F + 1} + (rac{R_B || R_S}{eta_F + 1})] \ & w_Z = rac{1}{R_E imes C_E} \end{aligned}$$

Normally, $w_Z < w_{L3}$ and the low frequency cut-off w_L is larger than the largest pole frequency. The low frequency cut-off can be approximated as

$$w_L \cong \sqrt{(w_{L1})^2 + (w_{L2})^2 + (w_{L3})^2}$$

The high frequency equivalent circuit of the common-emitter amplifier is shown in Figure 3.

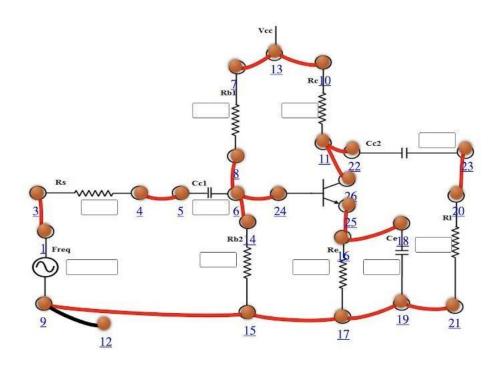


 C_{μ} is the collector base capacitance, C_{pi} is the emitter to base capacitance, r_x is the resistance of material of the base region between the base terminal B and an internal or intrinsic base terminal B'. Using Miler Theorem, it can be shown that 3-dB frequency at high frequencies is

$$w_H^{-1} = C_r \times (r_{pi} || [r_x + (R_B || R_S)])$$

where
$$C_T = C_{\pi} + C_u[1 + g_m(R_L||R_C)]$$
 and $g_m = \frac{I_C}{V_T}$

Circuit Diagram



Serial No.	Frequency(Hz)	Magnitude(dB)
1	80	4.77432
2	96	6.43712
3	183	12.1336
4	318	16.92652
5	727	23.917
6	1386	28.8692
7	2197	31.7644
8	4186	34.393

9	8746	35.606
10	20036	35.9562
11	26413	35.9928
12	38179	36.0186
13	79766	36.0352
14	105153	36.0358
15	138618	36.034
16	200364	36.0272
17	264131	36.0166
18	381786	35.9884
19	727478	35.8484
20	1051530	35.646
21	2003640	34.7474
22	4590080	31.5338
23	9590030	26.5178
24	45900800	13.4081

Source Resistance(R_S)=100 Ω

Collector Resistance(R_c)=500 Ω

Emitter Resistance(R_E)= 1000 Ω

Load Resistance(R_L)=2000 Ω

Base Resistance(R_{B1})= 5000 Ω

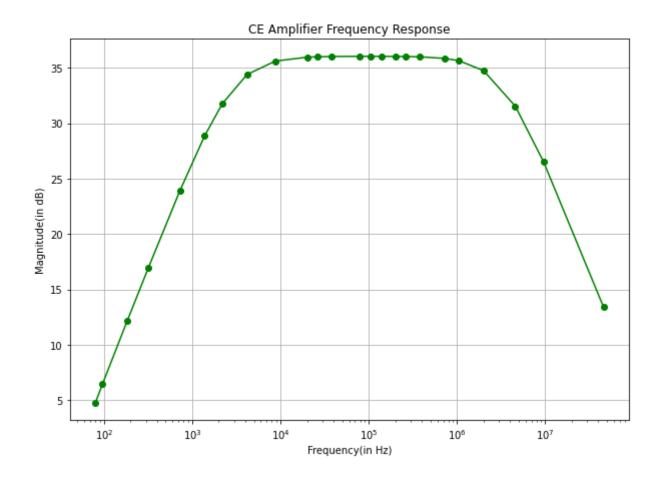
Base Resistance(R_{B2})= 5000 Ω

Coupling Capacitor(C_{C1})=10 μ F

Coupling Capacitor(C_{C2})=10 μF

Bypass Capacitance(C_E)=10 μF

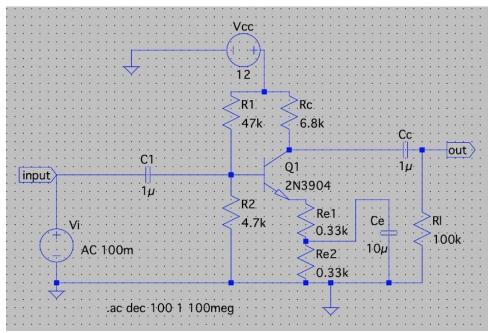
Graphs



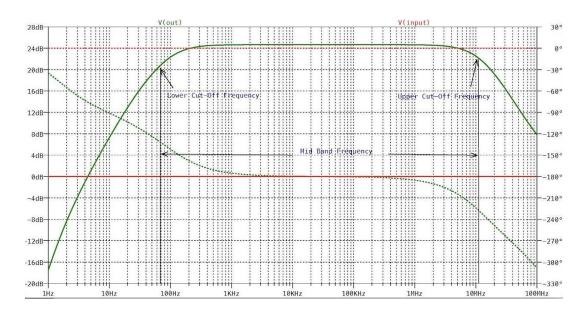
Midband gain = -63.41 Hz Low frequency cut-off = 17882.65323 Hz High frequency cut-off= 2.13515e⁺⁷ Hz

1) Frequency Response

a) Load Resistance is Connected



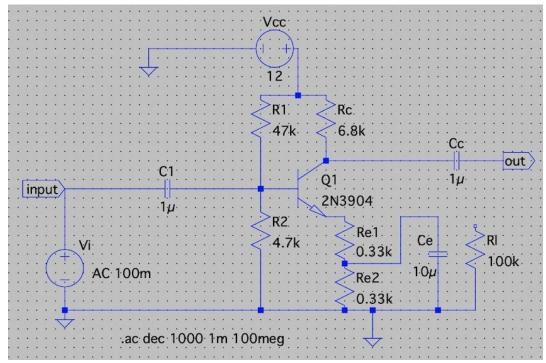
Circuit Diagram of CE Amplifier for Frequency Response



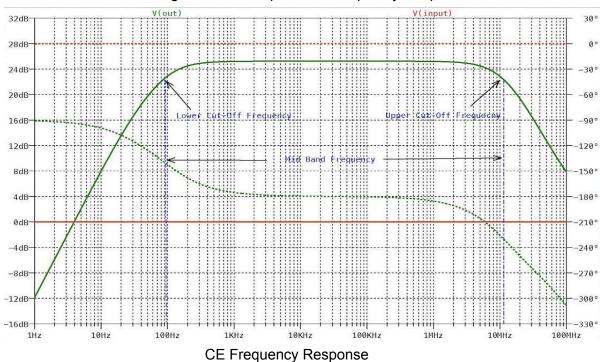
CE Frequency Response

Low frequency cut-off = 64.874Hz High frequency cut-off= 10.841 MHz

b) Load Resistance is not connected



Circuit Diagram of CE Amplifier for Frequency Response

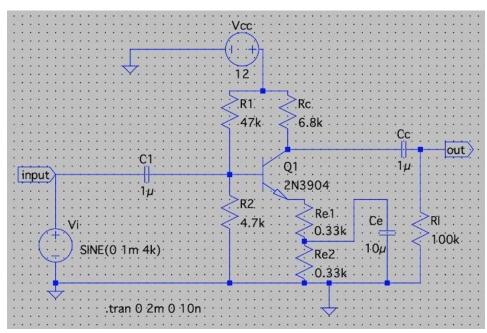


Low frequency cut-off = 90.331Hz

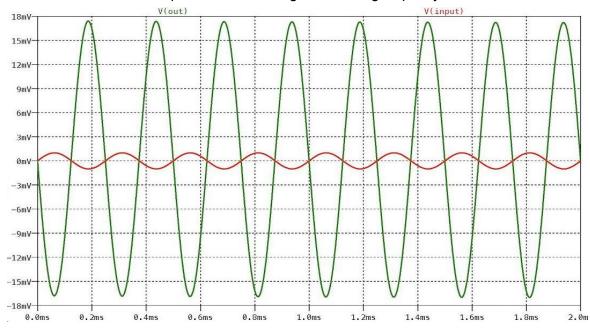
High frequency cut-off= 11.415 MHz

2) Signal Handling Capacity

a) Load Resistance is connected



CE Amplifier Circuit for Signal Handling Capacity



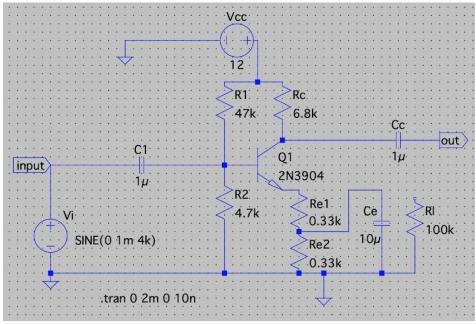
CE Amplifier
$$\frac{V_{out}}{V_{in}}$$
 in Time Domain

$$V_{in} = 1 \text{ mV}$$

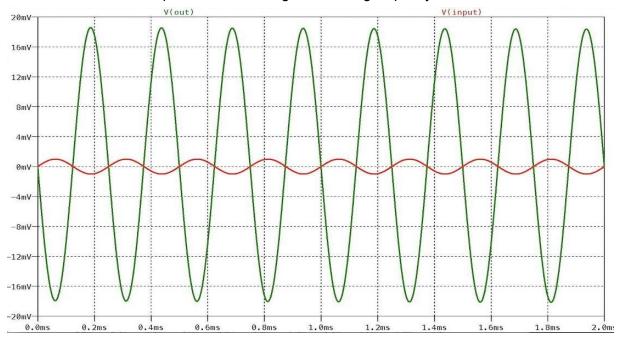
Gain =
$$\frac{V_{out}}{V_{in}} = \frac{17.5}{1} = 17.5$$

$$V_{sm}$$
 = 300 mV

b) Load Resistance isn't connected



CE Amplifier Circuit for Signal Handling Capacity



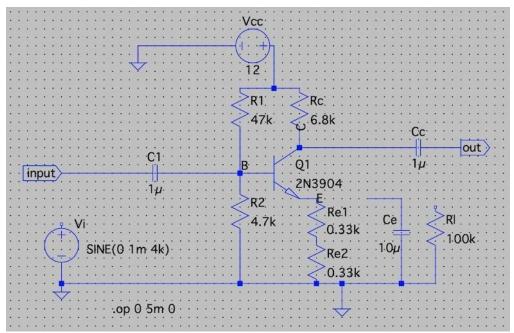
CE Amplifier $\frac{V_{out}}{V_{in}}$ in Time Domain

$$V_{in} = 1 \text{ mV}$$

Gain =
$$\frac{V_{out}}{V_{in}} = \frac{18.5}{1} = 18.5$$

$$V_{sm}$$
 = 300 mV

3) DC Analysis



Circuit Diagram for DC Analysis

Model of BJT being used - 2N3904

 $V_b = 1.08202 V$

 $V_{\rm C}$ = 7.49125 V

 $I_{\rm C}$ = 0.663051 mA

 $I_E = 0.665131 \text{ mA}$

Calculations:

Measurement of Input Resistance-

Here we have considered Vin = 1mV, f = 4kHz and the approximate Vsm = 300 mV.

We know that,
$$R_{in} = \frac{R_X - V_{out} I_{RX}}{V_{out} I_0 - V_{out} I_{RX}} - R_S$$

Where
$$R_x = 1k\Omega$$
, $V_{out}I_{Rx} = 14.91 \ mV$, $V_{out}I_{O} = 18.581 \ mV$

 $R_{_{\rm S}}~=~0$ as the voltage source is an ideal source.

$$R_{in} = \frac{1000 - (14.91 \times 10^{-3})}{(18.581 \times 10^{-3}) - (14.91 \times 10^{-3})} - 0 = 4050.53\Omega \simeq 4k\Omega$$

Measurement of Output Resistance-

Here we have considered Vin = 1mV, f = 4kHz and the approximate Vsm = 300 mV.

We know that,
$$R_{out} = R_L \times \frac{V_{out} I_{\infty} - V_{out} I_{R_L}}{V_{out} I_{R_L}}$$

Where
$$R_L = 100 \text{k}\Omega$$
, $V_{out} I_{\infty} = 18.58 \text{ mV}$, $V_{out} I_{R_L} = 17.4 \text{ mV}$

$$R_{out} = 100 \times 10^{3} \times \frac{(18.581 \times 10^{-3}) - (17.4 \times 10^{-3})}{17.4 \times 10^{-3}} = 6781.61\Omega \simeq 6.8k\Omega$$

Discussion:

At low frequencies (< FL) The reactance of coupling capacitor C_2 is relatively high and hence a very small part of the signal will pass from amplifier stage to the load. Moreover, CE cannot shunt the RE effectively because of its large reactance at low frequencies. These two factors cause a drop off of voltage gain at low frequencies. At high frequencies (> FH) The reactance of coupling capacitor C_2 is very small and it behaves as a short circuit. This increases the loading effect of the amplifier stage and serves to reduce the voltage gain.

Moreover, at high frequencies, the capacitive reactance of base-emitter junction is low which increases the base current. This frequency reduces the current amplification factor β. Due to these two reasons, the voltage gain drops off at high frequency.

At mid frequencies (FL to FH) The voltage gain of the amplifier is constant. The effect of the coupling capacitor C_2 in this frequency range is such as to maintain a constant voltage gain. Thus, as the frequency increases in this range, the reactance of CC decreases, which tends to increase the gain. However, we observe that the voltage gain drops off at low (< FL) and high (> FH) frequencies, whereas it is constant over the mid-frequency range (FL to FH).

Conclusion:

Conclusion from Above Curves:

- a) <u>Frequency Response</u>: The voltage gain drops off at low (< FL) and high (> FH) frequencies, whereas it is constant over the mid-frequency range (FL to FH). Also the gain incase of no load connected is more compared to when load is connected.
- b) <u>Signal Handling Capacity</u>: The output voltage is higher than the input voltage whether load is connected or not, thus input is amplified in both the cases. However on connecting the load resistance, the peak voltage decreases. We also observe a shift of 180^o
- c) <u>DC Analysis</u>: We see the stabilisation of the Q-point.Vcc is greater than Vce, thus the amplifier is biased in the active region.

In Common Emitter Amplifier, Input is applied to B-E Junction and Output is taken from E-C terminal, here the emitter terminal is common for both input and output.

It is a widely used amplifier circuit because it provides good current gain and good voltage gain and it is also known as an inverting amplifier because it gives 180° phase shift from input to output. It is widely used in audio amplification and signal amplification circuits. The current gain and voltage are moderate. However, in the CE amplifier, there is high thermal instability.