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Package Application Note for WLCSP Packages

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INTRODUCTION

This package application note provides the guidelines for the handling and assembly of Microchip WLCSP packages during the Printed Circuit Board (PCB) assembly. In addition, it provides general information for the PCB land pattern design and component rework guidelines.

SCOPE

This application note contains generic information for various Microchip WLCSP packages assembled internally or at external subcontractors. Specific information about each device is not provided. To develop a specific solution, actual experience and development efforts are required to optimize the assembly process and application design per individual device requirements, industry standards (such as IPC and JEDEC), and prevalent practices in the assembly environment. For more details about the specific devices contained in this document, visit www.microchip.com or contact your local Microchip sales office.

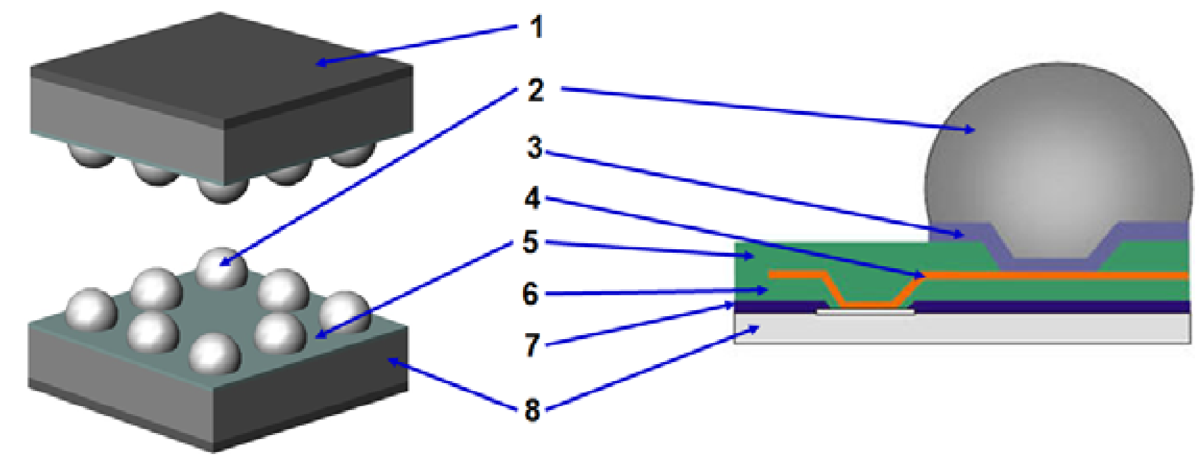
PACKAGE DESCRIPTION AND CONSTRUCTION

The WLCSP package is the only true chip-size package. The die itself is the package. Lead-free solder balls, usually Tin-Silver-Copper (SAC) material, are connected to the active side of the die, either directly to the die bond pads, or through the redistribution layer in fan-in configuration. The WLCSP part can then be mounted onto the customer's printed circuit board using standard surface mount assembly techniques. Microchip WLCSP products are offered in multiple pin-count configurations, and have the following features:

- Smallest package size, which is equal to the die size
- Smallest footprint per I/O count
- Thinner package profile with considerable weight reduction, due to the elimination of leadframe/substrate and molding compound
- No need for underfill material to be used
- Improved electrical performance, due to the elimination of wire bonds and package leads/traces
- Standard SMT performance characteristics

A typical WLCSP package construction (cross-section) and 3-D view are shown in Figure 1. These packages are assembled/constructed in a wafer level format through a standard wafer multi-mask process. Standard plated copper (Cu) or aluminum (Al) traces over the first re-passivation layer are used to make all necessary electrical connections between the die bond pads and each solder ball. The second re-passivation layer outlines the entire ball matrix, and each solder ball is attached to the RDL layer trough the Under-Bump-Metallization (UBM) layer. The WLCSP packages are processed in integrated assembly and test lines from wafer bumping through tape and reel.

FIGURE 1: WLCSP PACKAGE CONSTRUCTION



#	Description	#	Description
1	Backside Laminate (optional)	5	Re-passivation 2
2	SAC Solder Ball	6	Re-passivation 1
3	Under-Bump-Metallization (UBM) (Not used in thick RDL designs)	7	Die Passivation
4	Redistribution Layer (RDL) – Cu or Al	8	Silicon Die

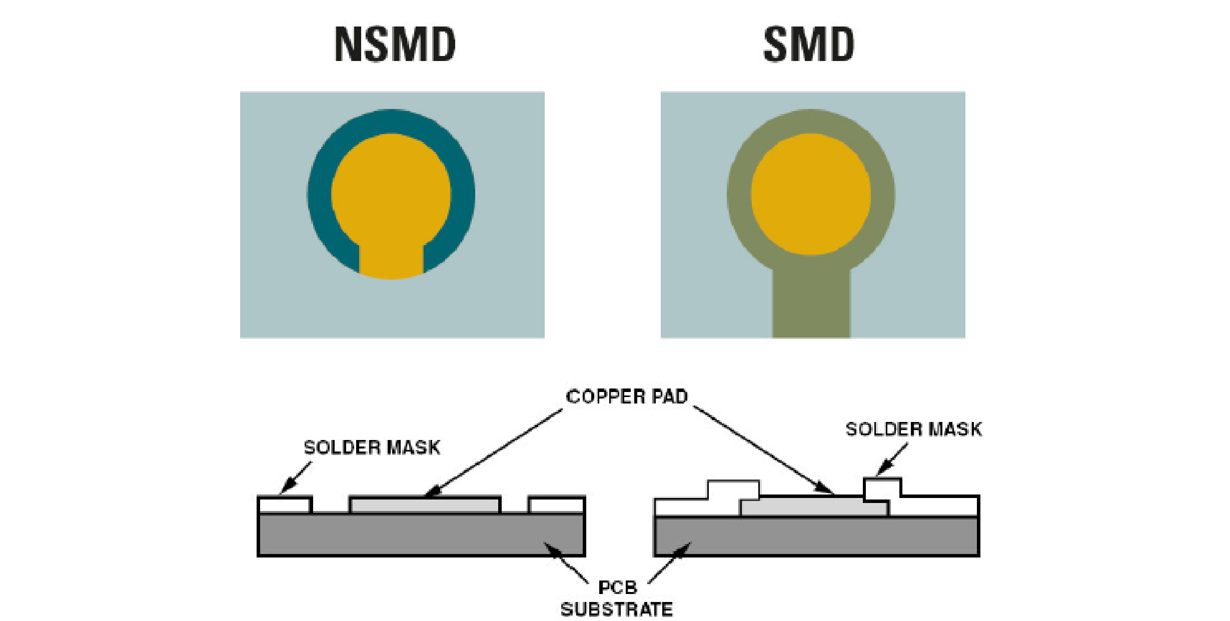
TYPICAL WLCSP CONFIGURATIONS AND DIMENSIONS

WLCSP products from Microchip come in various sizes with standard pitches of 0.4, 0.5 and 0.65 mm. The actual package outlines depend on the actual die sizes, which may or may not be the same as the more standardized packages. The actual package outlines are provided on the Microchip website as a separate document. To obtain the complete set of each WLCSP package dimensions and tolerances refer to the “Packaging Specification” (DS00000049) located on the Microchip website.

PCB LAND PATTERN GUIDELINES

The WLCSP is a surface-mountable package with bottom ball termination of its external connections. The land pattern design for all WLCSP type packages is based on IPC-7351 and IPC-7095 standards. A Non-Solder-Mask Defined (NSMD) pad design is recommended for all board pads, as shown in Figure 2.

FIGURE 2: NSMD AND SMD BOARD PAD DEFINITION



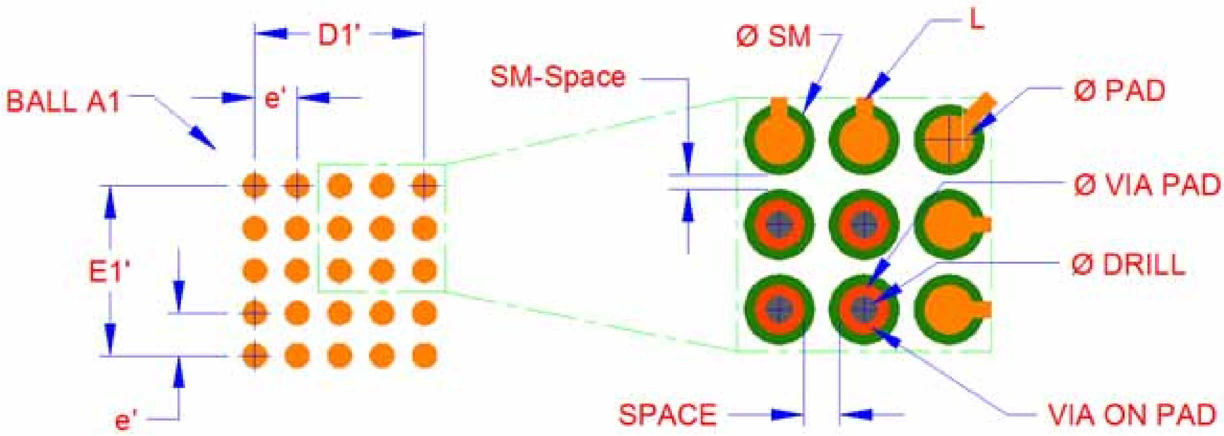
The NSMD board pad configuration provides a more robust solder joint than the SMD pads because the solder in the NSMD configuration wets the sides of the Cu pads, improving the strength of the solder joint between the WLCSP package and the PCB pads (see Figure 3). In the SMD pads, the edge of the solder mask can be a stress initiator at the base of the solder ball, which can result in solder joint cracking. NSMD requires the solder-wetted area of the pad to be determined by the defined Cu area, not by the solder mask. This is an advantage because of the tighter control on Cu etch process than the solder mask development operation. Furthermore, the smaller pad size in the NSMD design also provides more room for tight pitch routing on the PCB.

FIGURE 3: CROSS SECTION OF NSMD SOLDER JOINT

The size of the WLCSP part requires care in the PCB design process for optimum reliability, processing and performance. An example of typical land pattern information is shown in Figure 4. Additionally, the following rules should be observed when designing the PCB board:

- Best reliability results are achieved when the PCB laminate glass transition temperature is above the operating range of the intended application
- Ni/Au surface finishes are not recommended for Pb-free solder devices. Organic Solderability Preservative (OSP) surface finish will deliver superior reliability performance
- Cu traces routed away from the PCB land pads should be less than 100 um wide (preferably = 75 um) in the exposed area inside the solder mask opening (for NSMD pads). Wider trace widths will reduce part stand-off and impact reliability of the solder joints
- Trace routing away from the WLCSP device should be balanced in X and Y directions to avoid unintentional component movement as a result of unbalanced solder wetting forces
- No-clean solder paste Type 3 or 4 is recommended

FIGURE 4: TYPICAL WLCSP PCB LAND PATTERN



Symbol	Min	Nom	Max
D1'/E1'		1.600	
e'		0.400	
ØPAD	0.200	.0230	—
ØSM	0.300	0.330	—
Trace Width (L)	—	0.075	—
SPACE (Cu-to-Cu)	—	0.170	—
SM-Space	—	0.070	—
ØVIA PAD	0.200	0.230	—
ØDRILL	0.100	0.125	—

Note 1: To obtain the PCB land pattern guidelines and dimensions for each WLCSP package dimensions, refer to www.microchip.com/Packaging.

2: The information in this PCB land pattern should only be used as a guideline. Other factors, such as end-user layout and design, product specific application, and actual experience must be taken into consideration to define the final PCB land pattern for optimum component mounting process.

STENCIL DESIGN GUIDELINES

The stencil design should follow standard industry recommendations such as the IPC-7525 Stencil Design Guidelines. The best solder stencil performance is achieved using laser cut stencils with electro-polishing. The use of chemically etched stencils results in inferior solder paste volume control. The solder stencil opening should be identical for all solder pads in the WLCSP array. Square-shaped apertures are preferred over round apertures for better solder release, especially in thicker stencils. The corners of the square apertures may be rounded to minimize clogging. The apertures should be given a positive taper of about 5° with the bottom opening larger than the top to improve solder release. A 1:1 aperture to solder pad ratio is recommended. Suggested stencil design guidelines are shown in Table 1.

TABLE 1: SUGGESTED STENCIL DESIGN GUIDELINES

Pitch	0.4 mm	0.5 mm	0.65 mm
Nominal Ball Diameter (um)	250	300	350
PCB Solder Pad Diameter (um)	230	275	300
Stencil Opening (um)	230x230	275x275	300x300
Stencil Thickness (um)	100-125	100-125	125-150

REFLOW SOLDERING AND PROFILING

As with all SMT components, it is important that furnace profiles be monitored on all new board designs. In addition, if there are multiple package types on the board, the thermal profile should be measured at multiple locations. Component temperature may vary because of surrounding components, location of the device on the board, and package densities. To maximize the self-alignment effect of the WLCSP component, it is recommended that the maximum reflow temperature specified for the solder paste not be exceeded.

Microchip recommends that the user follows the guidelines of industry specifications IPC-7095 and J-STD-020 in developing the optimum reflow profile for the Pb-free WLCSP components with a given board.

HANDLING

The following information details handling procedures that should be used with WLCSP product packed in a Moisture Barrier Bag (MBB) and intended for surface mount applications. Following these handling guidelines will ensure that components maintain their as-shipped, dry state, alleviating package cracking and other moisture-related, stress-induced concerns that may be associated with the surface mount process.

1. Incoming Inspection

   Upon receipt, shipments should be inspected for bag integrity. There should not be holes, gouges, tears or punctures of any kind that expose either the contents or the inner layer of the bag.

2. Storage Conditions/Shelf Life

   When MSL-1 devices are stored according to JEDEC specification J-STD-033, the exposure time is unlimited.

3. Opening an MBB

   To open an MBB when the containers are ready to be used or inspected, simply cut across the top of the bag, being careful not to damage the enclosed materials. Once the bag has been opened, follow the guidelines for ambient exposure time in the following section to ensure that devices are maintained below the critical moisture level.

4. Manufacturing Conditions/Floor Life

   Microchip classifies surface mount components into levels of moisture sensitivity. The labels on the MBB list the moisture sensitivity level and the allowable floor life. Once the MBB has been opened, Microchip recommends that components from the bag be surface mounted and reflowed within the time indicated on the MBB label. This time is based on a manufacturing environment not more extreme than 30ºC/60% RH, and a maximum component body temperature during solder reflow of 260ºC. If the component cannot be mounted within this timeframe, they should be put into a storage environment immediately, as specified in J-STD-033, or sealed into an MBB as soon as possible.

5. Resealing an MBB

   If there is a need to reseal an MBB for any reason, Microchip recommends the following guidelines to ensure that the bag seal does not allow moisture into the bag. The seal area must not exhibit any separation when subjected to the load and temperature conditions specified in the JEDEC J-STD-033 specification. The integrity of the seal is vital to the storage life of the devices.

REWORK

WLCSP parts removed during PCB rework should not be reused for final assemblies unless the part needs to be used for further Failure Analysis (FA) work.

The WLCSP rework process is similar to the BGA type package rework process. The rework process should follow the below major steps:

- Part Removal – The failed part should be removed from the board by applying hot air on the top of the component and bottom heating the PCB. Discard the removed failed part if it is not needed for FA work.
- PCB Cleaning – The PCB land site need to be properly cleaned and dressed for the attachment of the new component. Either a de-soldering system or iron with solder wick method can be used to effectively remove the residual solder without damaging the solder mask material and/or the pads. It should be noted that the applied temperature should not be >245°C; otherwise, the copper pads on the PCB may peel off.
- Solder Paste Deposition – A mini stencil with the same thickness and aperture openings as the production stencil should be used to deposit the solder paste. The printed solder paste should be inspected to ensure uniform and sufficient volume is deposited before the part placement.
- Part Placement – A WLCSP reworking station with a vacuum nozzle and vision system should be used to pick the new WLCSP part and accurately align and place it on the corresponding footprint.
- Rework Reflow – The replaced WLCSP component is then soldered to the PCB using a temperature profile similar to the production reflow profile. The WLCSP reworking station typically has a programmable reflow profile to be selected for a given part.

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