Electrical Design Final Project

PWM Controlled Fan

3312ENG: Electrical Design Project

S5138877 - Jessy Barber
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Contents

Griffith UNIVERSITY

Gold Coast Campus

Griffith School of Engineering and Built Environment

Electrical Design Project

3312ENG

Trimester 1, 2021

Final Project Report

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Section 1: Introduction

The aim of this project is to design a PWM circuit and a DC power supply to manipulate the RPM of a PC fan with variable resistance from a potentiometer. This project is identical to the DC motor project, except for some differences in goal voltage values needed to drive the fan. This project combines circuit design and knowledge acquired from two previous labs, creating a DC power supply, and creating a triangle wave generator. The triangle wave generator is combined with DC voltage fed through the potentiometer as inputs to a comparator opamp. This produces a PWM waveform where the duty cycle will change with the variable resistance from the potentiometer. This PWM signal is now input to an optocoupler isolation IC which will separate the PWM signal from the DC voltage circuit using a photoresistor and transistor. The DC voltage circuit uses a transformer to supply a 240V amplitude 50Hz sinusoid AC voltage as input and converts this into a DC voltage using a full-wave rectifier and smoothing filter. The output of the optocoupler's emitter acts as the input the MOSFET's gate. The PWM PC fan has 4 pin connections where the +12V pin is connected to the output of the DC voltage circuit, and the GND is connected to the drain pin of the MOSFET.

When the PWM signal at the gate pin is high, the connection to the drain pin is bridged, short circuiting the fan and acting as a break slowing the rotational speed. When the PWM is in a low state, the drain and source pins will be connected, grounding the DC voltage input to the fan, and speeding up its rotation. This means that when the duty cycle of the PWM is low, the fan will be at full speed, and when the duty cycle of the PWM is high, the fan will be at low speed.

Section 2: Detailed Circuit Design

The block diagram for the final circuit design is shown as follow:

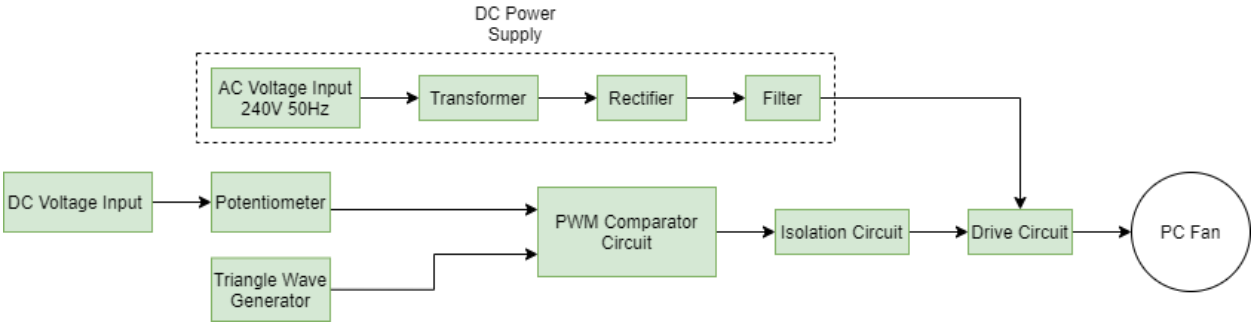


Figure 1: Project Block Diagram

In the final design of the project, it was chosen to use a potentiometer instead of a thermistor to achieve more precise duty cycles produced by the PWM comparator circuit. The circuit was then tested with a DC motor and presented with the PWM controlled PC fan. The pin layout for this fan is shown in appendix i.

The first part of the circuit to design were the inputs to the PWM Comparator circuit. This includes the triangle wave generator and DC voltage manipulated by a potentiometer to cut through the triangle wave.

2.1 Triangle Wave:

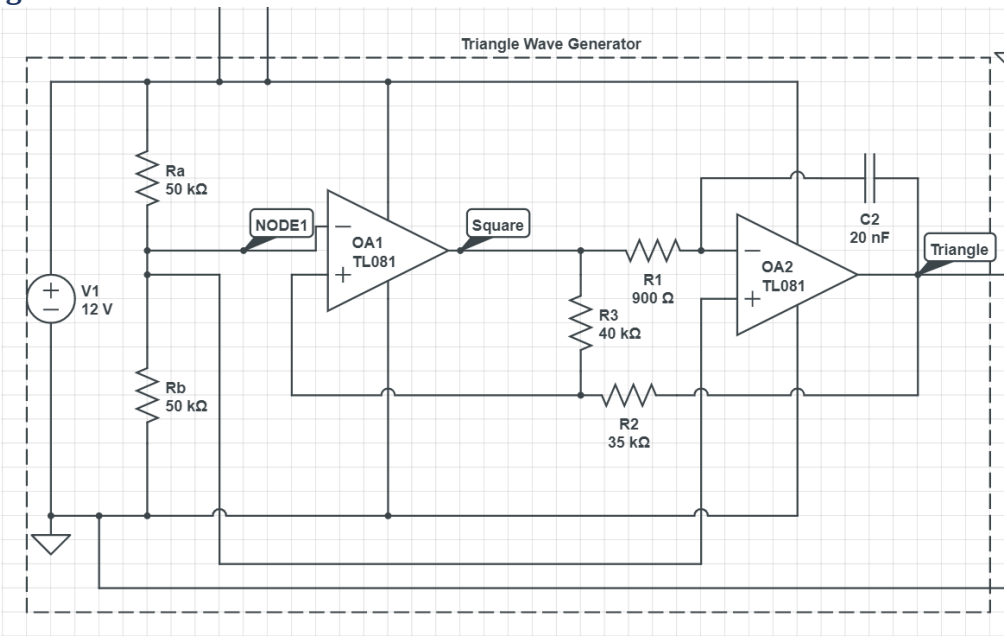


Figure 2: Triangle Wave Generator Circuit Schematic

The PC fan needs between 10V-12V to function, so the V_{CC} used for the circuit was 12V. After this 12V_{CC} was decided upon, the triangle wave generator and potentiometer circuit can be developed. The first step is to decide on an appropriate pk-pk output voltage for the triangle wave. We will use a $V_{pk\text{-}pk}$ of 10.5V and use this to find resistor values R_2 and R_3. These resistor values are found as follows:

$$V_{out(pp)} = V_{cc}\frac{R_2}{R_3} \rightarrow 10.5V = 12V\frac{R_2}{R_3}$$

Choosing an arbitrary value of R_2 = 35k**Ω**:

$$10.5V * R_3 = 420000 \rightarrow R_3 = 40k\Omega$$

If we also choose an arbitrary value of 20nF for the capacitor C_1, we can determine a desirable frequency for the triangle wave and use this to find the value of the R_1 resistor. The ideal frequency to control the PC fan is between 15 and 25kHz and hence:

Assume 15.8kHz:

$$f = \frac{R_3}{4R_1R_2C_1} \rightarrow 15.8kHz = \frac{40k\Omega}{4 * R_1 * 35k\Omega * 20nF} \rightarrow R_1 \approx 900\Omega$$

Since we want the triangle wave to exist in the positive voltage spectrum, we need to determine the voltage input to the negative terminal of OA1 and the positive terminal of OA2 (see appendix ii). We can determine the voltage input that we need by finding the upper and lower thresholds for the peak to peak voltage. A value between 1V and 0V is ideal, and after some practical

tweaking of the components, a minimum voltage level of 720mV was deemed suitable. The new input voltage can now be found as:

$$V_{pp} = V_{UTP} - V_{LTP} \rightarrow 12V - 720mV = 11.28V$$

$$V_{-/+} = \frac{11.28V}{2} + 720mV = 6.36V$$

This means at least 6.36V is required for the input to the negative and positive terminals of opamps OA1 and OA2 respectively, and the voltage divider network can be created around the 12V V_{CC}. If we aim for 6V for the input, R_a and R_b in the voltage divider network can be assigned the same value, and hence assuming R_a and R_b = 50kΩ:

$$V_{-/+} = V_{cc}\frac{R_b}{R_a + R_b} \rightarrow 6V = 12V\frac{50k\Omega}{100k\Omega} = 6V$$

2.2 Comparator PWM Generator:

The comparator circuit uses an opamp to determine whether the input at the negative or positive terminal is higher. The output will be in a high state when the input to the positive terminal is higher, and a low state when the input to the negative terminal is higher. The input to the positive terminal is provided by a potentiometer directly connected to the V_{CC} of 12V. The resistors R4 and R5 are used to manipulate the 12V voltage supplied by the to the comparator circuit to make sure that the potentiometer at a k value of 0 provides a voltage close to the minimum voltage of the triangle wave, and the potentiometer at a k value of 1 provides a voltage close to the maximum voltage of the triangle wave. This is to ensure that the comparator can recognize the maximum and minimum states in which the duty cycle of the PWM wave should be 100%, and 0%. The potentiometer used is 100kΩ and the resistor values R4 and R5 were experimentally chosen to be 8kΩ and 5kΩ respectively to achieve the full range of PWM. As a starting point, these resistor values can be found using the voltage divider equation, treating R4 as Ra and R5 as Rb:

$$Assume\ V_0 \approx 11V \rightarrow \frac{V_o}{V_{cc}} = \frac{R_{pot}}{R_a + R_{pot}} \rightarrow \frac{11V}{12V} = \frac{100k}{R_a + 100k} \rightarrow 4.5k\Omega$$

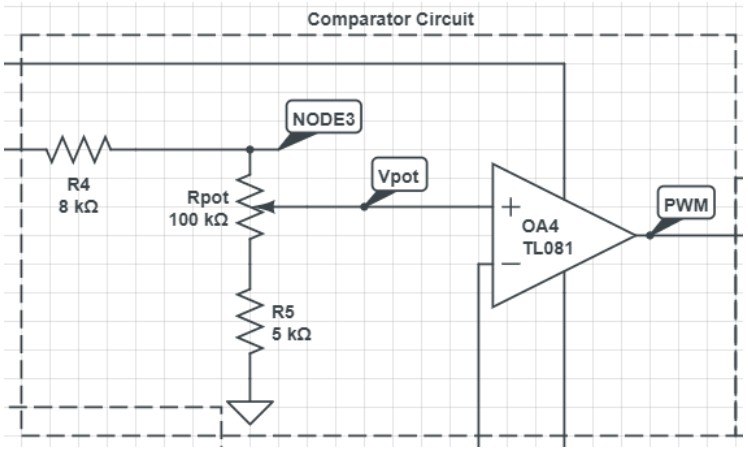


Figure 3: PWM Comparator Circuit Schematic

2.3 DC Power Supply:

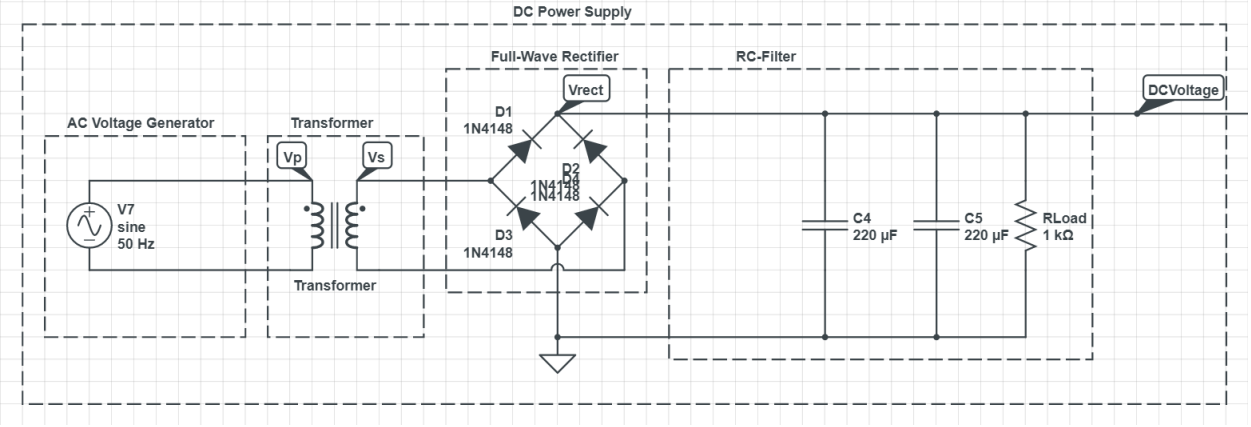


Figure 4: DC Power Supply Circuit Schematic

Since the operational voltage for the PC fan is 12V, the DC power supply circuit must achieve a voltage as close to this value as possible. The transformer used has an amplitude of 240V and 50Hz frequency. The output voltage is set to 10 which means that the turns ration for the transformer between V_P and V_s is 24. This is verified by the following:

$$n = \frac{V_p}{V_s} = \frac{N_p}{N_s} \rightarrow \frac{\sqrt{2} * 240V}{\sqrt{2} * 10V} = 24$$

This AC voltage is rectified using a full-wave rectifier circuit consisting of four ideal diodes and is then smoothed using two electrolytic capacitors and a load resistance.

2.4 Isolation Circuit:

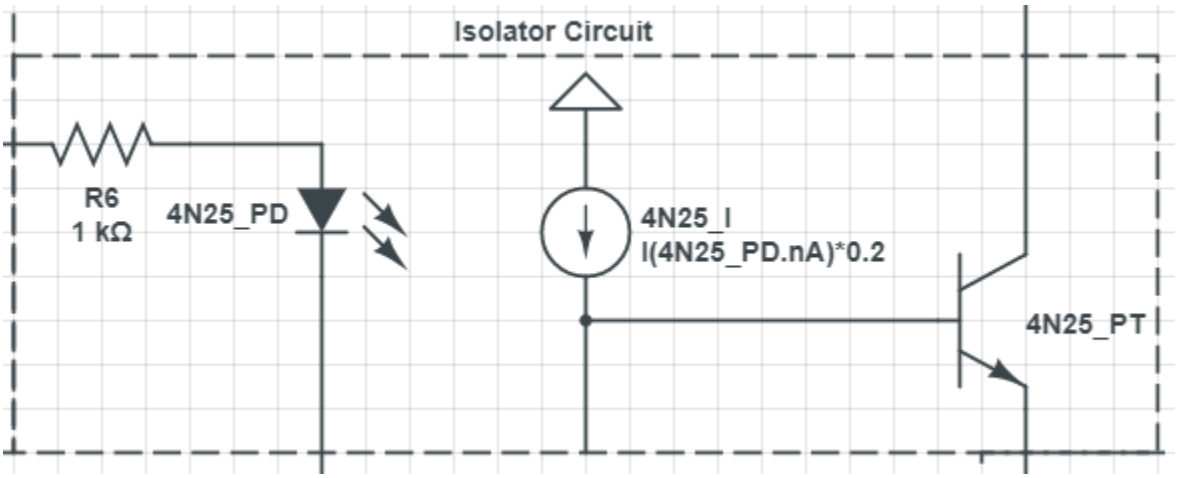


Figure 5: Isolation Circuit Schematic

The isolation circuit is handled by the 4N25 (see appendix iii), which includes an optocoupler and photoresistor output with base connection. The base will remain unconnected in this circuit and only pins 1, 2, 4 and 5 will be used. A 1kΩ resistor is used between the PWM comparator opamps output and the input to pin 1 to the photoresistor. This is to provide the photoresistor with suitable current to safely operate. The input of pin 5, the collector of the transistor is

connected to the output of the DC voltage waveform. Pin 4, the emitter of the transistor is now output to a voltage divider consisting of R7 = 10kΩ and R8 = 100Ω. R7 is connected to ground and R8 is connected to the gate pin of the N-channel IRLZ44N MOSFET junction (see appendix iv). The isolation circuit is now effectively separating the voltage from the DC power supply waveform and the PWM output waveform.

2.5 Drive Circuit:

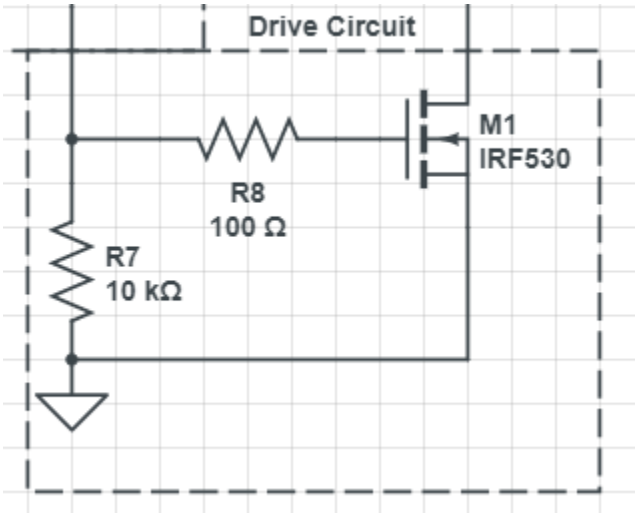


Figure 6: Drive Circuit Schematic

The driver circuit consists of the N-channel MOSFET where the gate is connected to the output of the isolation circuit, the drain is connected to the GND pin of the PC fan and the source is connected to ground. The N-channel MOSFET is an enhancement type which means that the gate opens when sufficient positive voltage is supplied and will flow through the MOSFET's drain pin. When the voltage is not high enough at the gate pin, the connection between the gate and the drain will be closed and the drain will be directly connected to the source pin, providing the connection to GND. Since the positive +12V input to the PC fan is provided by the DC power input, the GND pin of the fan can only reach GND when the gate drain connection is closed. This occurs when the PWM signal is at a low state and hence the PWM wave manipulates the duty cycle of the +12V input to the fan. For every high state produced by the PWM wave, the GND pin of the fan will be supplied +12V, and hence a short circuit will occur acting like a brake on the motor. For every low state produced by the PWM wave, the GND pin of the fan will be directly connected to GND, allowing the fan to spin.

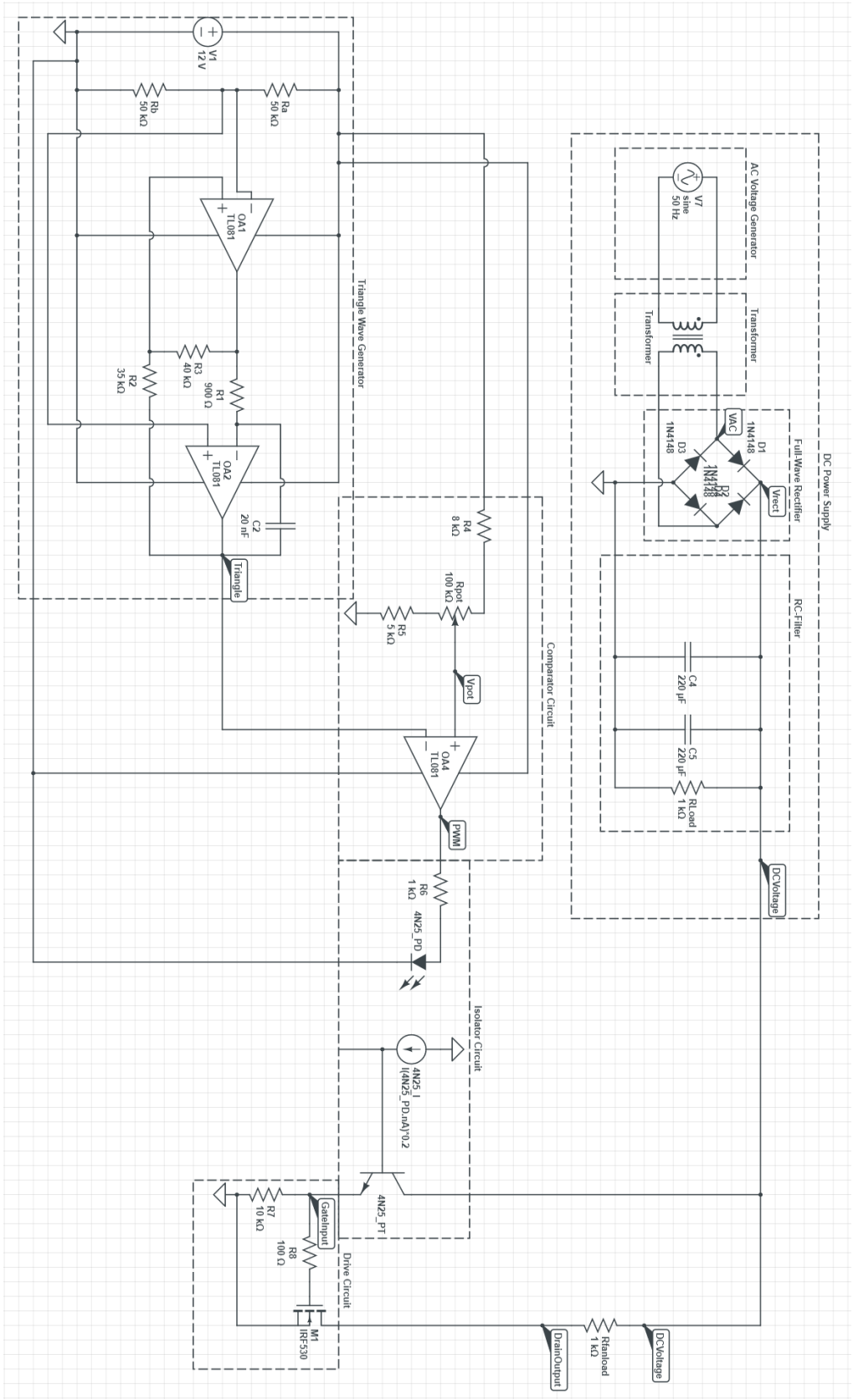


Figure 7: Full Circuit Schematic

Section 3: Simulation Results and Waveform Analysis

The first waveforms that will be analyzed are the inputs to the comparator opamp. This is the triangle wave and different levels of DC input dictated by the resistance of the potentiometer. These **test points** are taken from the **Triangle**, **PWM** and **Vpot nodes** shown in the full circuit schematic.

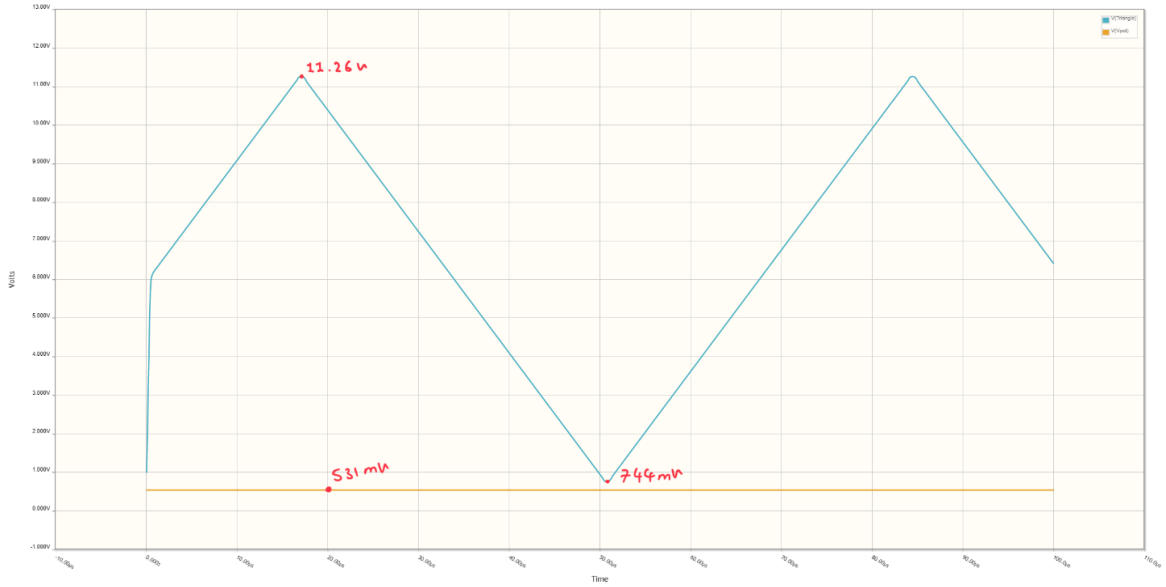


Figure 8: Simulated Triangle Wave & Potentiometer Voltage at k = 0

As we can see from the above image, when the k value of the potentiometer is set to 0, the DC voltage input passing through the potentiometer never reaches a higher voltage than the triangle wave and results in the following 0% Duty Cycle.

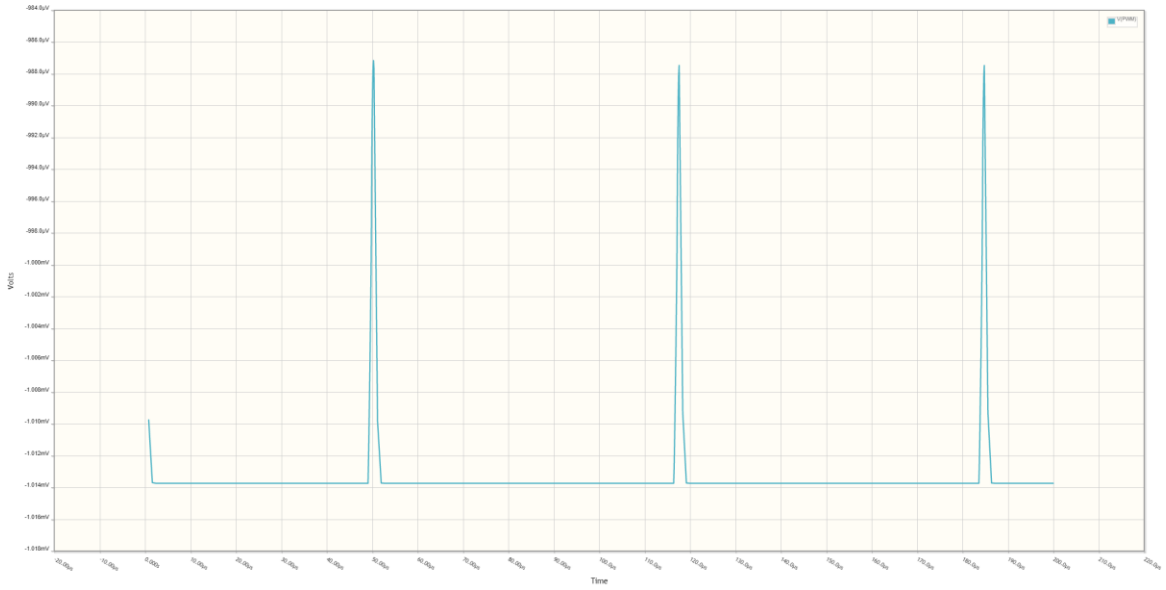


Figure 9: Simulated PWM at 0% Duty Cycle

As above, the PWM waveform at 0% Duty Cycle and its peaks exist in the negative voltage spectrum. Even though there are peaks, the waveform is considered to be in an always off state since there is not enough positive voltage to switch the MOSFET gate drain connection on.

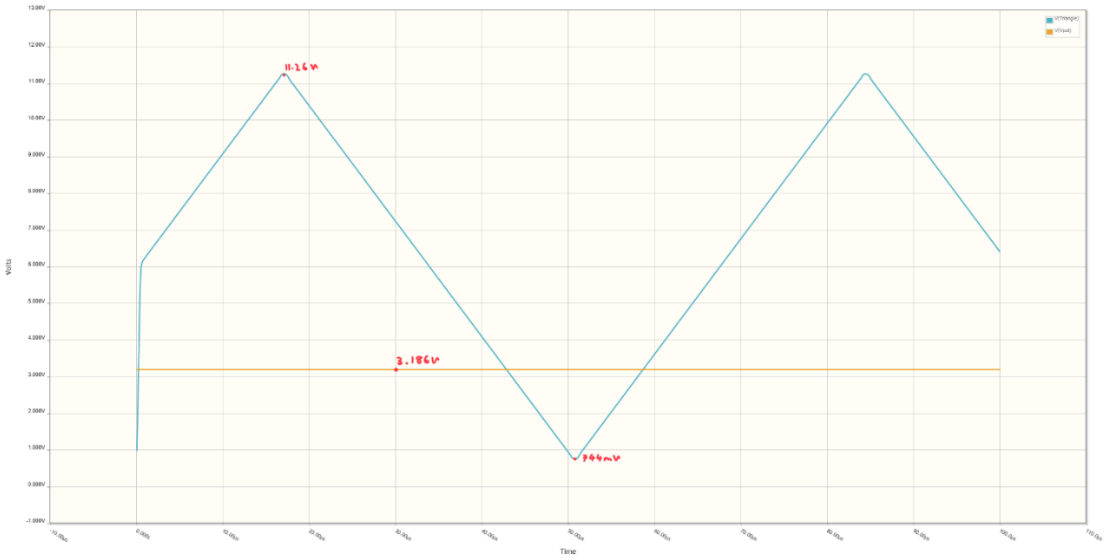


Figure 10: Simulated Triangle Wave & Potentiometer Voltage at k = 0.25

At a k value of 0.25, the DC voltage from the potentiometer should be at 25% of the maximum triangle wave generator. This should be approximately 2.815V but exists at 3.186V instead. This means that the simulated voltage for a duty cycle of 25% has a percentage error of 13.18% if 3.186V is assumed to be the exact expected value. This is verified by:

$$\%error = \frac{3.186V - 2.815V}{2.815V} * 100 = 13.18\%$$

The resultant PWM waveform of k = 0.25 is shown below.

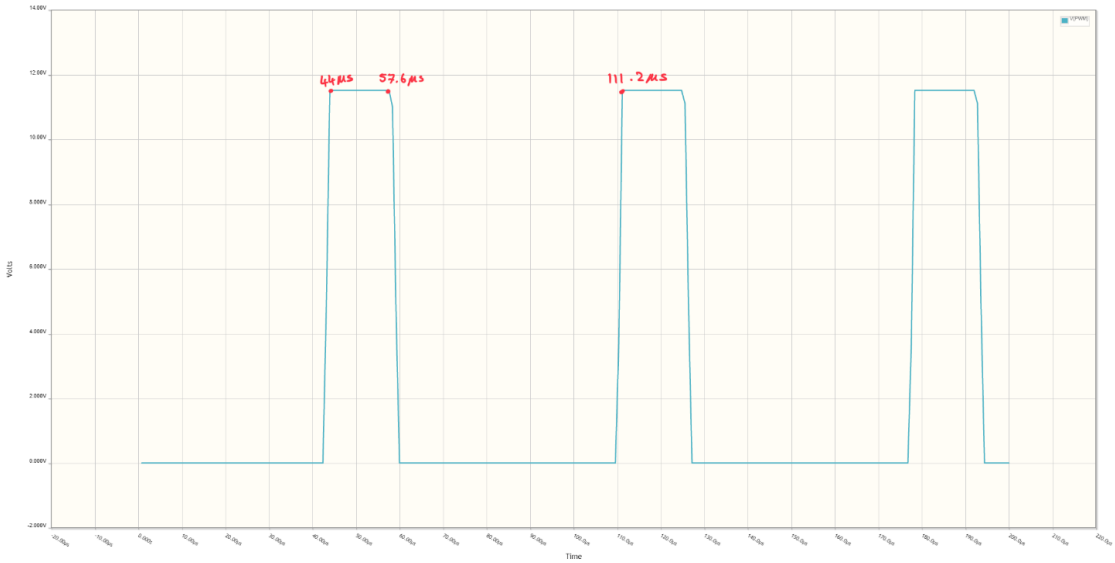


Figure 11: Simulated PWM at 25% Duty Cycle

The simulated Duty Cycle can be found by taking the Pulse Width from a pulse, and the period of the signal. This can be done using the following mathematical formula:

$$Duty\ Cycle = \frac{PW}{T} * 100\% \rightarrow \frac{57.6\mu s - 44\mu s}{111.2\mu s - 44\mu s} * 100\% = \frac{13.6\mu s}{67.2\mu s} * 100\% = 20.24\%$$

The Duty Cycle from the simulation is less than the expected value of 25%, if we assume that 25% is the true value, the percentage error between the expected Duty Cycle and achieved Duty Cycle is:

$$\%error = \frac{25 - 20.24}{25} * 100 = 19.04\%$$

This means that the achieved simulated Duty Cycle of 20.24% has a percentage error of 19.04% from the expected Duty Cycle of 25%.

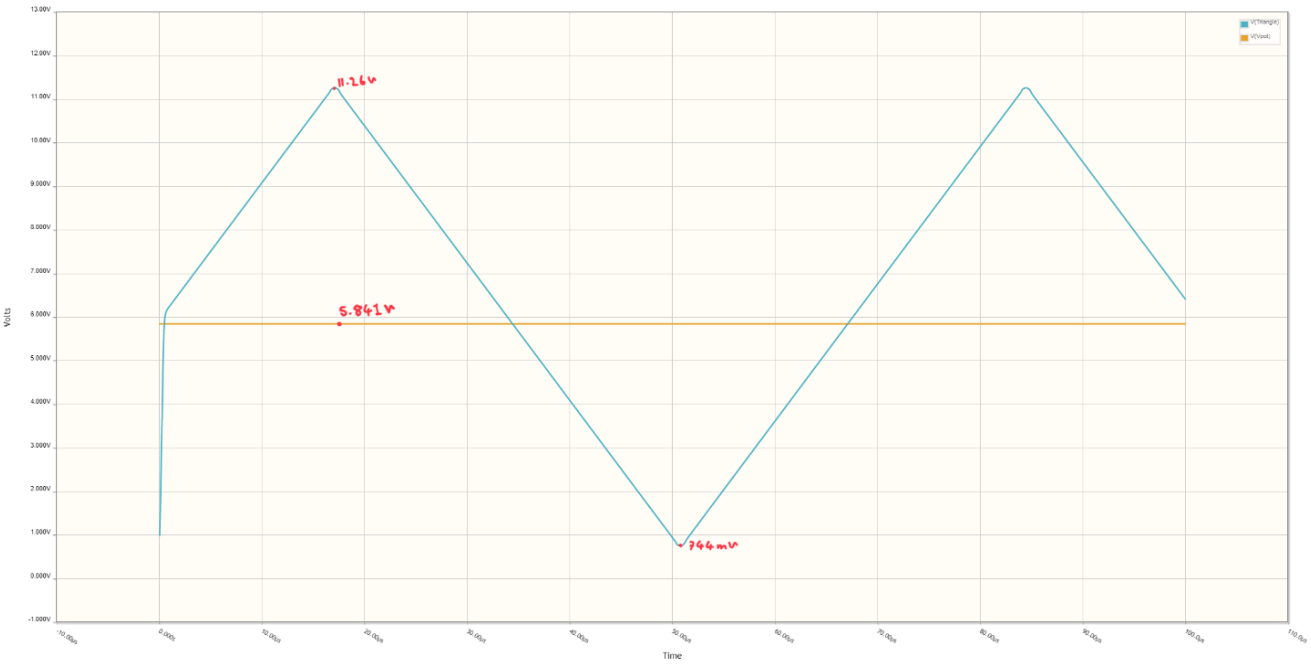


Figure 12: Simulated Triangle Wave & Potentiometer Voltage at k = 0.5

As seen in the waveform above, at a k value of 0.5 the DC voltage from the potentiometer should be at 50% of the maximum triangle wave generator. This should be approximately 5.63V but exists at 5.841V instead. If 5.63V is considered the expected exact value, the achieved voltage of 5.841V has a percentage error of 3.75% as verified by:

$$\%error = \frac{5.841V - 5.63V}{5.63V} * 100 = 3.75\%$$

The resultant PWM waveform achieved from a k value of 0.5 is as follows:

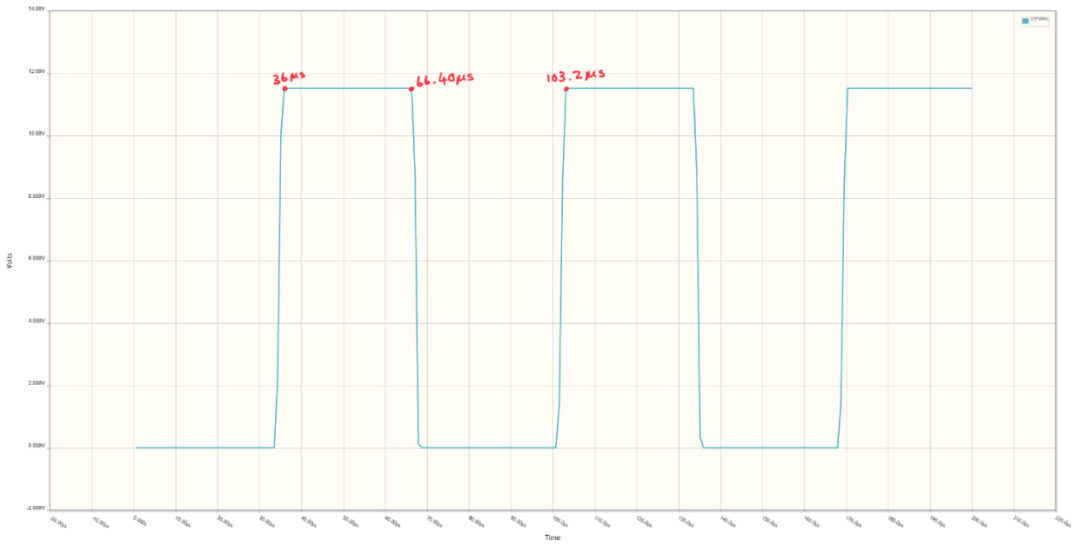


Figure 13: Simulated PWM at 50% Duty Cycle

The simulated Duty Cycle can be calculated by observing the Pulse Width and period of the above waveform. This can be calculated as follows:

$$Duty\ Cycle = \frac{PW}{T} * 100\% \rightarrow \frac{66.4\mu s - 36\mu s}{103.2\mu s - 36\mu s} * 100\% = \frac{30.4\mu s}{67.2\mu s} * 100\% = 45.24\%$$

The Duty Cycle achieved from the simulation is off by just under 5% and the percentage error of this, assuming 50% is the true desirable value is:

$$\%error = \frac{50 - 45.24}{50} * 100 = 9.52\%$$

Therefore, the simulated Duty Cycle of 45.24% has a percentage error of 9.52% when compared with the expected value of 50%.

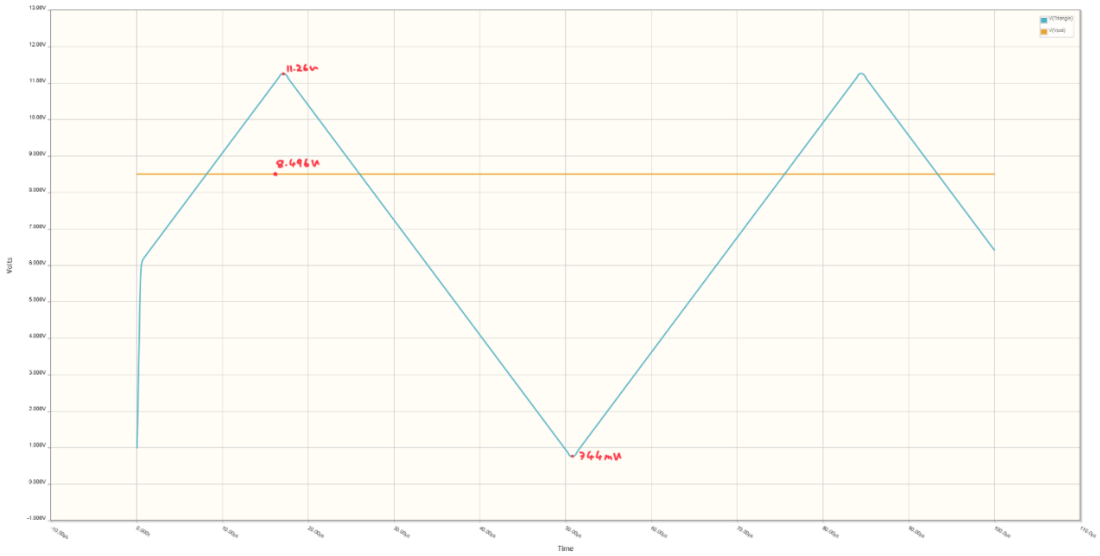


Figure 14: Simulated Triangle Wave & Potentiometer Voltage at k = 0.75

As seen in the waveform above, at a k value of 0.75 the DC voltage from the potentiometer should lie at 75% of 11.26V. The achieved value lies at 8.496V, and if the true value is considered as 8.445V:

$$\%error = \frac{8.496V - 8.445V}{8.445V} * 100 = 0.604\%$$

The achieved value of 8.496V is very close to the expected voltage of 8.445V and only deviates by 0.604%. The PWM waveform for a k value of 0.75 is shown in the waveform below:

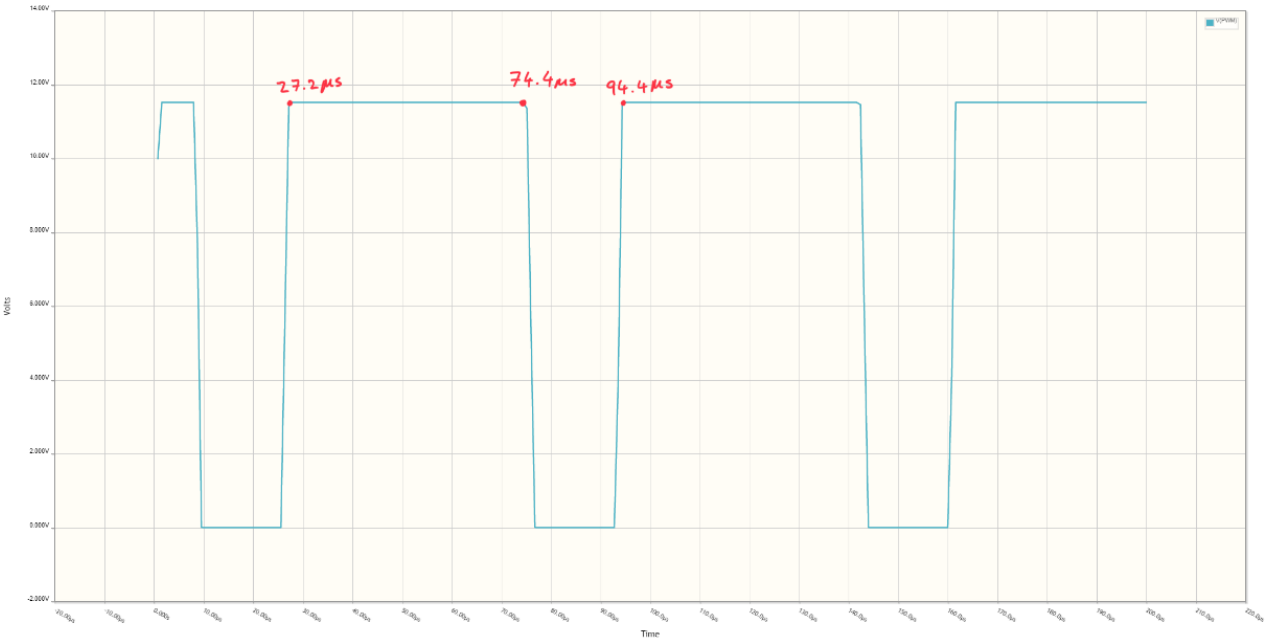


Figure 15: Simulated PWM at 75% Duty Cycle

The simulated Duty Cycle is can be calculated by observing the Pulse Width and period of the PWM signal. This can be calculated as follows:

$$Duty\ Cycle = \frac{PW}{T} * 100\% \rightarrow \frac{74.4\mu s - 27.2\mu s}{94.4\mu s - 27.2\mu s} * 100\% = \frac{47.2\mu s}{67.2\mu s} * 100\% = 70.24\%$$

The Duty Cycle achieved from the simulation is just under 5% of the expected value. Considering that 75% is the expected value:

$$\%error = \frac{75 - 70.24}{75} * 100 = 6.35\%$$

This means that the simulated Duty Cycle of 70.24% has a percentage error of 6.35% compared to the expected value of 75%.

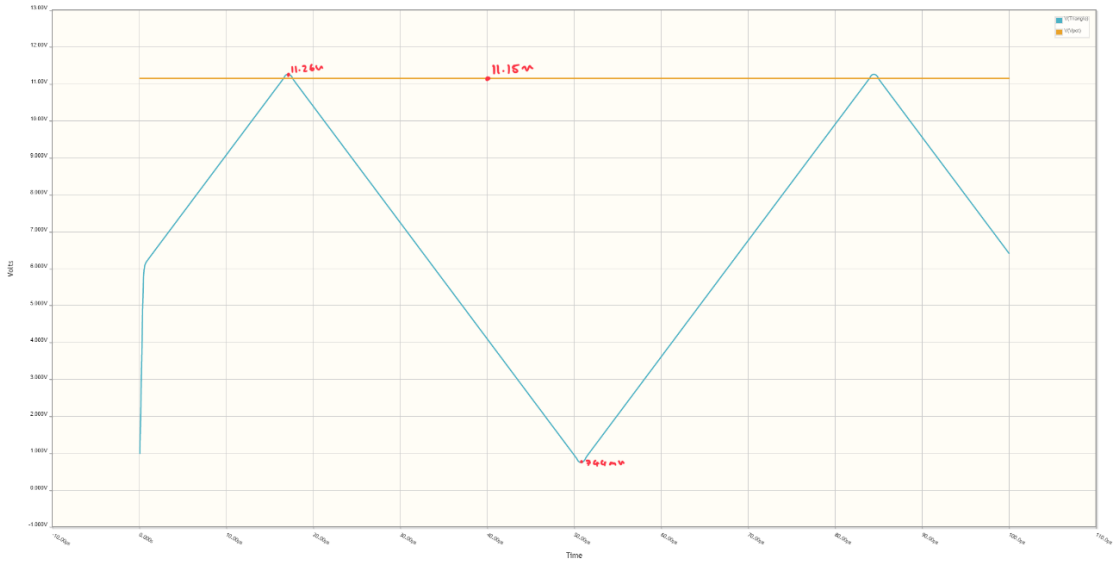


Figure 16: Simulated Triangle Wave & Potentiometer Voltage at k = 1

As seen in the waveform above, the DC voltage from the potentiometer with k = 1 lies just under the expected value of 11.26V at 11.15V. If the true value is considered 100%, the percentage error is:

$$\%error = \frac{11.26V - 11.15V}{11.26V} * 100 = 0.98\%$$

The simulated voltage value is very close to the expected voltage value. The PWM waveform for k = 1 is shown below:

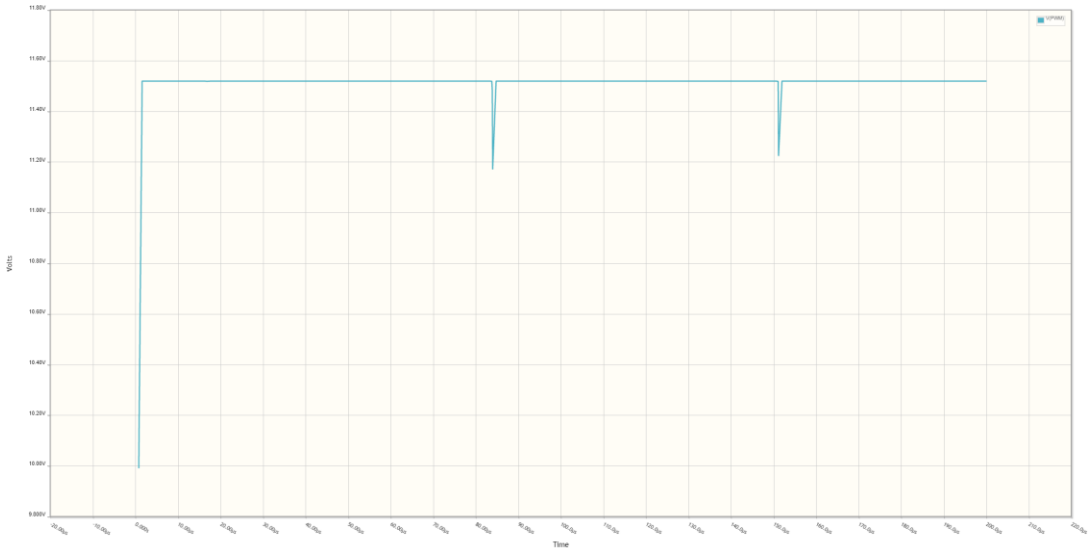


Figure 17: Simulated PWM at 100% Duty Cycle

As seen above, the PWM waveform is at 100% Duty Cycle with some minor dips. Since the dips are minor, this PWM waveform is sufficient to open the MOSFET gate drain connection to provide the fan with 100% speed.

The output for the DC voltage supply is measured from the **test points** of the **VAC** and **DCVoltage node**.

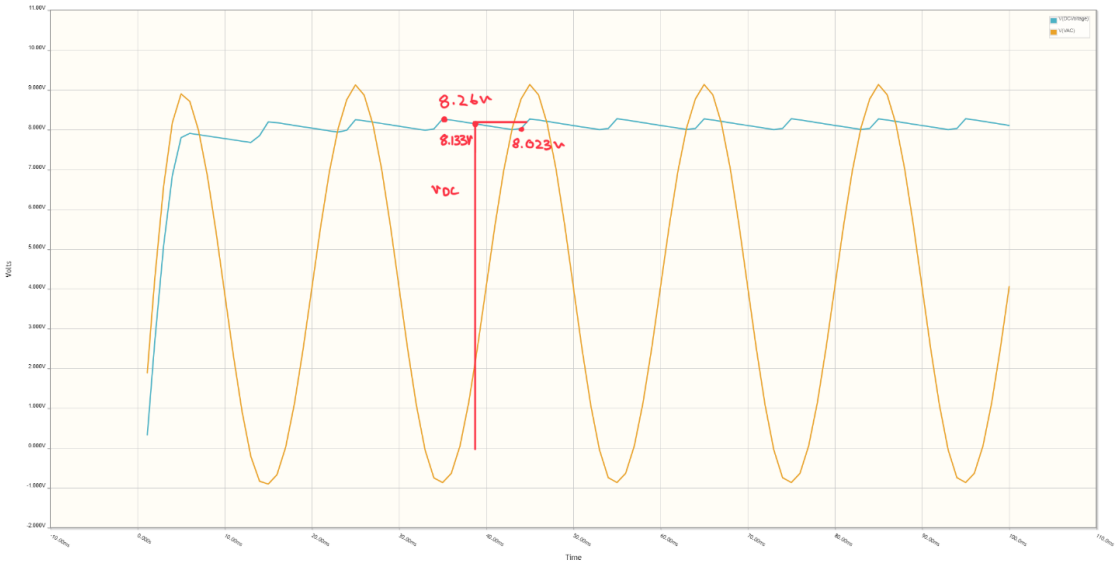


Figure 18: Simulated AC Voltage & Smoothed Ripple Voltage

As seen above, the waveform is only achieving a maximum of around 8.3V. This was found to be different in the breadboard implementation phase, and the real-life value is closer to 11V. The ripple factor of the smoothed voltage can be found by finding the peak to peak voltage $V_{R(pp)}$ and average DC voltage V_{DC} of the smoothed voltage waveform.

$$V_{R(pp)} = 8.26V - 8.023V = 0.237V, V_{DC} = 8.133V$$

$$Ripple\ Factor = \frac{V_{R(pp)}}{V_{DC}} \rightarrow \frac{0.237V}{8.133V} = 0.029$$

The ripple factor is very low which means that the rectified output is being ideally smoothed by its capacitors. The following are the waveforms for the drain output and the gate input of the MOSFET measured at the test points **DrainOutput** and **GateInput**.

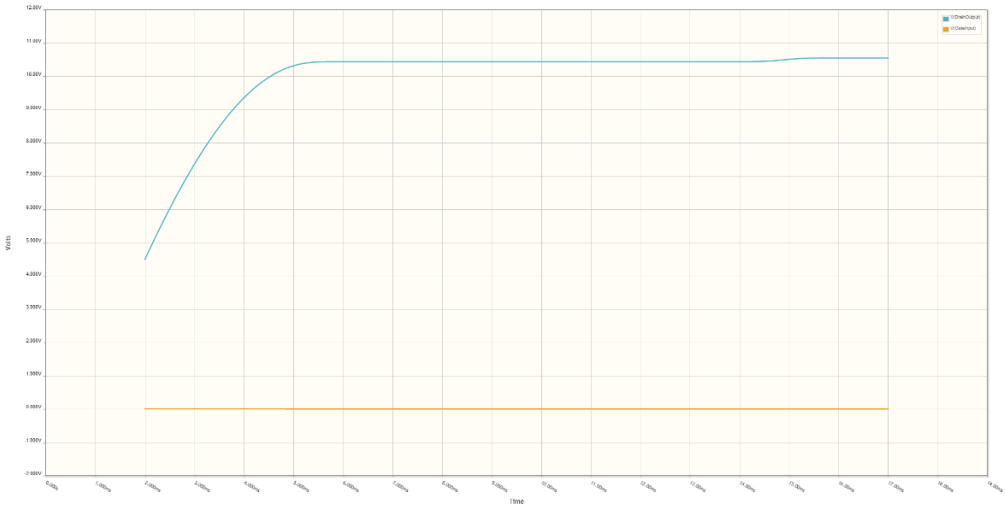


Figure 19: Simulated Drain Output & Gate Input at 0% Duty Cycle

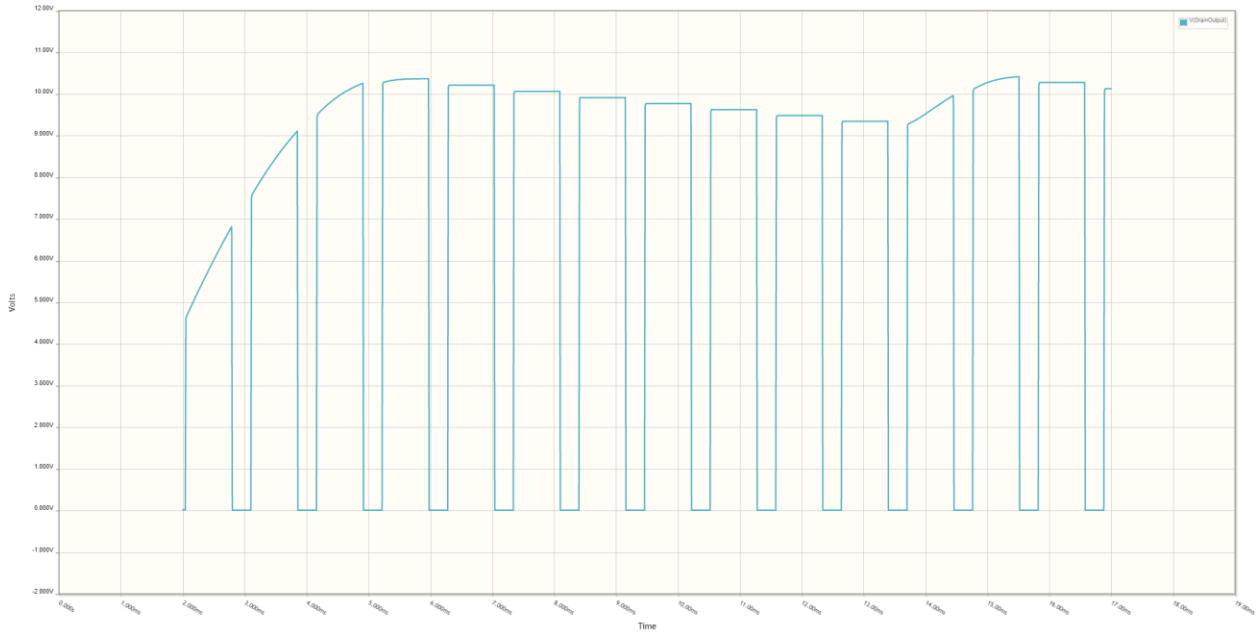


Figure 20: Simulated Drain Output at 25% Duty Cycle

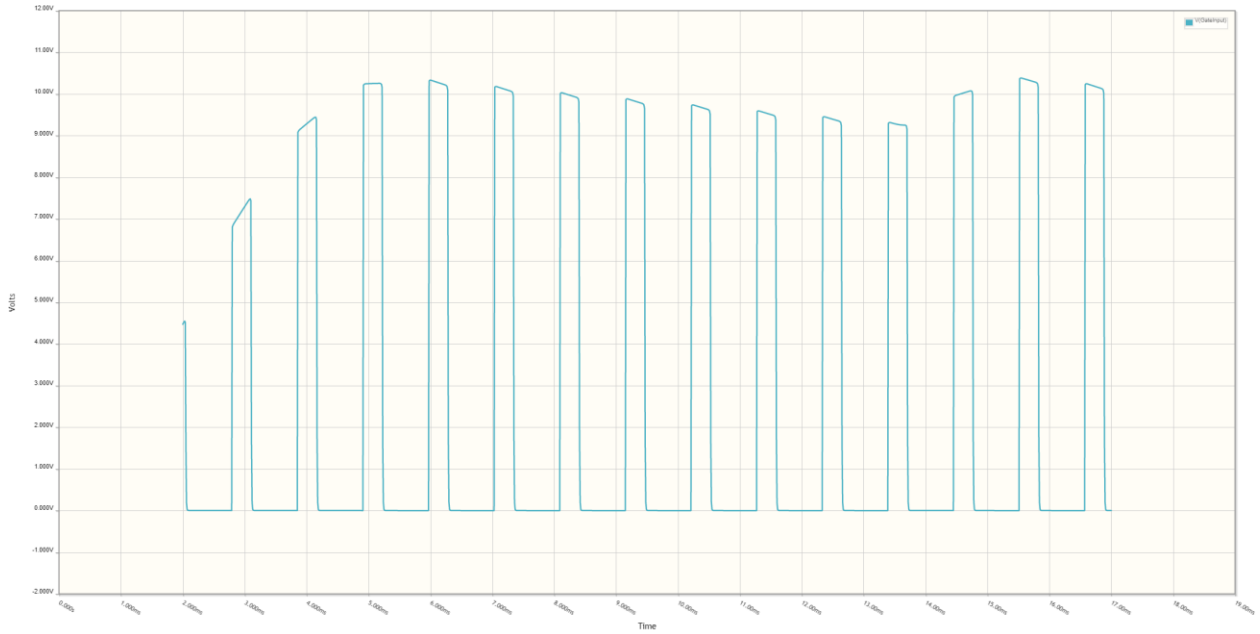


Figure 21: Simulated Gate Input at 25% Duty Cycle

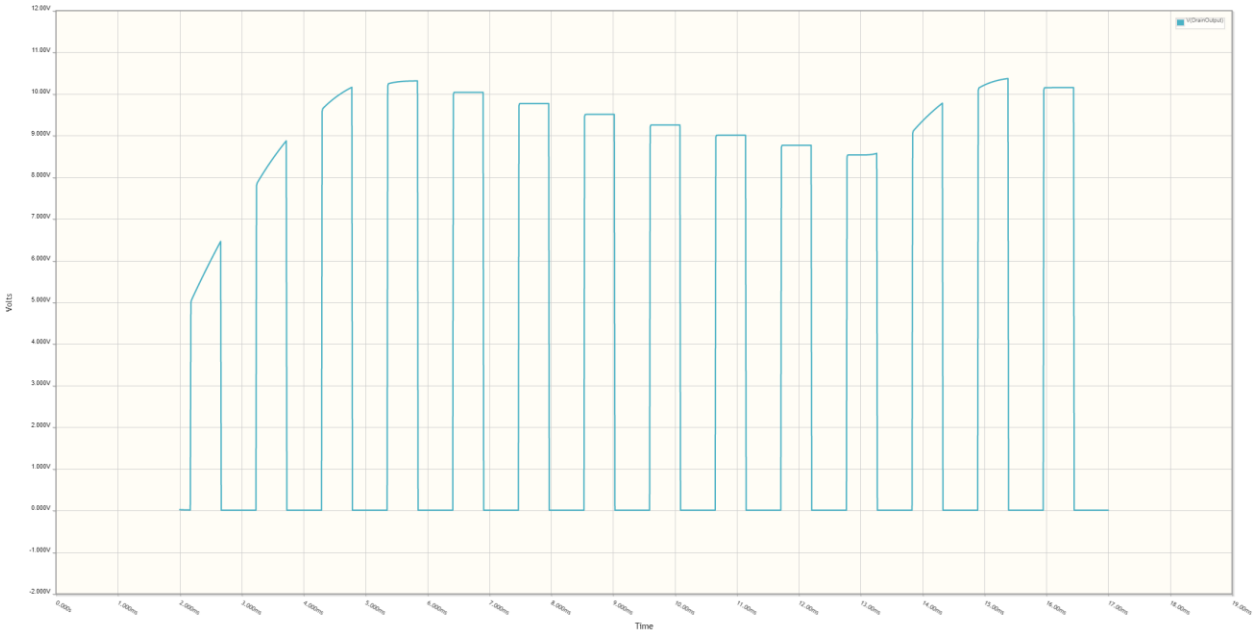


Figure 22: Simulated Drain Output at 50% Duty Cycle

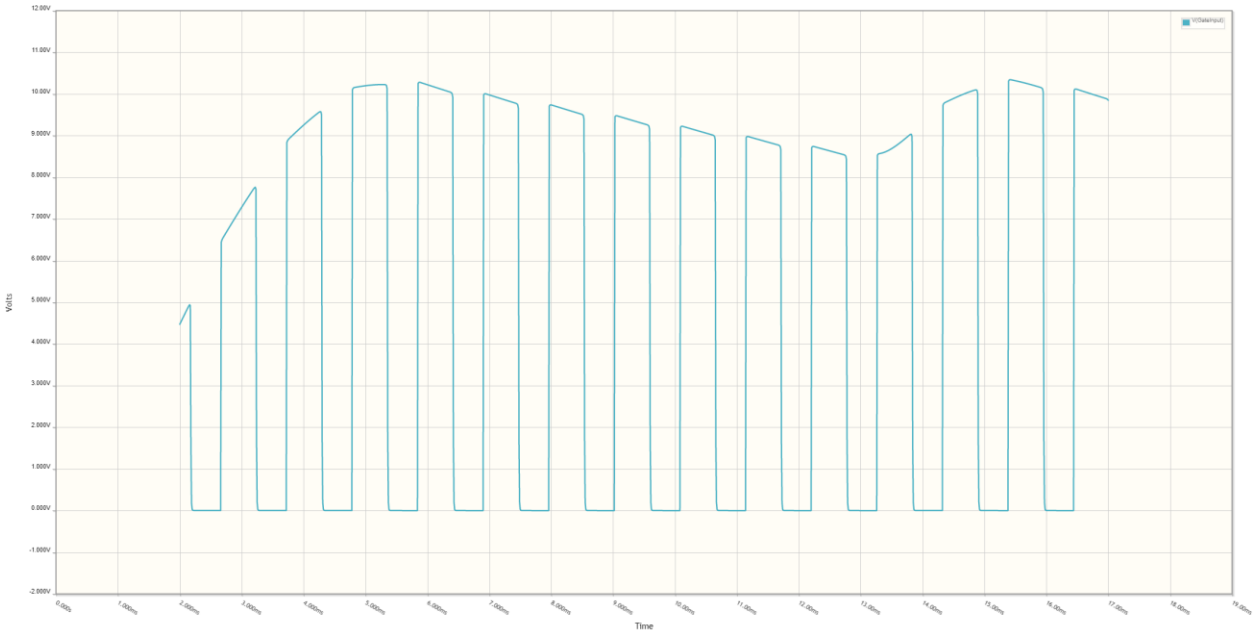


Figure 23: Simulated Gate Input at 50% Duty Cycle

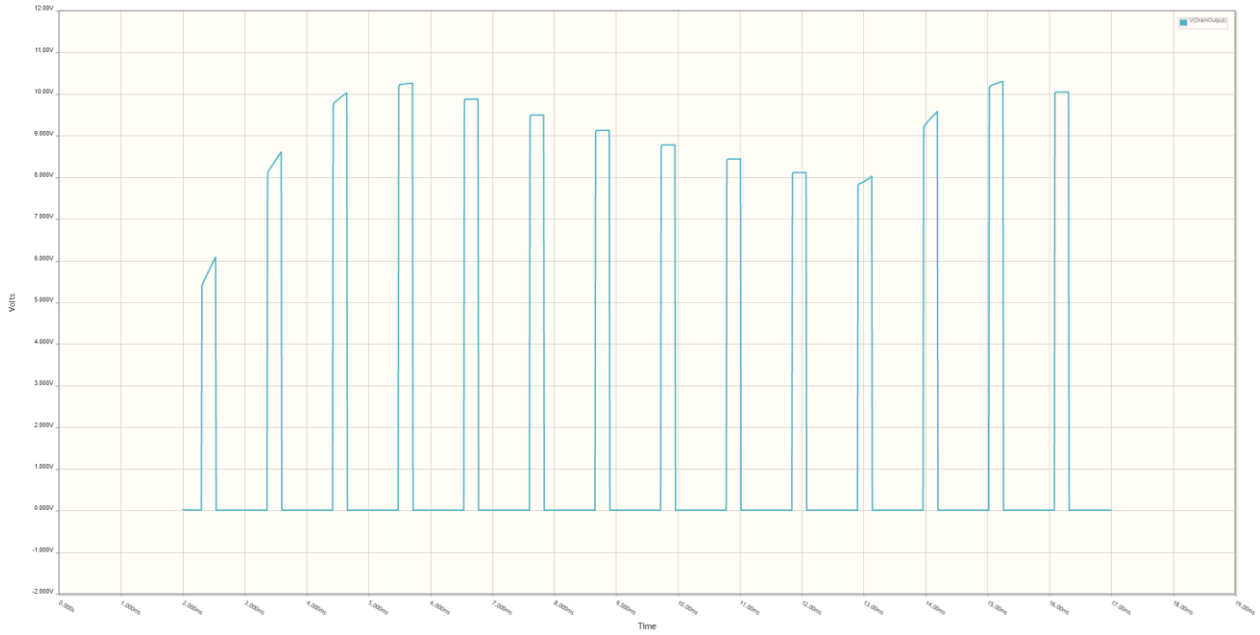


Figure 24: Simulated Drain Output at 75% Duty Cycle

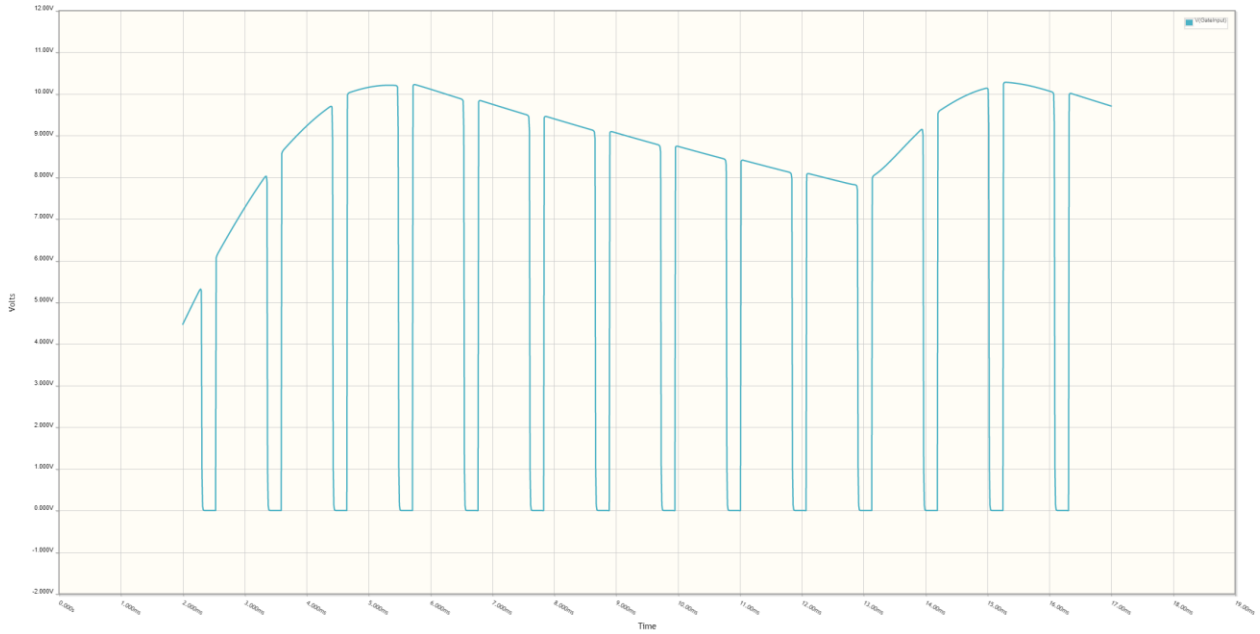


Figure 25: Simulated Gate Input at 75% Duty Cycle

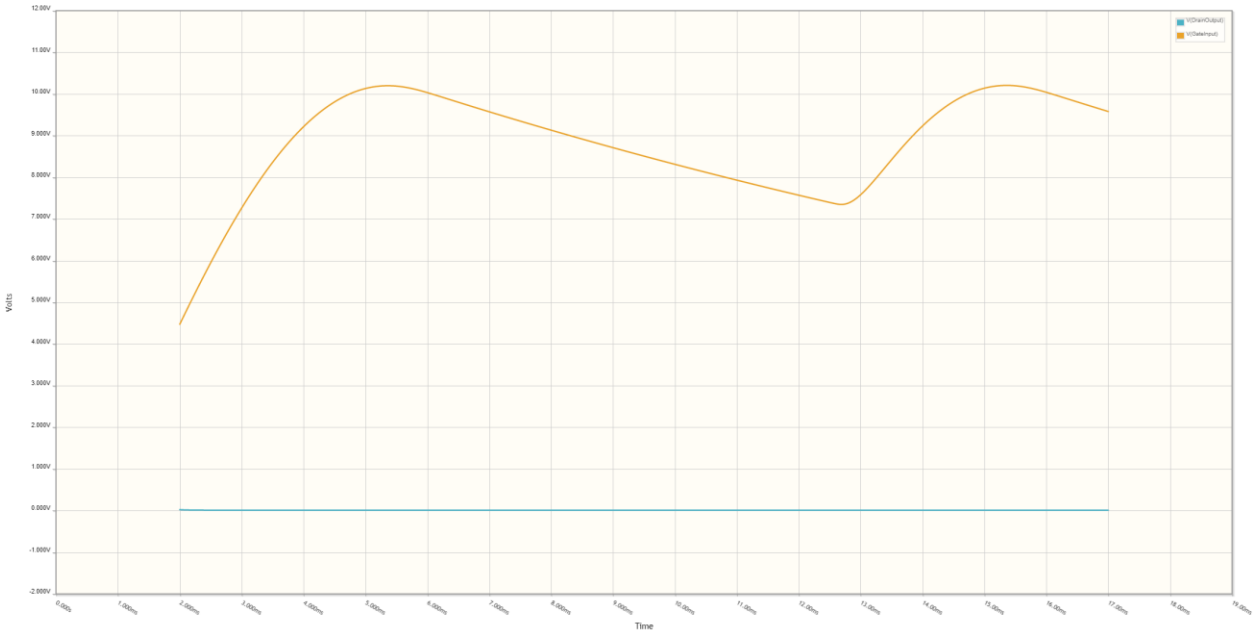
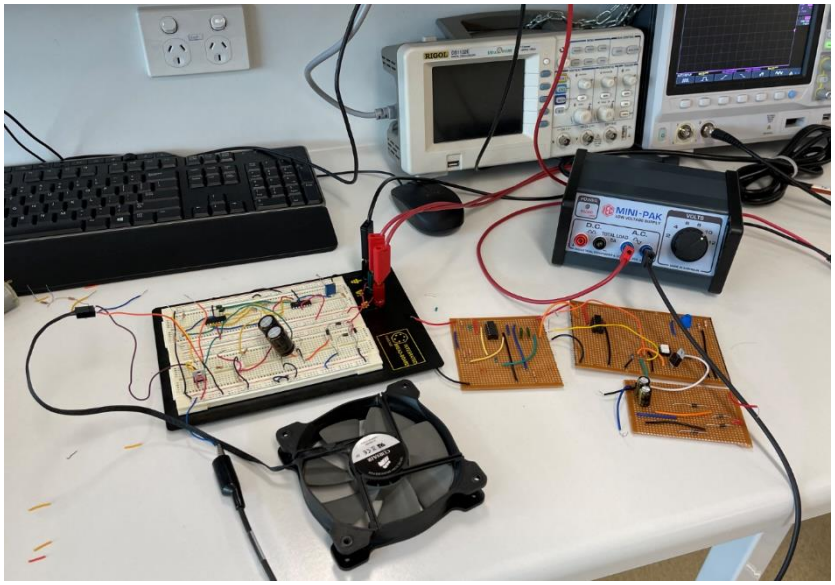


Figure 26: Simulated Drain Output & Gate Input at 100% Duty Cycle

Section 4: Full Circuit Implementation

The circuit was completely implemented on a bread board and was functional in this state. The circuit was also implemented on a Vero Board but was non-functional at the PWM waveform, however the triangle wave and DC Voltage generator modules were functional. The following images present these implementations:



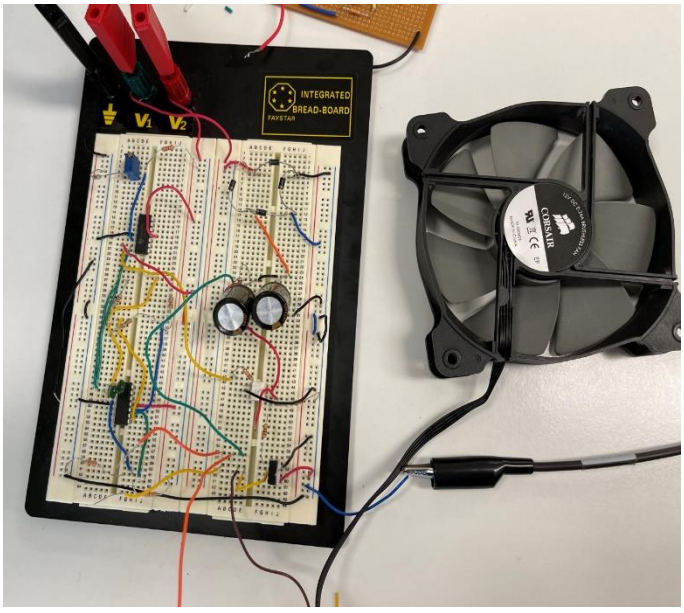


Figure 27: Bread Board and Vero Board Implementations

Figure 28: Bread Board Implementation

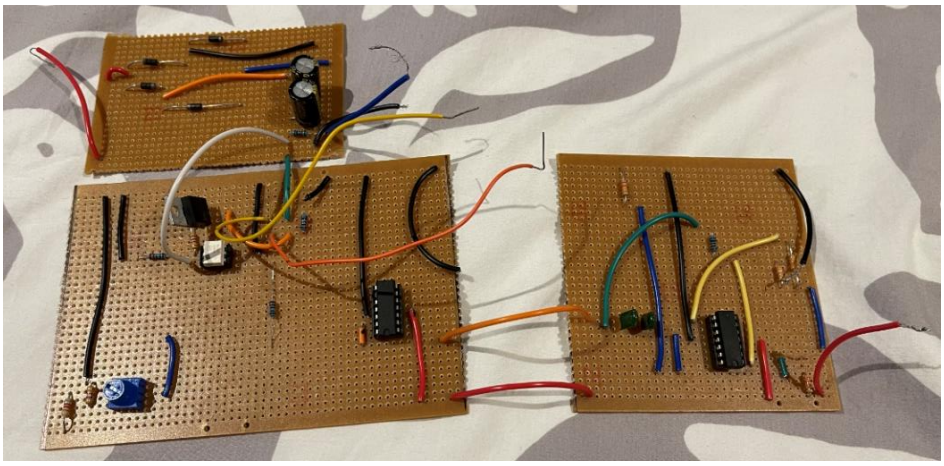


Figure 29: Vero Board Implementation

Section 5: Test Procedure

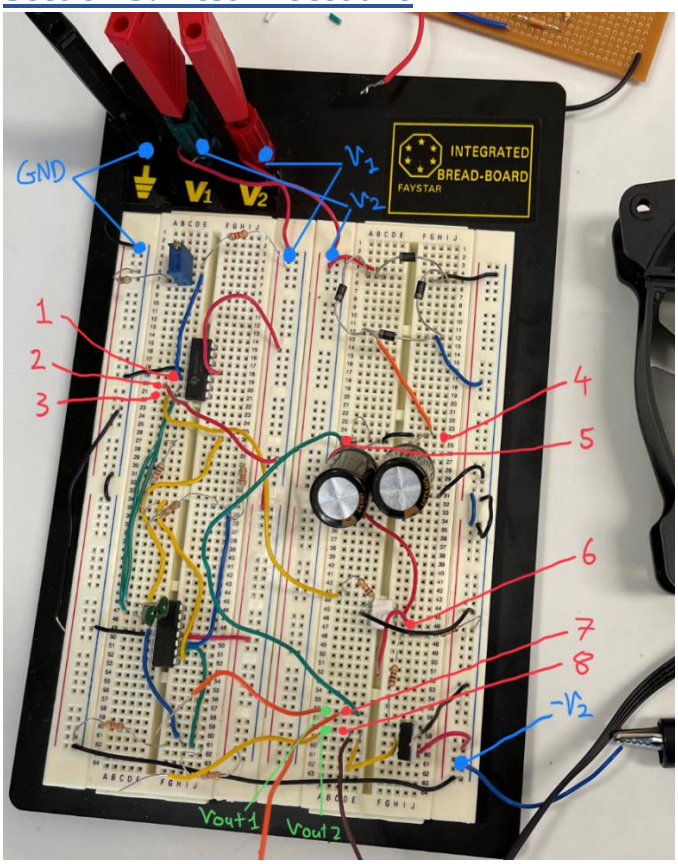


Figure 30: Bread Board Test Point

1. (Vpot): DC output from potentiometer.
2. (Triangle): Triangle waveform.
3. (PWM): PWM waveform.
4. (Vrect): Rectified DC voltage.
5. (DCVoltage): Smoothed DC voltage.
6. (GateInput): Isolator emitter output and drive circuit gate input.
7. (DCVoltage): DC voltage input to fan.
8. (DrainOutput): Output of drive circuit drain pin and fan GND input.

Adding test connections to the specified test points above will enable the user to measure the nodes shown in the full circuit schematic. All test points should be measured on a digital oscilloscope and waveforms should be observed for different k values of the potentiometer.

Port V_1 and GND are connected to power supply with +12V.

Port V_2 and $-V_2$ (blue wire) are connected to transformer with output dial set to 10.

Connect V_{out1} to the +12V pin on the PC fan, and V_{out2} to the GND pin on the PC fan.

Step 1: Confirm that the circuit is free from loose wires or damaged components. Now ensure that the entire circuit is deenergized and has not been connected to any form of voltage source / power supply.

Step 2: Perform a continuity test on each sub-circuit of the main circuit to ensure there are no shorts or open circuits.

Step 3: Verify the integrity of the isolation in the optocoupler by testing the resistance at each pin.

Step 4: Before connecting the transformer, ensure the correct RMS voltage is being supplied.

Step 5: Before connecting the power supply, ensure the power supply is producing 12V. Also ensure that the power rails on the bread board are working correctly and the mid sections have been bridged.

Step 6: Connect the negative lead of the transformer to the blue wire connected to the second lowest power rail, as seen in the test point -V2. Connect the positive lead of the transformer to the V2 breadboard input.

Step 7: Verify the input AC voltage by measuring the un-rectified waveform.

Step 8: Connect the DSO to test points 4 and 5 and verify the rectified and smoothed DC voltage waveforms.

Step 9: Connect the positive power supply lead to the V1 breadboard input, and the negative power supply lead to the GND breadboard input.

Step 10: Connect the DSO to test points 1, 2 and 3 and verify the triangle wave, potentiometer output and PWM waveforms.

Step 11: Connect the DSO to test points 6, 7, and 8 and verify the MOSFET gate input, MOSFET drain output and DC voltage output waveforms.

Step 12: Record and observe all waveforms at different k levels of the potentiometer.

Step 13: Turn off all power supplies and voltage inputs and connect the +12V input of the PC fan to test point V_{out1} and connect the GND input of the PC fan to test point V_{out2}.

Step 14: Observe the speed of the motor as well as the PWM and DrainOutput waveforms as the variable resistance of the potentiometer is changed.

Step 15: Verify the full range of Duty Cycles is achievable and the motor can achieve 0% - 100% speed.

Section 6: Test Results

The following test results were acquired by measuring the test points specified in the test procedure on a digital oscilloscope.

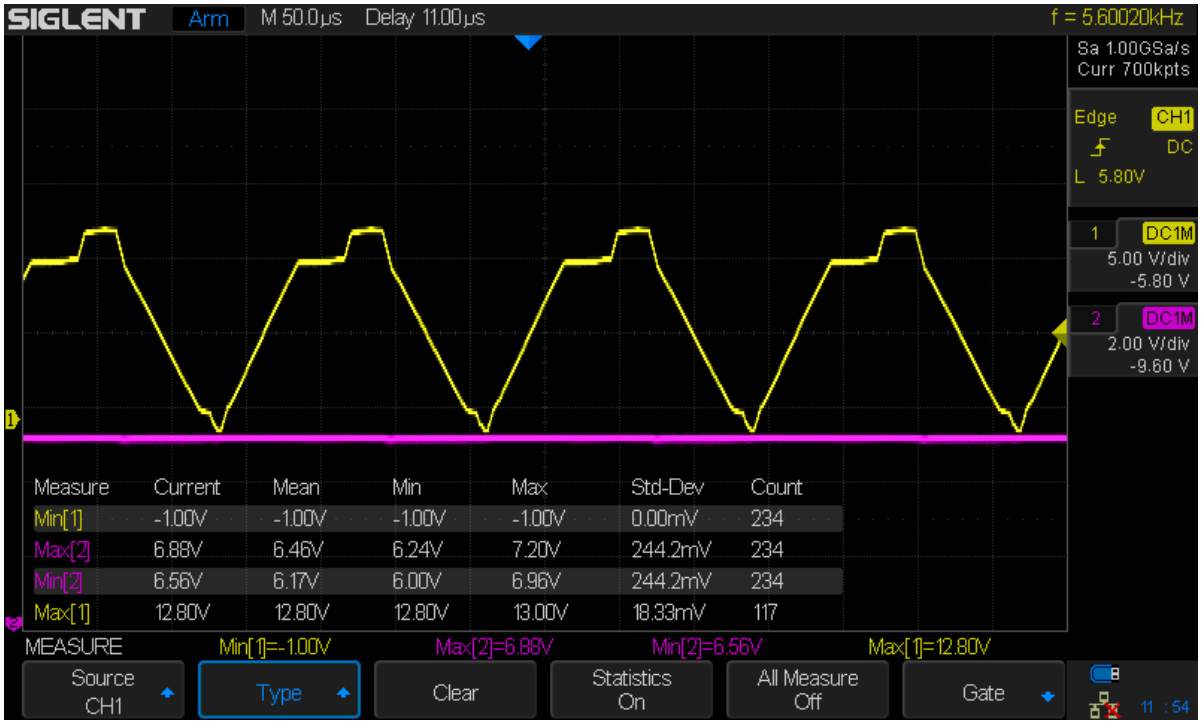


Figure 31: DSO Triangle Wave & Potentiometer Voltage at k = 0

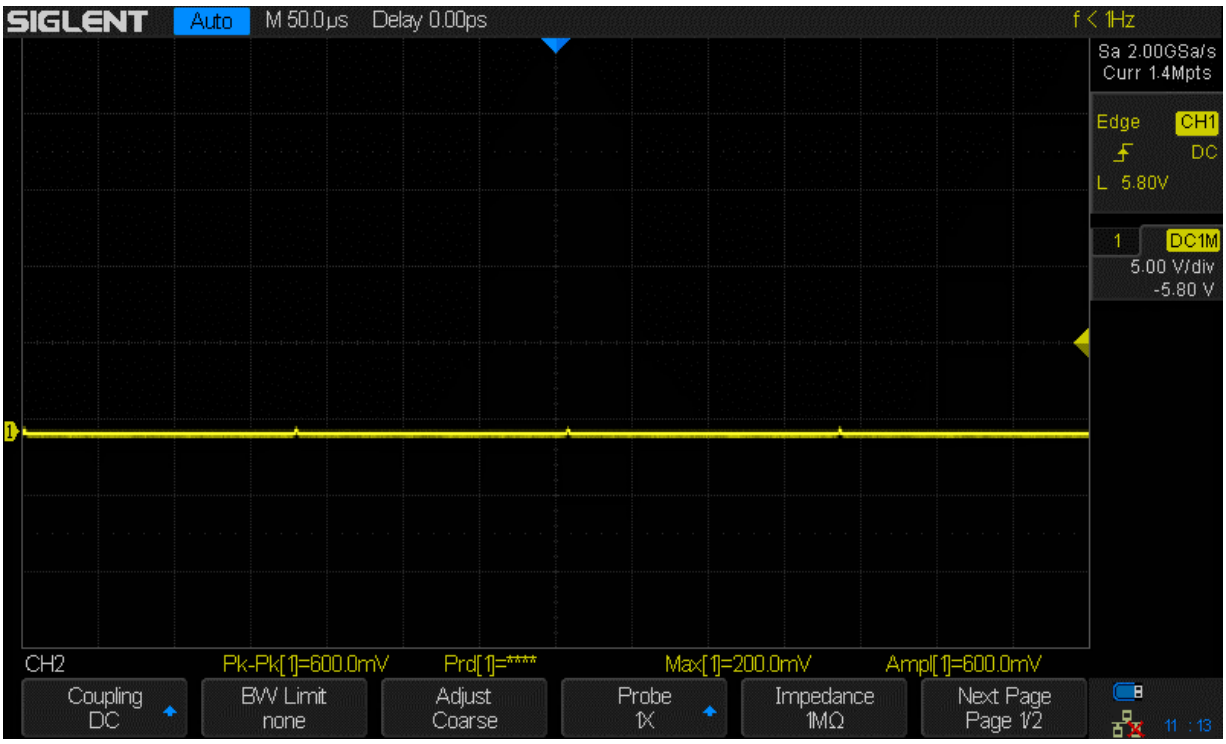


Figure 32: DSO PWM at 0% Duty Cycle

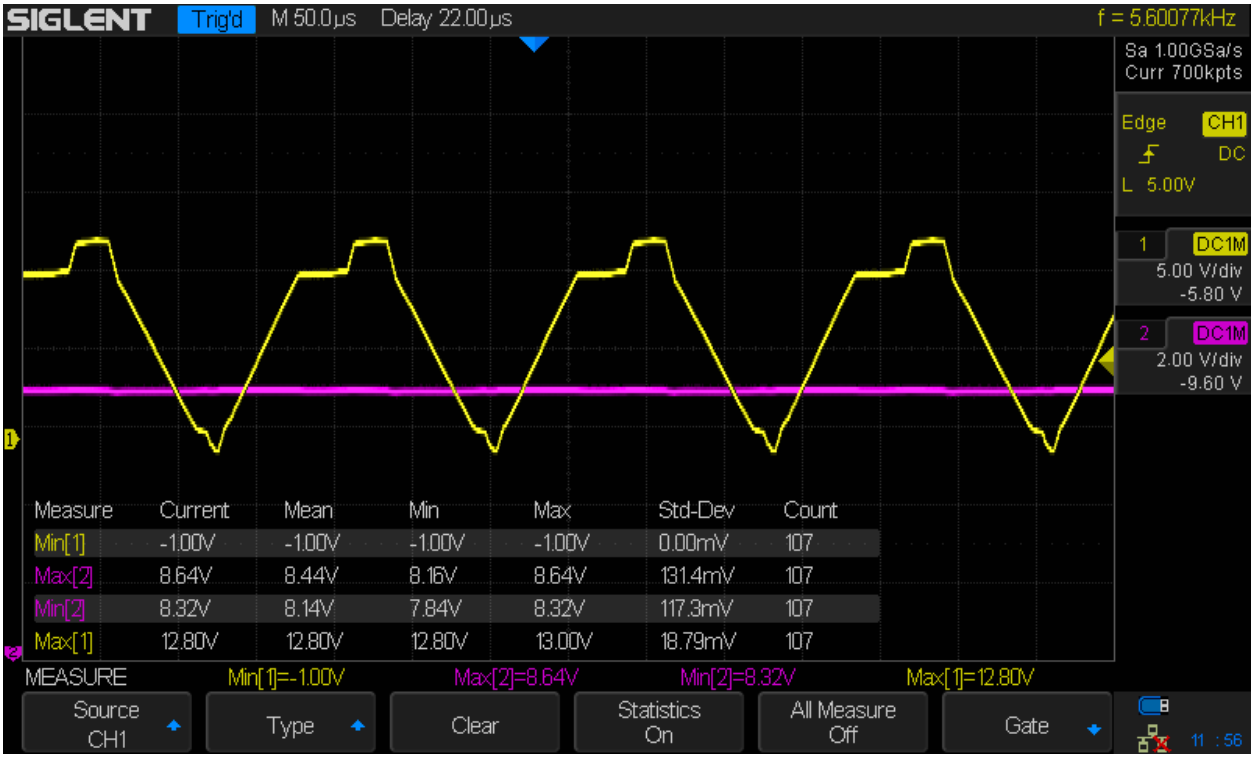


Figure 33: DSO Triangle Wave & Potentiometer Voltage at k = 0.25

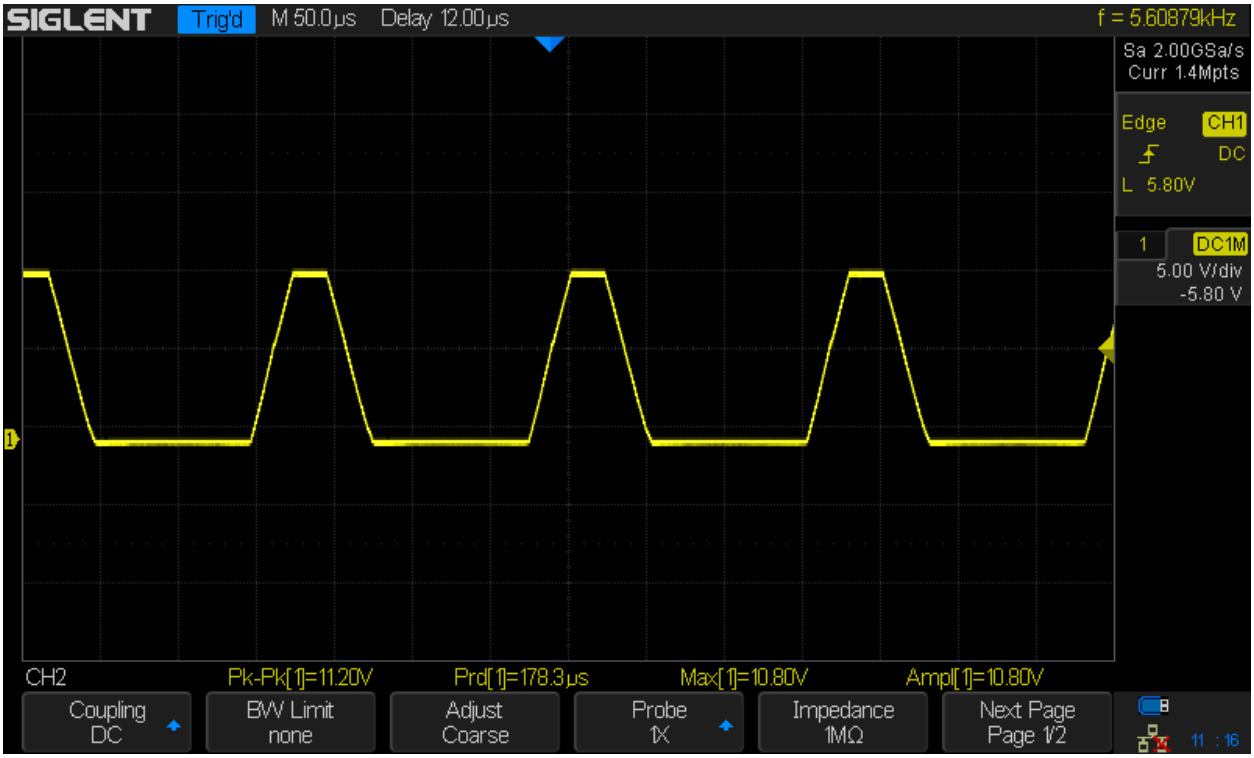


Figure 34: DSO PWM at 25% Duty Cycle

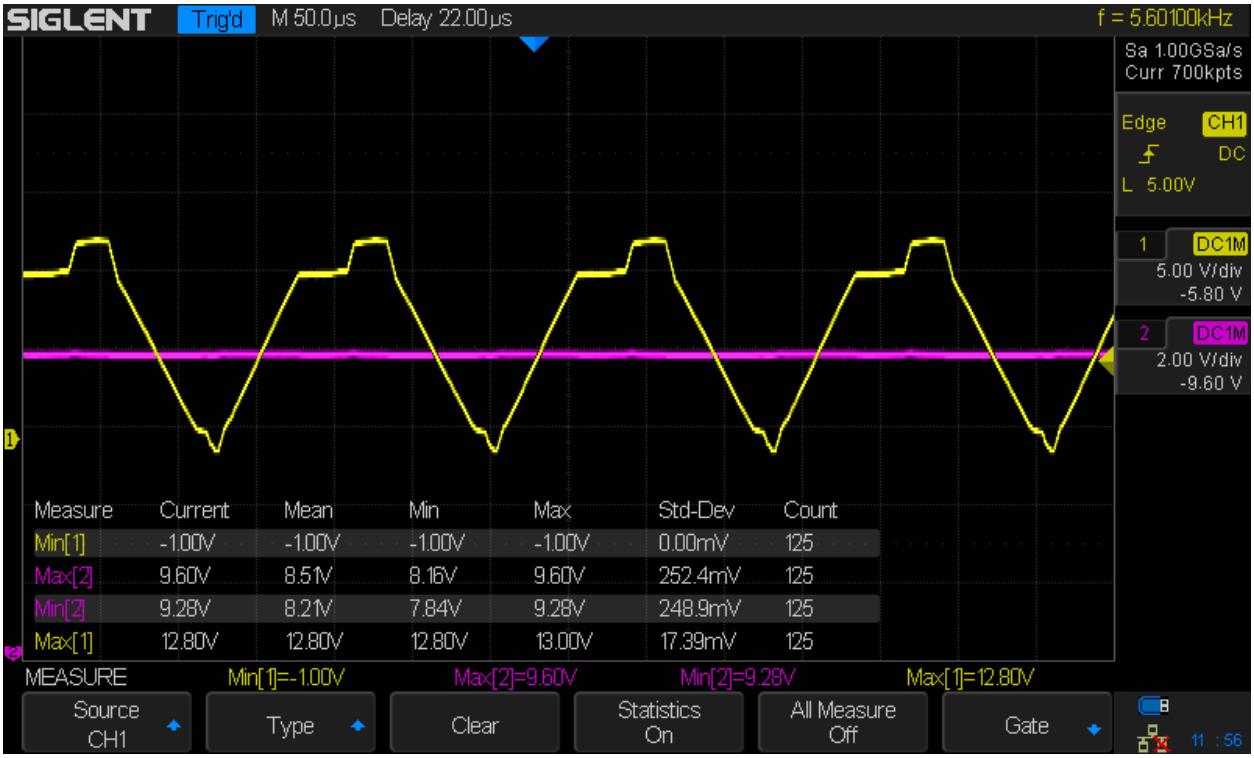


Figure 35: DSO Triangle Wave & Potentiometer Voltage at k = 0.5

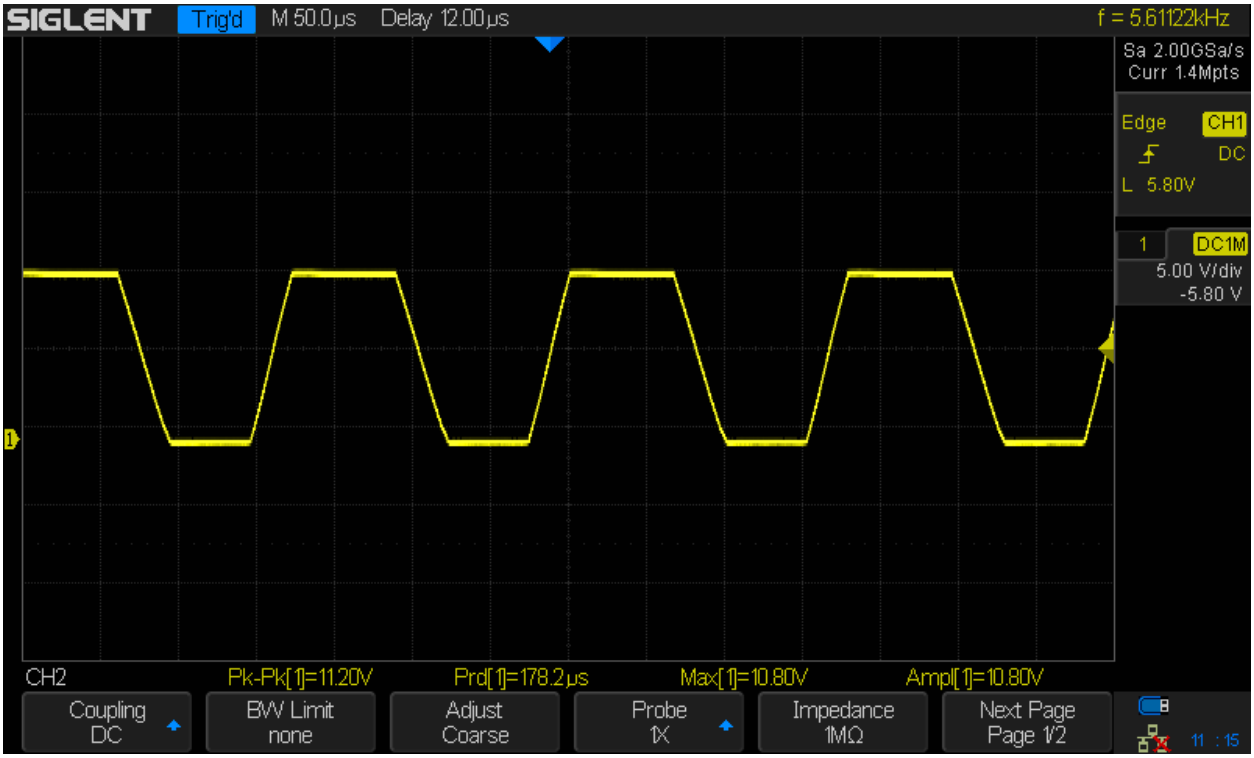


Figure 36: DSO PWM at 50% Duty Cycle

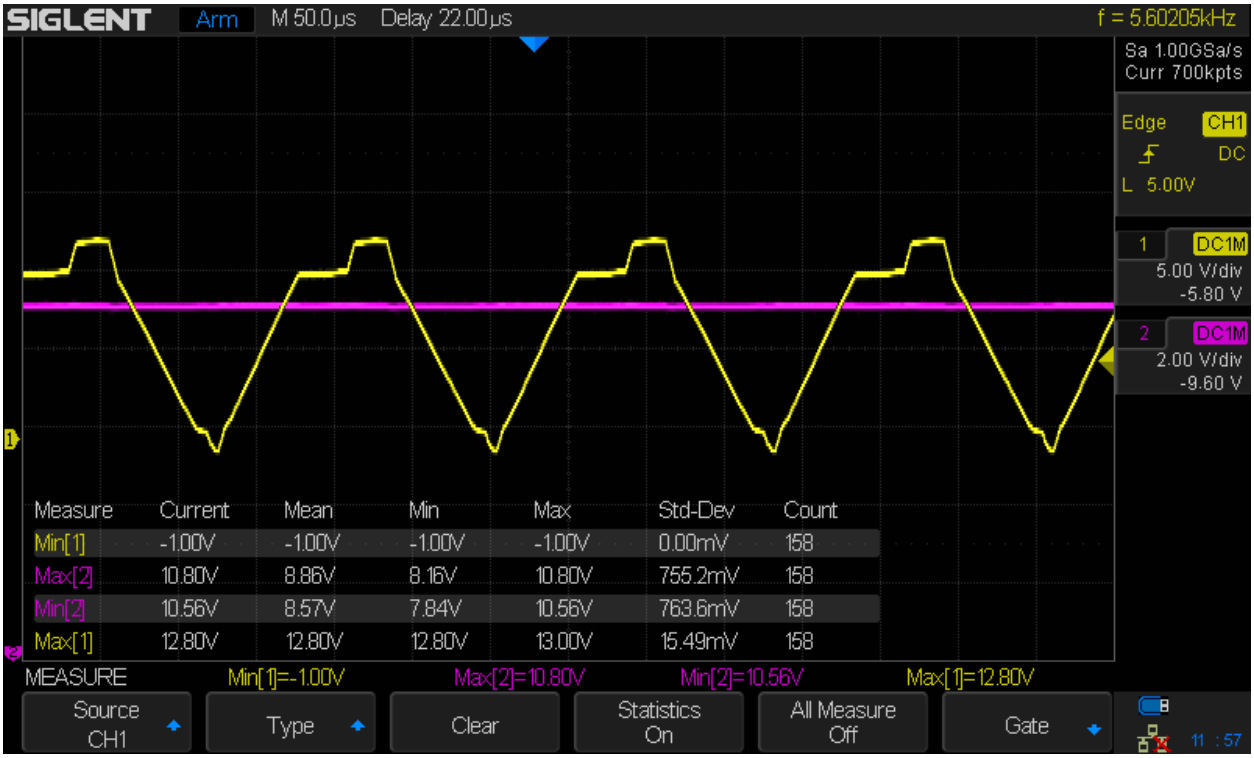


Figure 37: DSO Triangle Wave & Potentiometer Voltage at k = 0.75

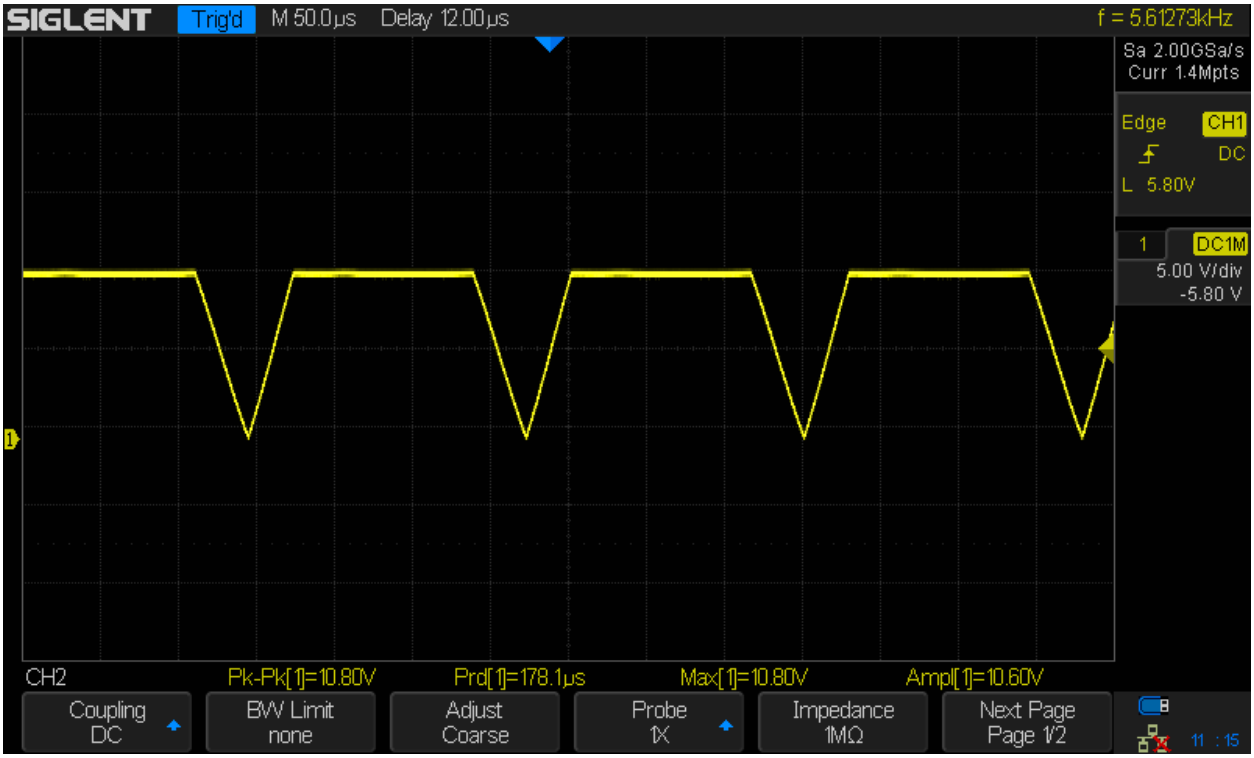


Figure 38: DSO PWM at 75% Duty Cycle

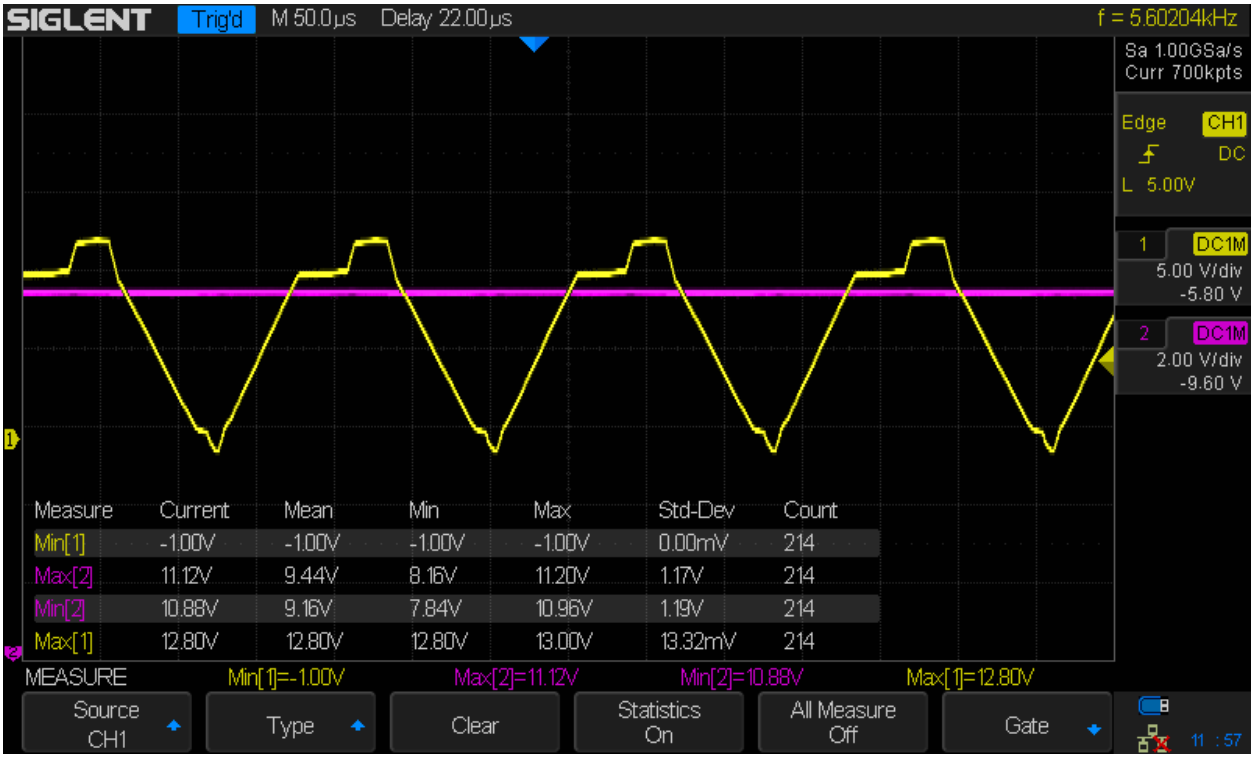


Figure 39: DSO Triangle Wave & Potentiometer Voltage at k = 1

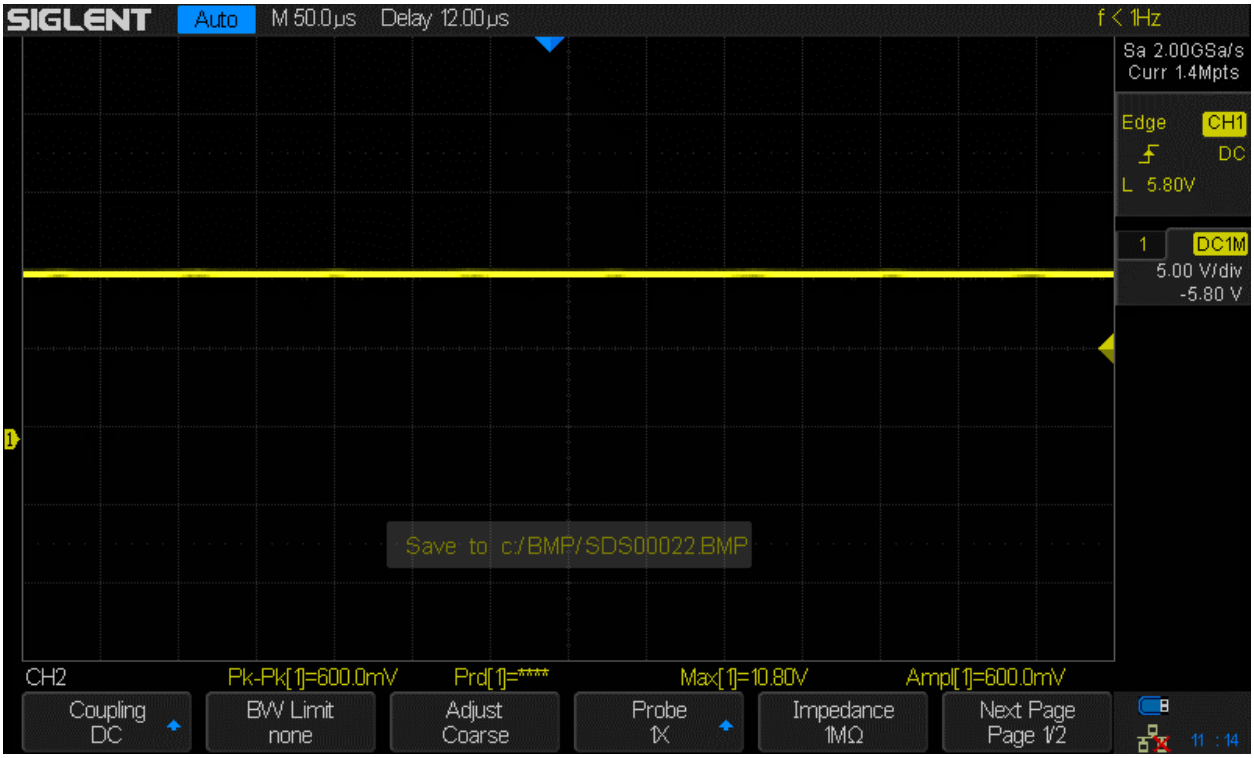


Figure 40: DSO PWM at 100% Duty Cycle

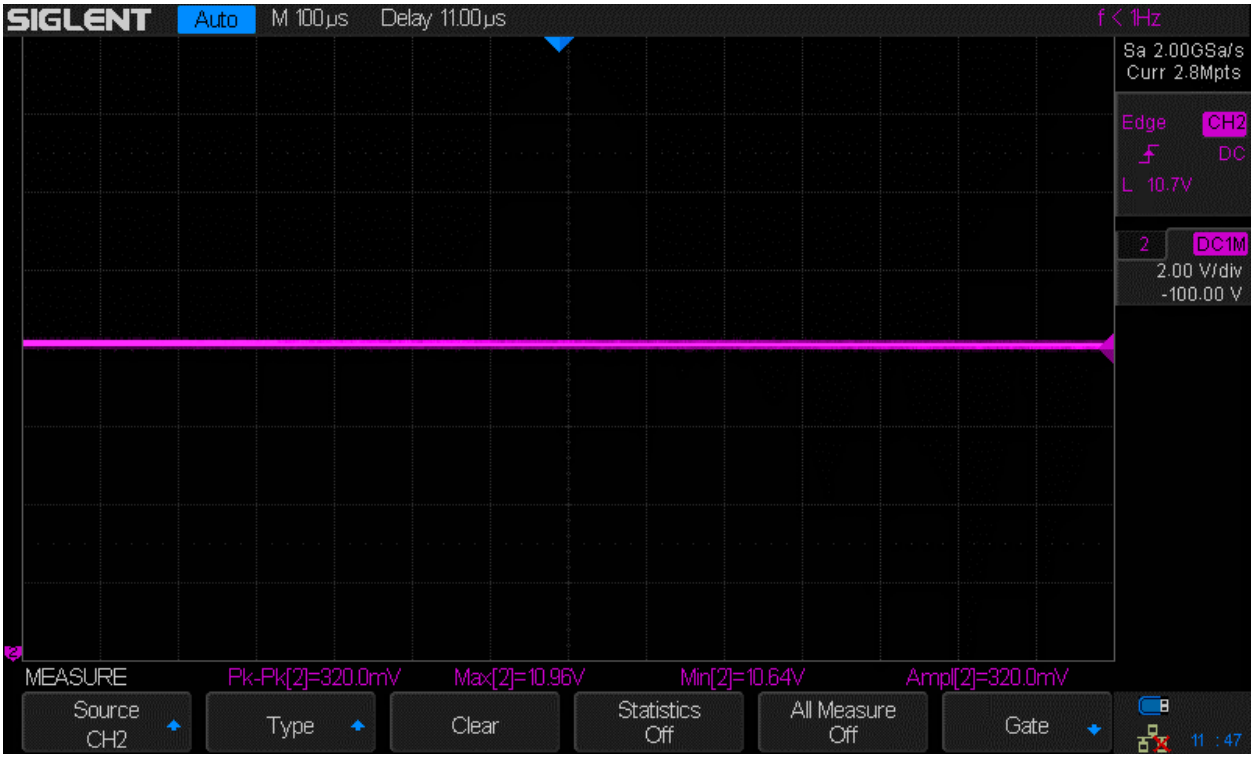


Figure 41: DSO Smoothed Ripple Voltage

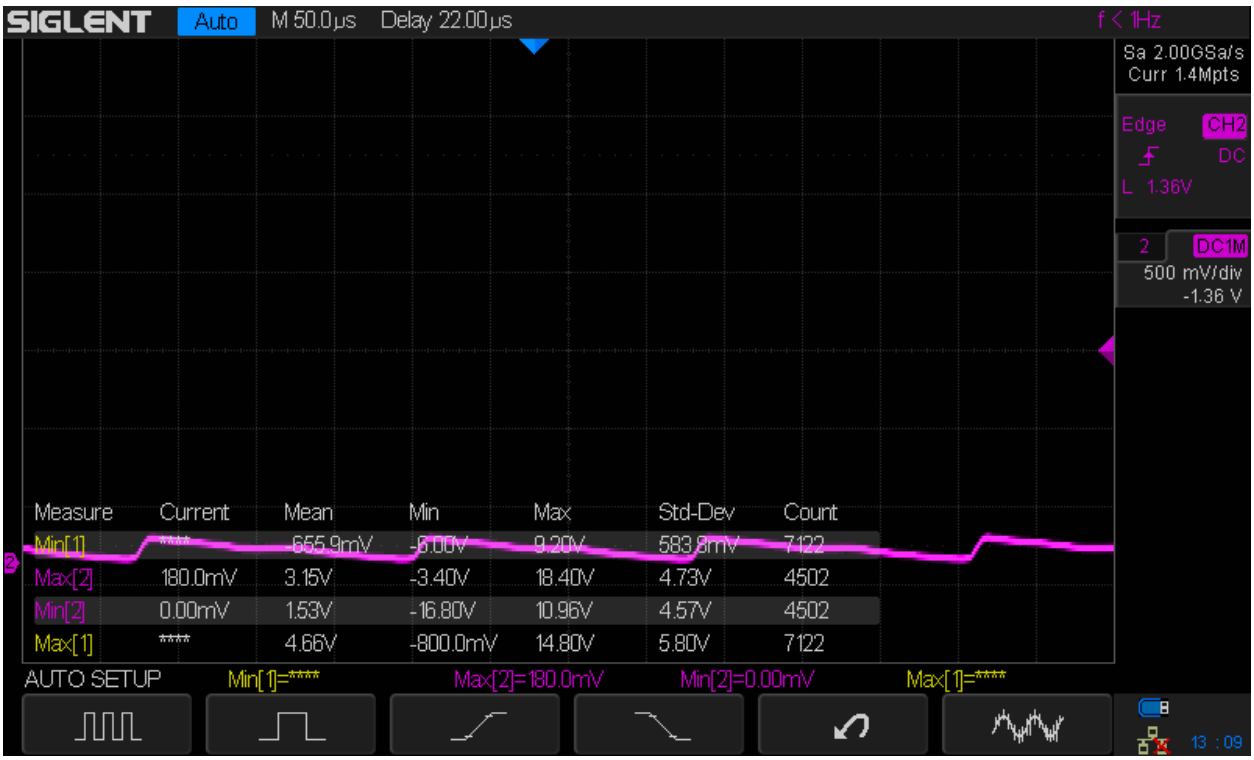


Figure 42: DSO Drain Output at 100% Duty Cycle

Figure 43: DSO Drain Output at 75% Duty Cycle

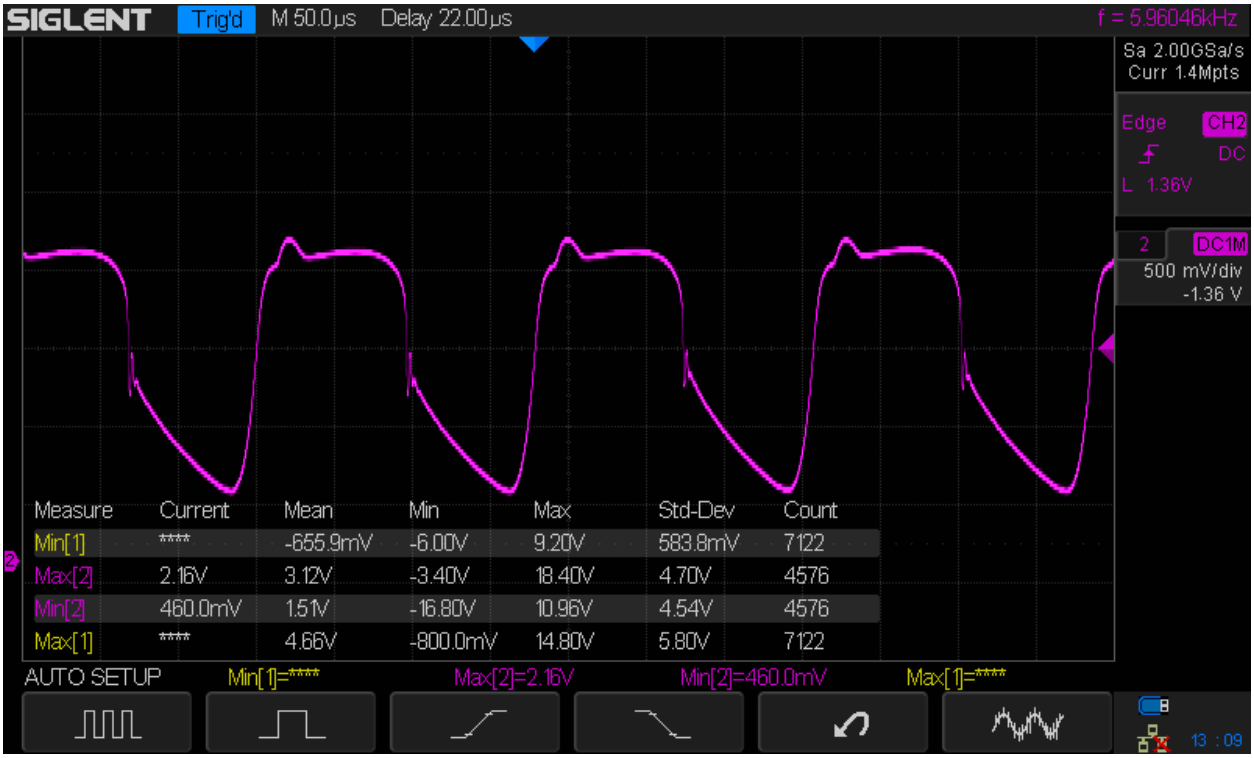


Figure 44: DSO Drain Output at 25% Duty Cycle

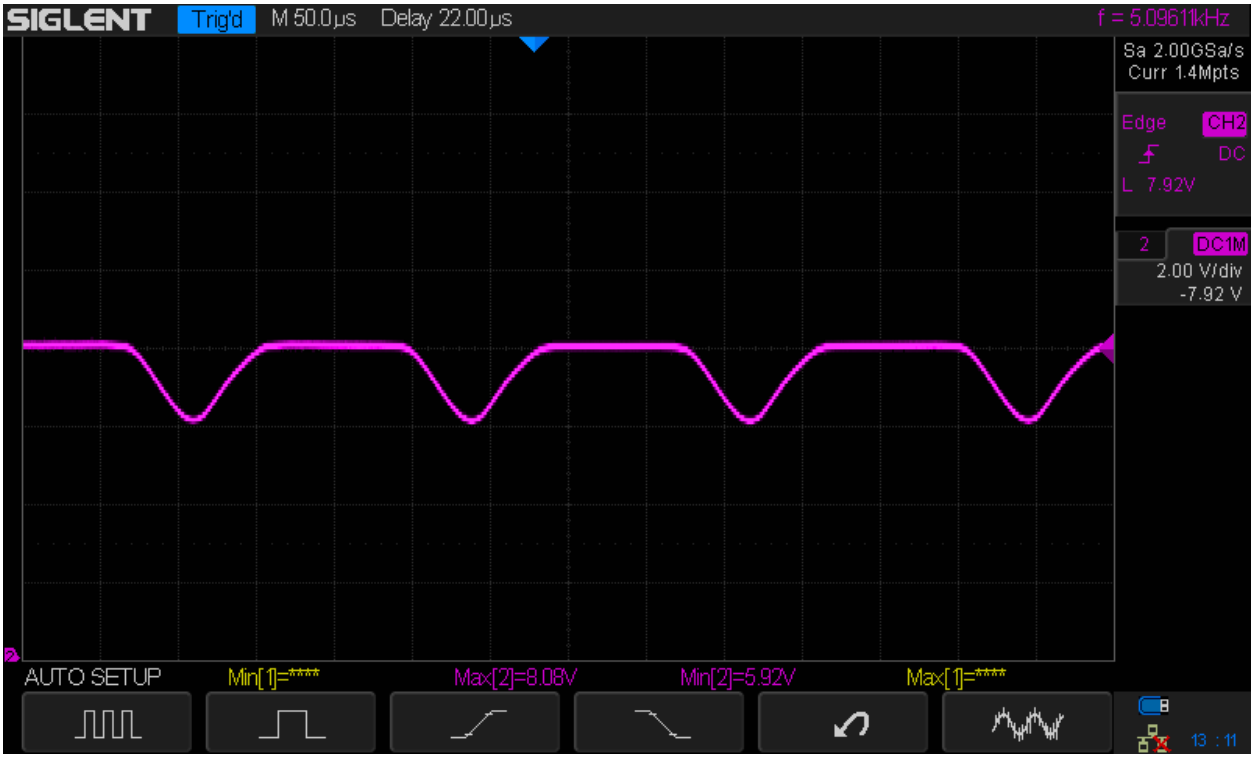


Figure 45: DSO Drain Output at 50% Duty Cycle

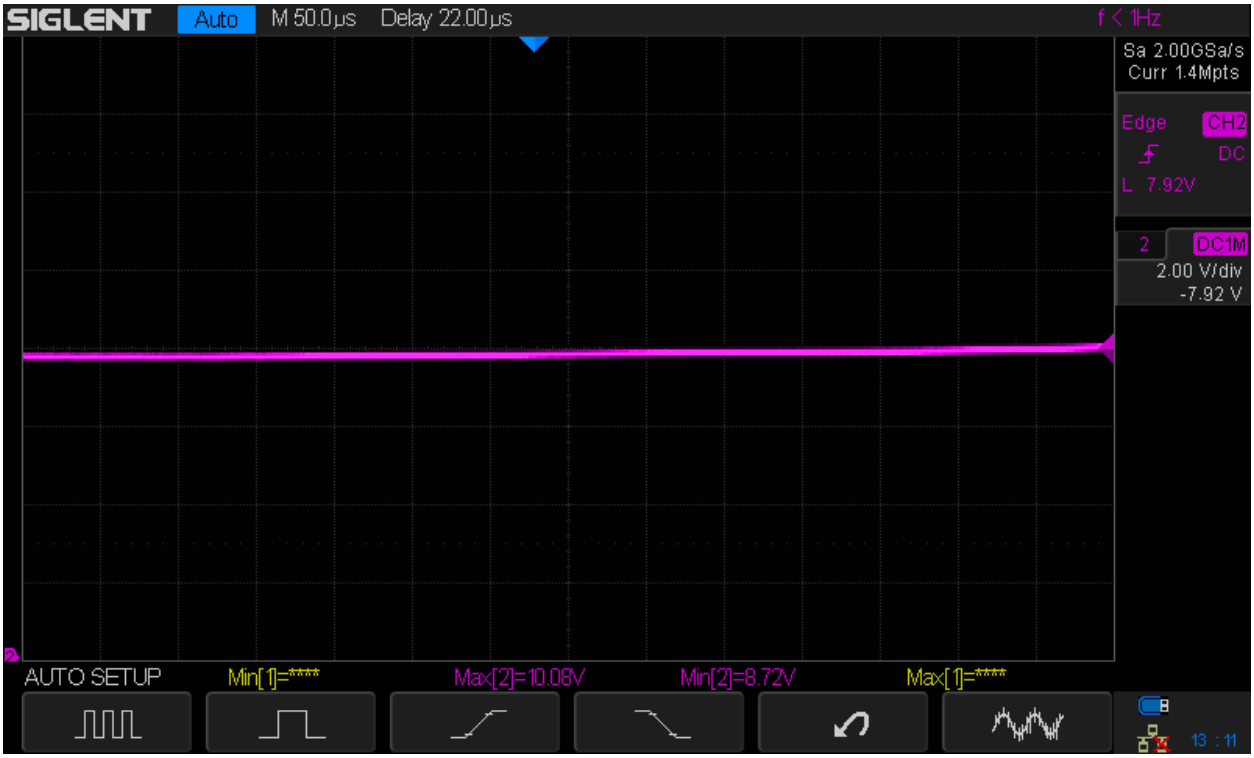


Figure 46: DSO Drain Output at 0% Duty Cycle

As seen in the DSO waveforms above, the expected results are being achieved from the bread board implementation of the circuit. The waveforms are not perfect, especially the misshapen triangle wave which may be due to an incorrect value of capacitance storing the charge in the rising edge of the waveform. Besides this, appropriate PWM waveforms are achieved that resemble 0%, 25%, 50%, 75% and 100% duty cycles. The DC voltage output is achieving a voltage of 10.96V which is enough to power the PC fan. The drain outputs show smoothed versions of the PWM Duty Cycles which is expected of this output. It can be seen that as the PWM Duty Cycle increases, the resultant Duty Cycle of the drain output to the fan is inversed. This is because for the high states of the PWM signal entering the MOSFET's gate pin, the fan connection is short circuited since the gate and drain pins are bridged, and the fan decelerates. The opposite is true for when the PWM signal at the MOSFET's gate pin is low and the drain and source pins are bridged. This causes the fan to accelerate.

As demonstrated in the lab, both the DC motor and DC fan could be connected to the output of this circuit and displayed the acceleration and deceleration properties of adjusting the variable resistance in the potentiometer. As verified by the laboratory instructor, the PC fan and DC motor accelerated when the potentiometer was decreased towards a k value of 0 and decelerated when the potentiometer was increased towards a k value of 1.

Section 7: Bill of Materials

Component	Designator	Value	Description	Supplier	Manufacturer	Quantity	Cost ($)
14pin IC Socket	SKT	-	Socket for 14pin opamps	Jaycar	-	2	0.80
Diode	D	400V 1A	400V 1A ideal diodes	Jaycar	-	4	4.70
Opamp	IC	LM324-N	Quad-Operational Amplifier	Jaycar	Texas Instruments	2	3.50
Optocoupler	OP	4N25	Optocoupler Isolator chip	Jaycar	Texas Instruments	2	1.50
6pin IC socket	SKT	-	Socket for 6pin optocouplers	Jaycar	-	2	0.72
Electrolytic Capacitor	C	220uF	220uF electrolytic capacitor 50V threshold	Jaycar	-	2	1.10
Solder	-	1mm	15g tube of 1mm solder	Jaycar	Duratech	1	1.40

PCB Vero Board	-	95x305mm	95x305mm Vero Board	Jaycar	-	2	25.90
Bipolar green capacitor	C	10uF	10uF green cap bipolar capacitor 50V threshold	Jaycar	-	2	0.60
Desolder braid	-	1.5mm	Desolder braid	Jaycar	GootWick	1	5.95
Solder Sucker	-	-	Solder Sucker	Jaycar	-	1	6.50
Cable pack	W	0.12mm	Frayed wire pack 0.12mm	Jaycar	-	1	5.95
DSO	-	-	Digital Oscilloscope	Griffith University	-	1	-
Transformer	T	240V 50Hz	240V 50Hz Transformer	Griffith University	-	1	-
Breadboard	-	-	Bread board	Griffith University	-	1	-
Potentiometer	VR	100kΩ	100kΩ variable resistor potentiometer	Griffith University	-	1	-
MOSFET	MOSFET	V_{DSS} 55V $R_{DS(on)}$ 0.022Ω I_D 47A	HEXFET Power MOSFET	Griffith University	Texas Instruments	1	-
PWM PC Fan	-	12V 15-25Hz 20mA	Corsair PWM Pc fan	Umart	Corsair	1	-
Resistor	R	50kΩ	50kΩ resistor	Griffith University	-	2	-
Resistor	R	40kΩ	40kΩ resistor	Griffith University	-	1	-
Resistor	R	35kΩ	35kΩ resistor	Griffith University	-	1	-

Resistor	R	900Ω	900Ω resistor	Griffith University	-	1	-
Resistor	R	8kΩ	8kΩ resistor	Griffith University	-	1	-
Resistor	R	5kΩ	5kΩ resistor	Griffith University	-	1	-
Resistor	R	100kΩ	100kΩ resistor	Griffith University	-	1	-
Resistor	R	1kΩ	1kΩ resistor	Griffith University	-	3	-
Resistor	R	10kΩ	10kΩ resistor	Griffith University	-	1	-
Resistor	R	100Ω	100Ω resistor	Griffith University	--	1	-
	Total Cost						58.62

Appendix:

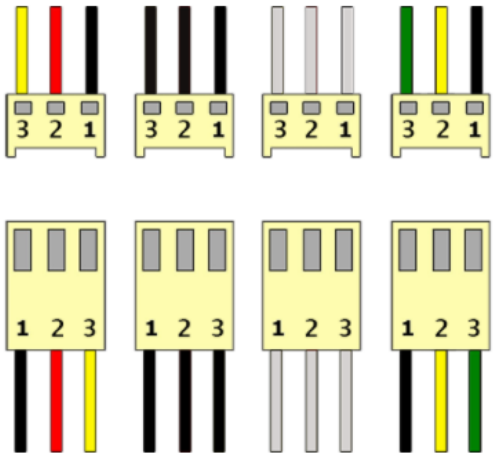
Appendix i: PWM controlled PC fan pin layout

https://landing.coolermaster.com/faq/3-pin-and-4-pin-fan-wire-diagrams/

3 pin and 4 pin Fan Wire Diagrams

3 pin Fan Connections

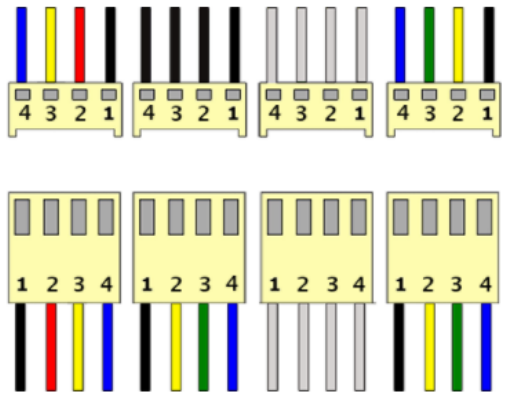
*cable coloring varies from fan to fan



Pin	Name	Color	Color	Color	Color
1	Ground	Black	Black	Gray	Black
2	+12v	Red	Black	Gray	Yellow
3	Tach/Signal/Sense	Yellow	Black	Gray	Green

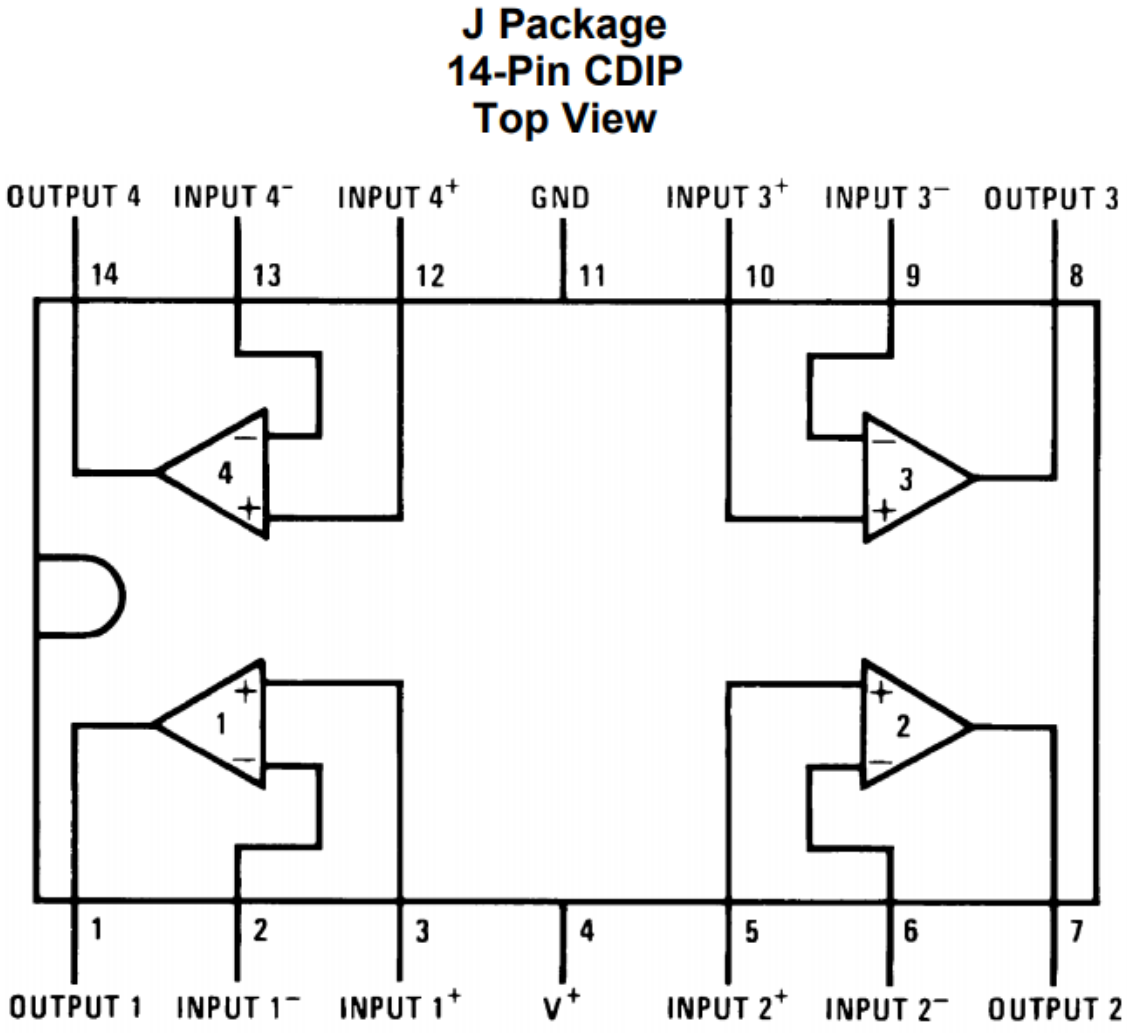
4 pin Fan Connections

*cable coloring varies from fan to fan

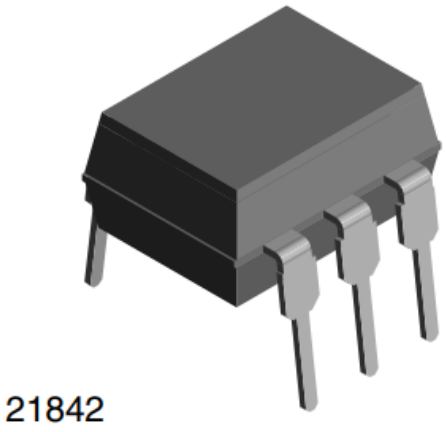


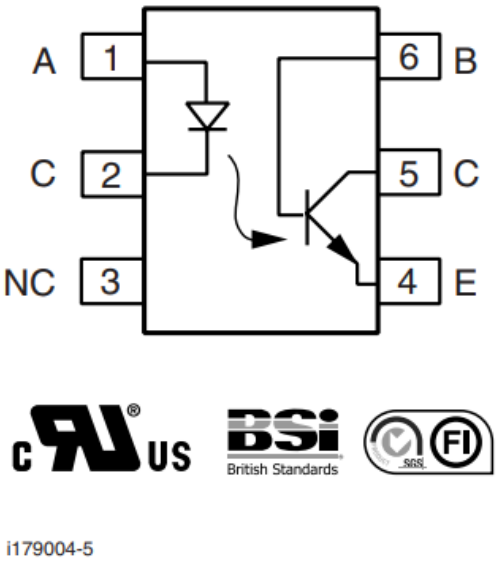
Pin	Name	Color	Color	Color	Color
1	Ground	Black	Black	Gray	Black
2	+12v	Red	Black	Gray	Yellow
3	Tach/Signal/Sense	Yellow	Black	Gray	Green
4	Control/PWM	Blue	Black	Gray	Blue

Appendix ii: Opamp pin layout

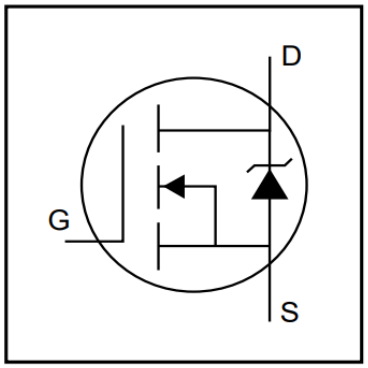


Appendix iii: 4N25 pin layout





Appendix iv: IRLZ44N MOSFET pin layout



V_{DSS} = 55V

$R_{DS(on)}$ = 0.022Ω

I_D = 47A