

[01] - COVER PAGE.SchDoc  
[01] - COVER PAGE.SchDoc

[02] - BLOCK DIAGRAM.SchDoc  
[02] - BLOCK DIAGRAM.SchDoc

[03] - CONNECTORS\_1.SchDoc  
[03] - CONNECTORS\_1.SchDoc

[04] - CONNECTORS\_2.SchDoc  
[04] - CONNECTORS\_2.SchDoc

[05] - DAC.SchDoc  
[05] - DAC.SchDoc

[06] - ADC.SchDoc  
[06] - ADC.SchDoc

[07] - Power\_Stage.SchDoc  
[07] - Power\_Stage.SchDoc

[08] - REVISION HISTORY.SchDoc  
[08] - REVISION HISTORY.SchDoc

# TEMPLATE NOTES

## Set Project Parameters

- 1) Go to Project -> Project Options -> Parameters
- 2) Set Company, Project and VersionRevision

Mark Not Fitted Components as  
**NF**

## Net Class Example



## Differential signal example

TITLE Examples (You can change the color to reflect your company color)

# PAGE TITLE

*Peripheral / Group of component title*

*Smaller Title*

## Schematic Status Explanation

- DRAFT** - Very early stage of schematic, ignore details.
- PRELIMINARY** - Close to final schematic.
- CHECKED** - There should not be any mistakes. Tell the engineer if you find one.
- RELEASED** - A board with this schematic has been sent to production.



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Title: FPGA_Interface_Baseboard		Variant: [No Variations]	
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Size:	DWG NO		Revision: v3.0
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# FPGA\_Interface\_Baseboard

## Variant: [No Variations]

28/06/2019  
v3.0

CHECKED 05-JUN-2019

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### DESIGN CONSIDERATIONS

DESIGN NOTE:  
Example text for informational  
design notes.

DESIGN NOTE:  
Example text for cautionary  
design notes.

DESIGN NOTE:  
Example text for debug notes.

DESIGN NOTE:  
Example text for critical  
design notes.

LAYOUT NOTE:  
Example text for critical  
layout guidelines.

Cannot open file S:\FEDEVEL\iMX6 Rex Development Baseboard\Docs\iMX6 Rex  
Development bb - top view.jpg

TOP VIEW

BOTTOM VIEW

Cannot open file S:\FEDEVEL\iMX6 Rex Development Baseboard\Docs\iMX6 Rex  
Development bb - bottom view.jpg



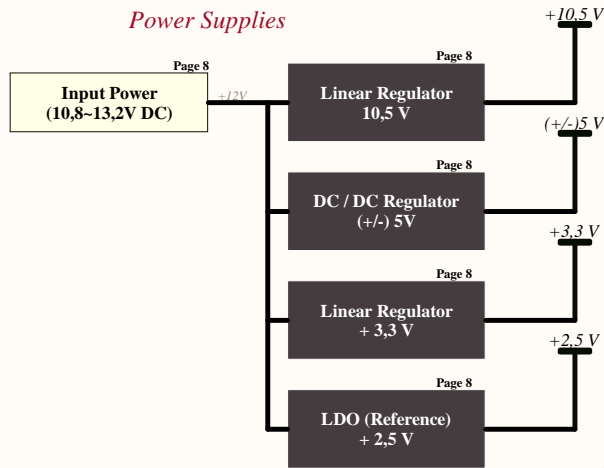
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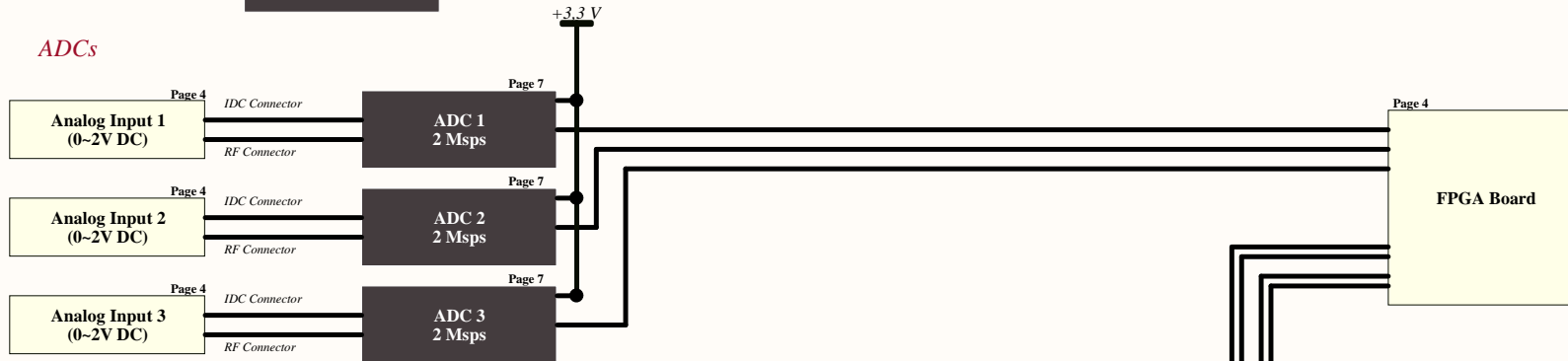
# FPGA\_Interface\_Baseboard

## (Block Diagram)

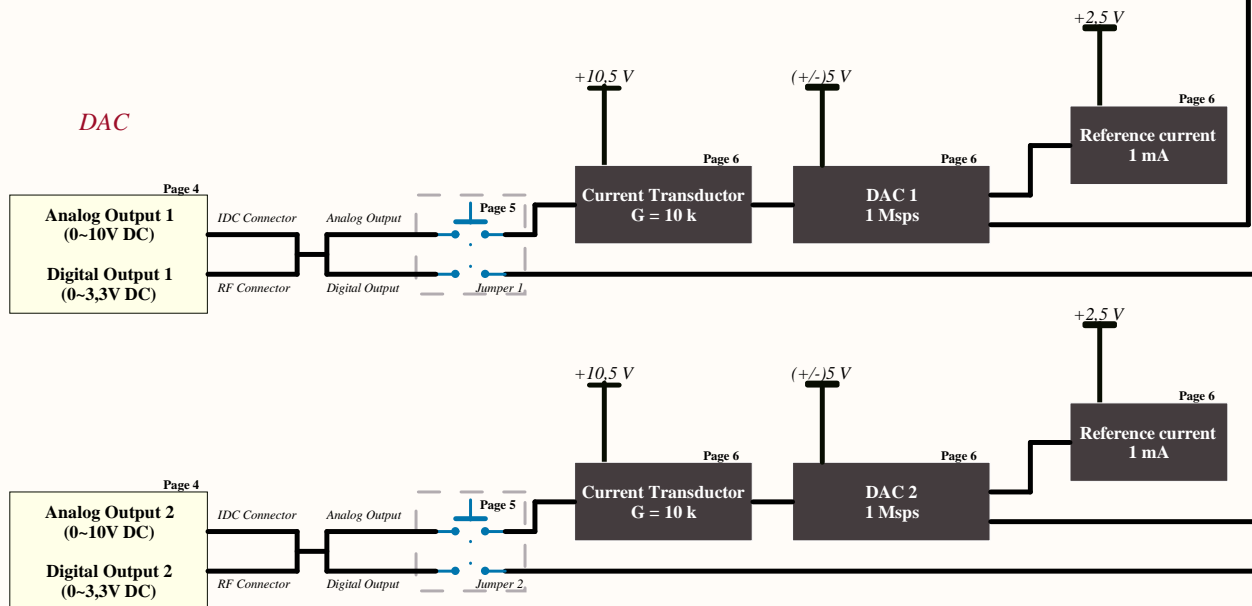
### Power Supplies



### ADCs



### DAC

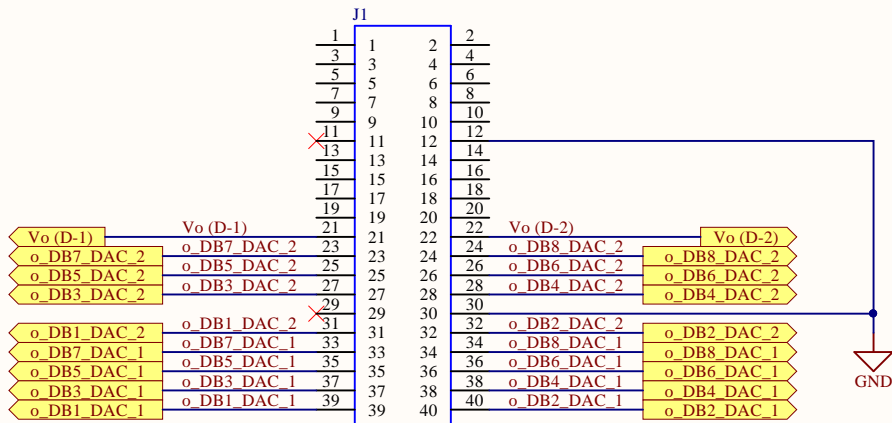


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# CONNECTORS

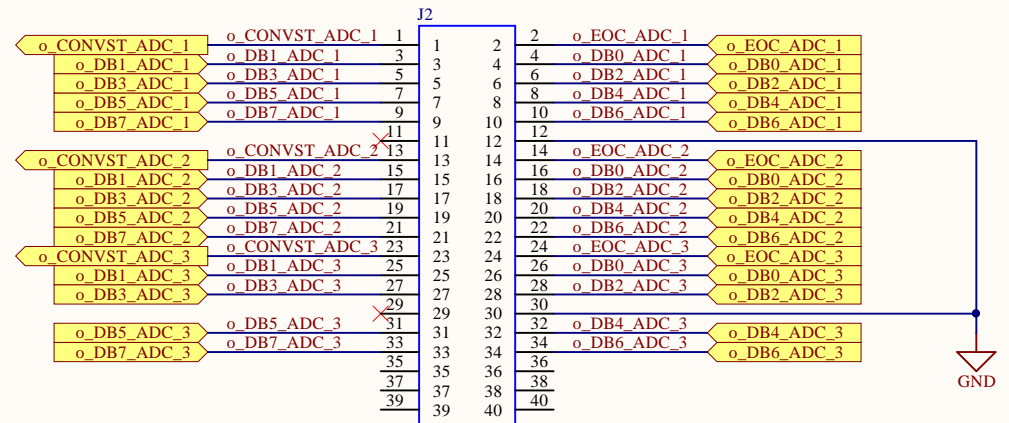
## DAC Digital signals



IDC connector

LAYOUT NOTE:  
Taces shall be the same length.

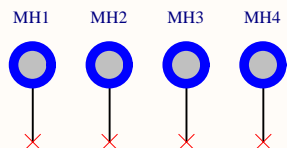
## ADC Digital signals



IDC connector

LAYOUT NOTE:  
Taces shall be the same length.

## Mechanical Board Mounting Holes

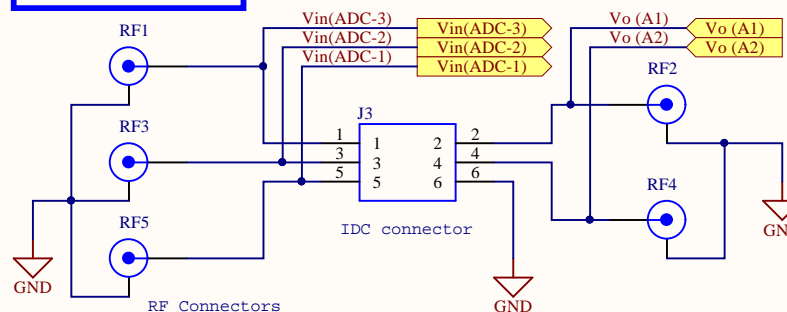


Mounting holes 7.4mm pad 3.2mm drill

BOARD MOUNTING HOLES  
ONE IN EACH CORNER

LAYOUT NOTE:  
- Place connectors as  
near as possible to ADC  
Analog Input pin and  
DAC Analog Output pin.

## DAC & ADC Analog signals



IDC connector

RF Connectors



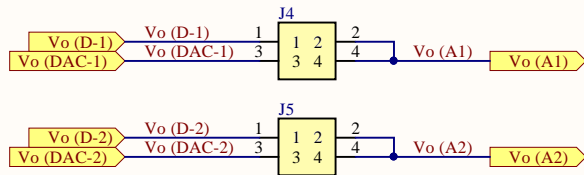
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# CONNECTORS

## DAC

### *Jumpers*



DESIGN NOTE:  
Option (1-2) -> DAC Analog Output  
Option (3-4) -> FPGA/Microcontroller Digital Output  
Objective -> Activate Mosfets Drivers.

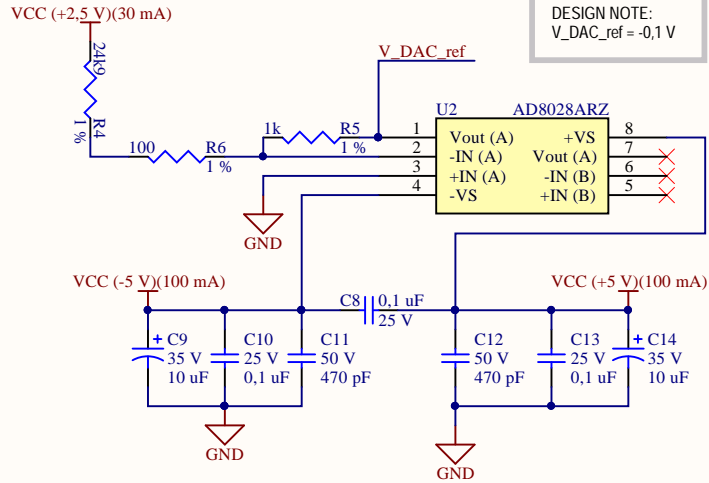


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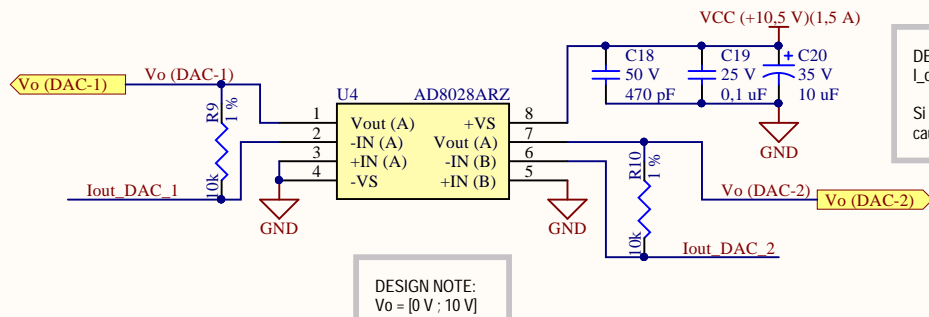
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# DAC

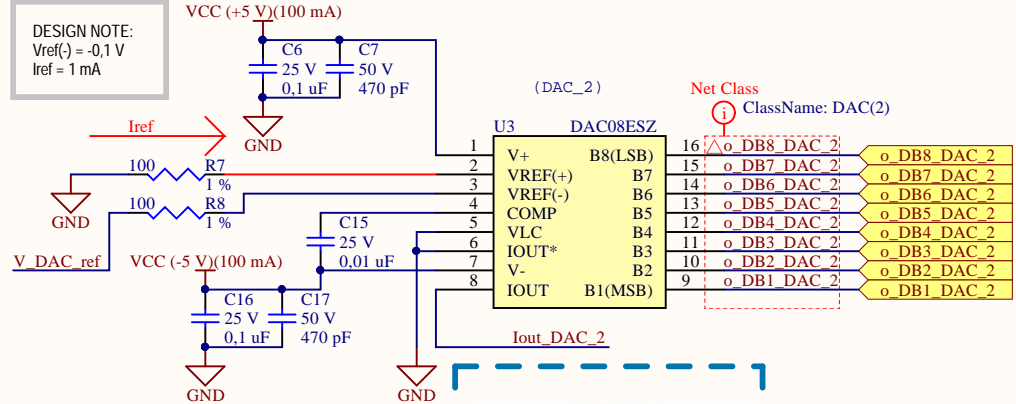
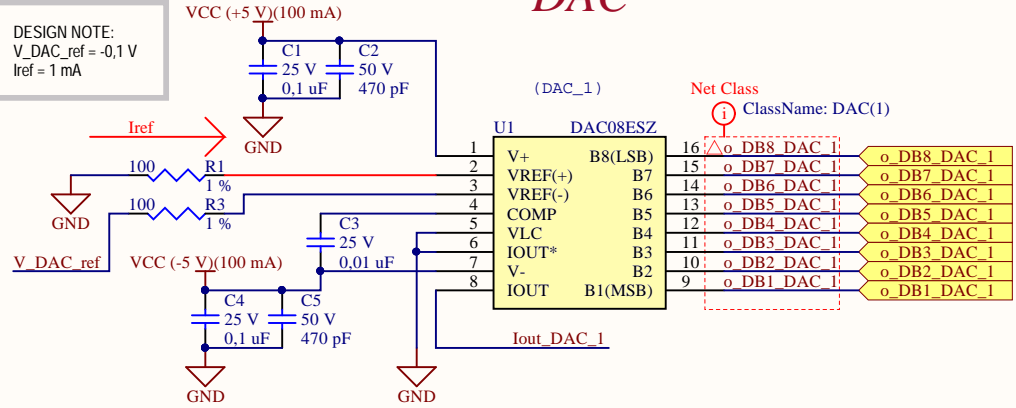
## DAC Voltage reference



## DAC Current Transducer



DESIGN NOTE:  
V\_DAC\_ref = -0,1 V  
Iref = 1 mA

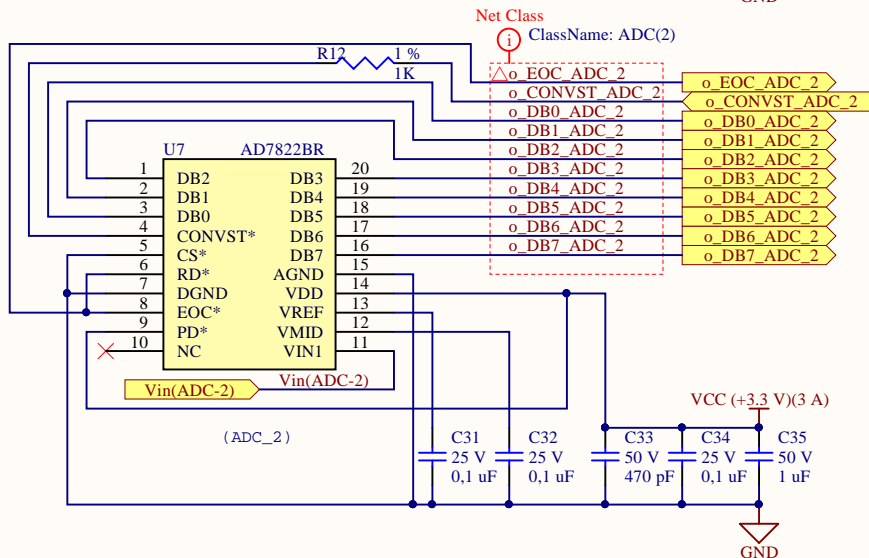
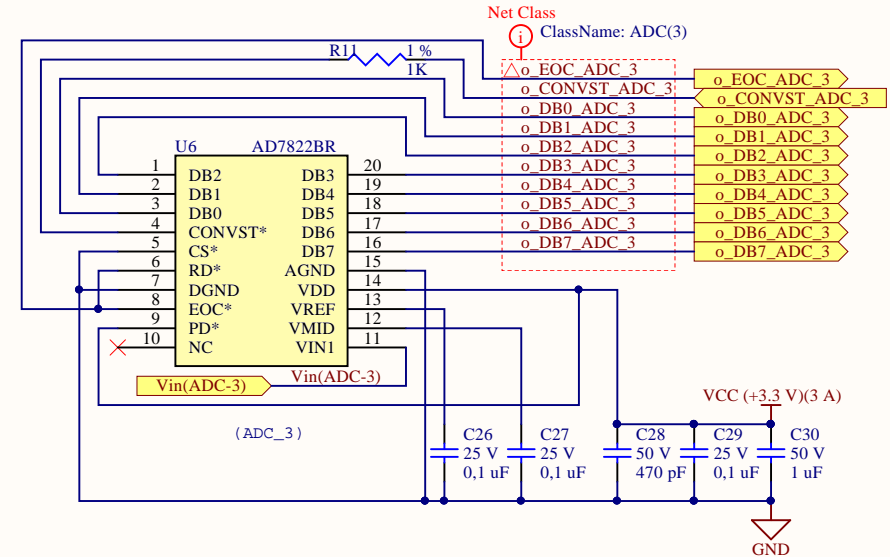
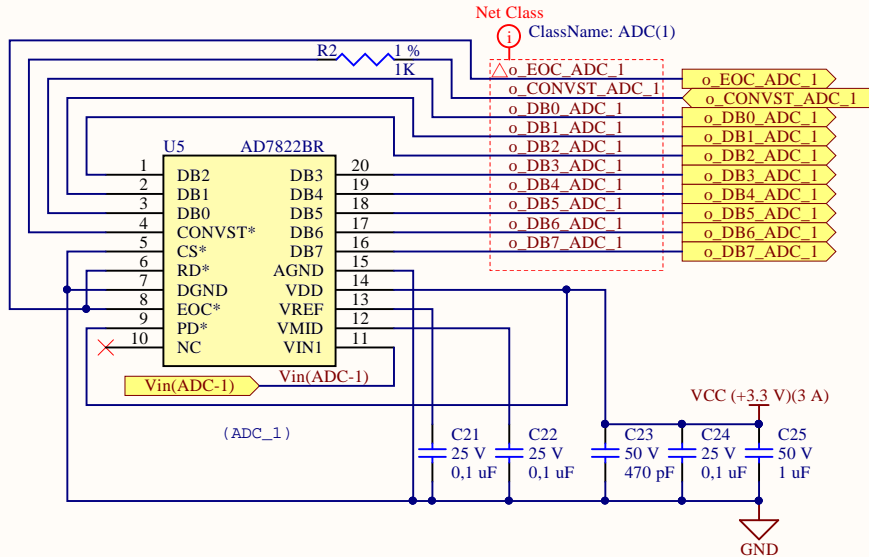


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# ADC

## ADC



DESIGN NOTE:  
For all ADC ->

Vin = [0 V ; 2 V]

LAYOUT NOTE:  
- Make separate return paths for  
DGND (Digital Ground) and AGND  
(Analog Ground).

DGND -> PIN 7  
AGND -> PIN 15

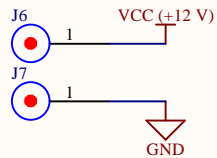


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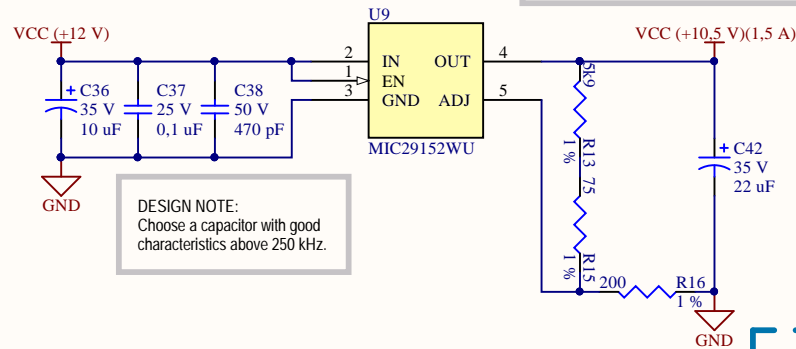
# Power Supplies

## VCC Input



DESIGN NOTE:  
Vin = [10,8 V ; 13,2 V]

## 10,5 V Voltage Regulator



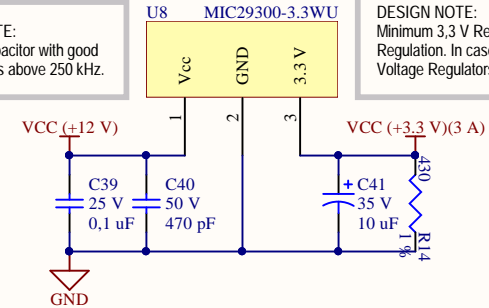
DESIGN NOTE:  
Choose a capacitor with good characteristics above 250 kHz.

DESIGN NOTE:  
Minimum 10,5 V Regulator Load to Enable Voltage Regulation. In case of < 5 mA current Load, the Voltage Regulators doesn't regulate the output.

$$(R35+R37) = R36 * (Vout/1.240 - 1)$$

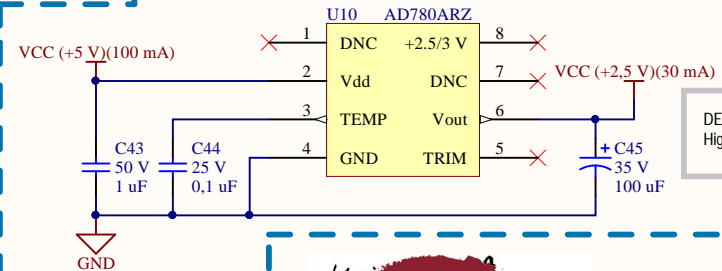
## 3,3 V Voltage Regulator

DESIGN NOTE:  
Choose a capacitor with good characteristics above 250 kHz.



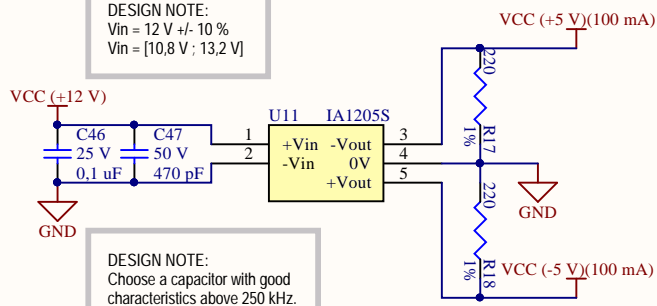
DESIGN NOTE:  
Minimum 3,3 V Regulator Load to Enable Voltage Regulation. In case of < 7 mA current Load, the Voltage Regulators doesn't regulate the output.

## 2,5 V Voltage Precision Reference



DESIGN NOTE:  
High Precision 2,5 V reference.

## (+/-)5 V DC/DC Converter



DESIGN NOTE:  
Vin = 12 V +/- 10 %  
Vin = [10,8 V ; 13,2 V]

DESIGN NOTE:  
Choose a capacitor with good characteristics above 250 kHz.

DESIGN NOTE:  
Line Regulation = 1.2%/1% ΔVin  
Load Regulation = 10% (20-100% load change)  
Setpoint Accuracy = ±3%  
Maximum Capacitive Load = ±100 μF  
Switching Frequency = Variable, 80 KHz typical  
Efficiency = 75%


DESIGN NOTE:  
Minimum 5 V Regulator Load to Enable Voltage Regulation. In case of < 20 mA current Load, the Voltage Regulators doesn't regulate the output.



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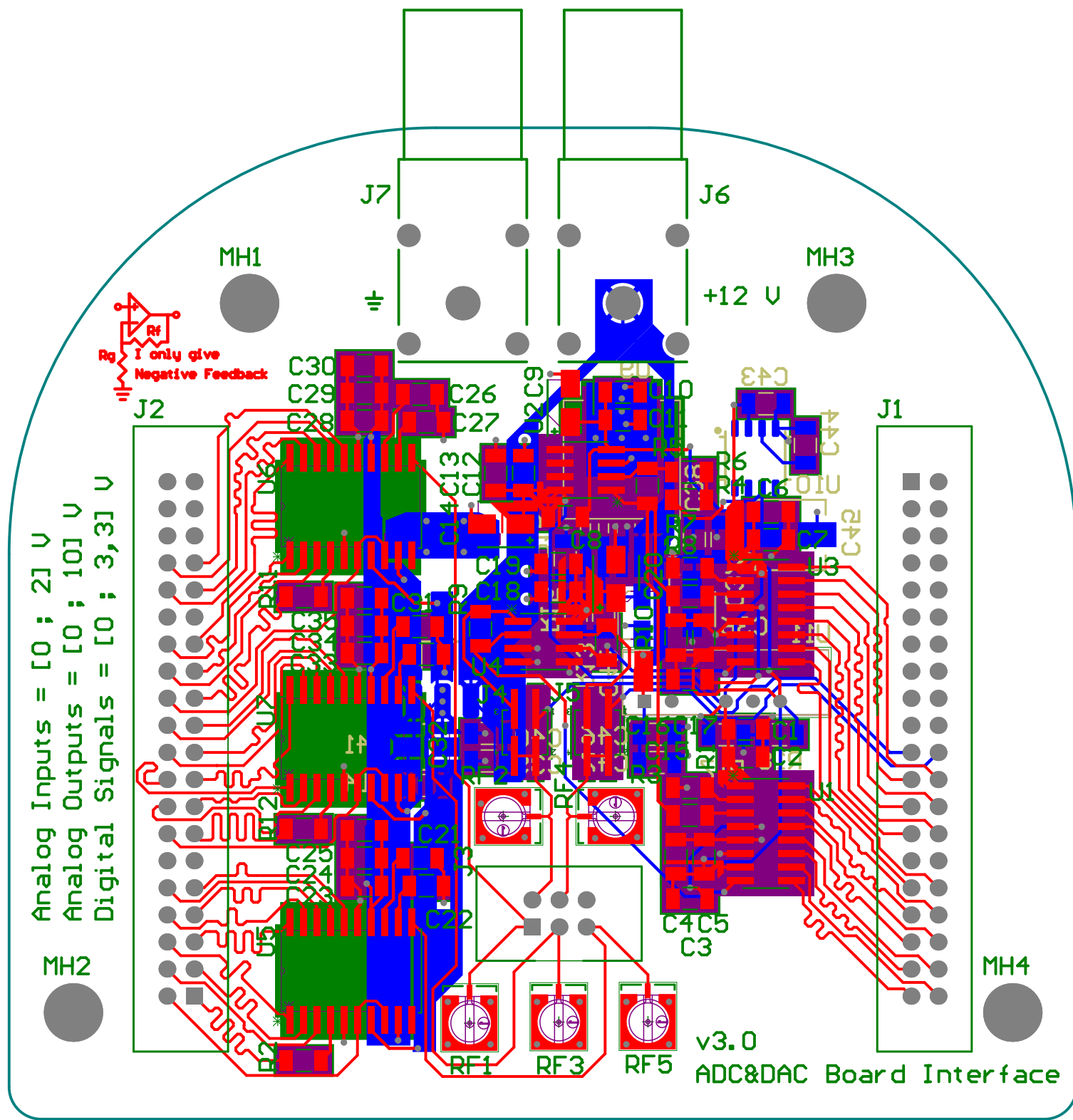


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A	<div>REVISION HISTORY</div>							A																				
B								B																				
C								C																				
D	<div><div><div>Universitat Rovira i Virgili <a href="http://www.urv.cat/es/">www.urv.cat/es/</a></div></div><table><tr><td colspan="2">URV</td><td colspan="2">CONFIDENTAL. Do not distribute.</td></tr><tr><td>Title:</td><td>FPGA_Interface_Baseboard</td><td colspan="2">Variant: [No Variations]</td></tr><tr><td colspan="2">Page Contents:</td><td>[08] - REVISION HISTORY.SchDoc</td><td>Jesús Fuente Porta</td></tr><tr><td>Size:</td><td>A3</td><td>DWG NO</td><td>Revision: v3.0</td></tr><tr><td>Date:</td><td colspan="2">28/06/2019</td><td>Sheet 9 of 9</td></tr></table></div>							URV		CONFIDENTAL. Do not distribute.		Title:	FPGA_Interface_Baseboard	Variant: [No Variations]		Page Contents:		[08] - REVISION HISTORY.SchDoc	Jesús Fuente Porta	Size:	A3	DWG NO	Revision: v3.0	Date:	28/06/2019		Sheet 9 of 9	D
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Analog Inputs = [0 ; 2] V  
Analog Outputs = [0 ; 10] V  
Digital Signals = [0 ; 3,3] V

$R_g$   
I only give  
Negative Feedback

+12 V

v3.0  
ADC&DAC Board Interface

[illegible]