Advance Information

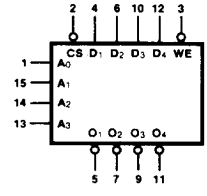
SN54LS189/SN74LS189

64-BIT RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS

DESCRIPTION — The 54LS/74LS189 is a high-speed, low-power 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high-impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

- **3-STATE OUTPUTS FOR DATA BUS APPLICATIONS**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**
- **LOW POWER SCHOTTKY DESIGN MINIMIZES POWER CONSUMPTION**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

AN	Address Input
$\overline{CS}$	Chip Select (active LOW) Input
D_n	Data Input
$\overline{O}_n$	Data (inverted) Output
$\overline{WE}$	Write Enable (active LOW) Input

FUNCTION TABLE

INPUTS $\overline{CS}$	INPUTS $\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	H	Write	HIGH Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	HIGH Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial