Configuración de las funciones de los pines del LPC4088

Diseño Basado en Microprocesadores

Víctor Manuel Sánchez Corbacho

Dpto. de Automática, Electrónica, Arquitectura y Redes de Computadores

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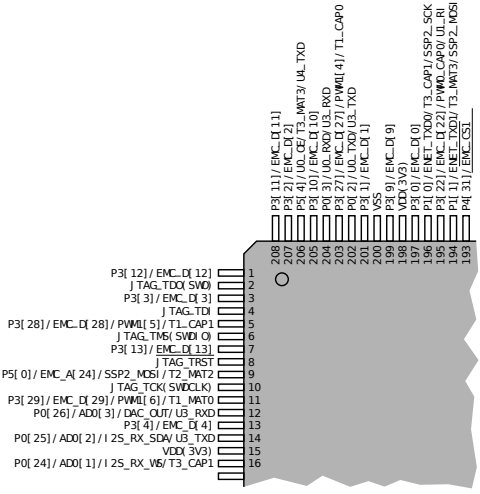
Contenido

Introducción



- En los μC hay varias funciones multiplexadas sobre cada pin de E/S.
- La función por defecto suele ser GPIO.
- Pero pueden asignarse otras funciones alternativas a cada uno.

Introducción

- En el LPC4088 cada patilla de E/S puede asumir hasta 8 funciones diferentes.
- La configuración de cada pin está controlada por un registro `IOCON` propio.

Table 75. Summary of I/O pin configuration registers

Port	Registers	Detail Table
Port 0 pins	IOCON_P0_nn, where nn is the port pin number, from 0 to 31 [1]	Table 76
Port 1 pins	IOCON_P1_nn, where nn is the port pin number, from 0 to 31 [1]	Table 77
Port 2 pins	IOCON_P2_nn, where nn is the port pin number, from 0 to 31 [1]	Table 78
Port 3 pins	IOCON_P3_nn, where nn is the port pin number, from 0 to 31 [1]	Table 79
Port 4 pins	IOCON_P4_nn, where nn is the port pin number, from 0 to 31 [1]	Table 80
Port 5 pins	IOCON_P5_nn, where nn is the port pin number, from 0 to 4 [1]	Table 81

[1] Which pins are available depends on the part number and package combination.

- Los registros `IOCON` también controlan:
  - Activación de resistencias de pull-up o pull-down internas.
  - Modo de salida en drenador abierto.
  - Habilitación de histéresis de entrada.
  - Control de slew rate de salida.
  - Activación de funciones analógicas.
  - Modo I^2C.

Registros IOCON de los pines del puerto 0

Table 76. I/O Control registers for port 0

Port pin	Register	Access	Reset Value[1]	Address	IOCON type[2]	208-pin	180-pin	144-pin	80-pin
P0[0]	IOCON_P0_00	R/W	0x030	0x4002 C000	D (tables 82, 83)	x	x	x	x
P0[1]	IOCON_P0_01	R/W	0x030	0x4002 C004	D (tables 82, 83)	x	x	x	x
P0[2]	IOCON_P0_02	R/W	0x030	0x4002 C008	D (tables 82, 83)	x	x	x	x
P0[3]	IOCON_P0_03	R/W	0x030	0x4002 C00C	D (tables 82, 83)	x	x	x	x
P0[4]	IOCON_P0_04	R/W	0x030	0x4002 C010	D (tables 82, 83)	x	x	x	-
P0[5]	IOCON_P0_05	R/W	0x030	0x4002 C014	D (tables 82, 83)	x	x	x	-
P0[6]	IOCON_P0_06	R/W	0x030	0x4002 C018	D (tables 82, 83)	x	x	x	x
P0[7]	IOCON_P0_07	R/W	0x0A0	0x4002 C01C	W (tables 90, 91)	x	x	x	x
P0[8]	IOCON_P0_08	R/W	0x0A0	0x4002 C020	W (tables 90, 91)	x	x	x	x
P0[9]	IOCON_P0_09	R/W	0x0A0	0x4002 C024	W (tables 90, 91)	x	x	x	x
P0[10]	IOCON_P0_10	R/W	0x030	0x4002 C028	D (tables 82, 83)	x	x	x	x
P0[11]	IOCON_P0_11	R/W	0x030	0x4002 C02C	D (tables 82, 83)	x	x	x	x
P0[12]	IOCON_P0_12	R/W	0x1B0	0x4002 C030	A (tables 84, 85)	x	x	x	-
P0[13]	IOCON_P0_13	R/W	0x1B0	0x4002 C034	A (tables 84, 85)	x	x	x	-
P0[14]	IOCON_P0_14	R/W	0x030	0x4002 C038	D (tables 82, 83)	x	x	x	-
P0[15]	IOCON_P0_15	R/W	0x030	0x4002 C03C	D (tables 82, 83)	x	x	x	x
P0[16]	IOCON_P0_16	R/W	0x030	0x4002 C040	D (tables 82, 83)	x	x	x	x
P0[17]	IOCON_P0_17	R/W	0x030	0x4002 C044	D (tables 82, 83)	x	x	x	x
P0[18]	IOCON_P0_18	R/W	0x030	0x4002 C048	D (tables 82, 83)	x	x	x	x
P0[19]	IOCON_P0_19	R/W	0x030	0x4002 C04C	D (tables 82, 83)	x	x	x	-
P0[20]	IOCON_P0_20	R/W	0x030	0x4002 C050	D (tables 82, 83)	x	x	x	-
P0[21]	IOCON_P0_21	R/W	0x030	0x4002 C054	D (tables 82, 83)	x	x	x	-
P0[22]	IOCON_P0_22	R/W	0x030	0x4002 C058	D (tables 82, 83)	x	x	x	x
P0[23]	IOCON_P0_23	R/W	0x1B0	0x4002 C05C	A (tables 84, 85)	x	x	x	-
P0[24]	IOCON_P0_24	R/W	0x1B0	0x4002 C060	A (tables 84, 85)	x	x	x	-
P0[25]	IOCON_P0_25	R/W	0x1B0	0x4002 C064	A (tables 84, 85)	x	x	x	x
P0[26]	IOCON_P0_26	R/W	0x1B0	0x4002 C068	A (tables 84, 85)	x	x	x	x
P0[27]	IOCON_P0_27	R/W	0	0x4002 C06C	I (tables 88, 89)	x	x	x	-
P0[28]	IOCON_P0_28	R/W	0	0x4002 C070	I (tables 88, 89)	x	x	x	-
P0[29]	IOCON_P0_29	R/W	0	0x4002 C074	U (tables 86, 87)	x	x	x	x
P0[30]	IOCON_P0_30	R/W	0	0x4002 C078	U (tables 86, 87)	x	x	x	x
P0[31]	IOCON_P0_31	R/W	0	0x4002 C07C	U (tables 86, 87)	x	x	x	-

[1] Reset Value reflects the data stored in used bits only. It does not include reserved bits content.

[2] IOCON types are D (standard digital pin), and other pins with a specialized function: A (analog), U (USB), I (I2C), and W.

Registros IOCON de los pines del puerto 1

Table 77. I/O Control registers for port 1

Port pin	Register	Access	Reset Value[1]	Address	IOCON type	208-pin	180-pin	144-pin	80-pin
P1[0]	IOCON_P1_00	R/W	0x030	0x4002 C080	D (tables 82, 83)	x	x	x	x
P1[1]	IOCON_P1_01	R/W	0x030	0x4002 C084	D (tables 82, 83)	x	x	x	x
P1[2]	IOCON_P1_02	R/W	0x030	0x4002 C088	D (tables 82, 83)	x	x	-	-
P1[3]	IOCON_P1_03	R/W	0x030	0x4002 C08C	D (tables 82, 83)	x	x	-	-
P1[4]	IOCON_P1_04	R/W	0x030	0x4002 C090	D (tables 82, 83)	x	x	x	x
P1[5]	IOCON_P1_05	R/W	0x030	0x4002 C094	W (tables 90, 91)	x	x	-	-
P1[6]	IOCON_P1_06	R/W	0x030	0x4002 C098	W (tables 90, 91)	x	x	-	-
P1[7]	IOCON_P1_07	R/W	0x030	0x4002 C09C	W (tables 90, 91)	x	x	-	-
P1[8]	IOCON_P1_08	R/W	0x030	0x4002 C0A0	D (tables 82, 83)	x	x	x	x
P1[9]	IOCON_P1_09	R/W	0x030	0x4002 C0A4	D (tables 82, 83)	x	x	x	x
P1[10]	IOCON_P1_10	R/W	0x030	0x4002 C0A8	D (tables 82, 83)	x	x	x	x
P1[11]	IOCON_P1_11	R/W	0x030	0x4002 C0AC	D (tables 82, 83)	x	x	-	-
P1[12]	IOCON_P1_12	R/W	0x030	0x4002 C0B0	D (tables 82, 83)	x	x	-	-
P1[13]	IOCON_P1_13	R/W	0x030	0x4002 C0B4	D (tables 82, 83)	x	x	-	-
P1[14]	IOCON_P1_14	R/W	0x030	0x4002 C0B8	W (tables 90, 91)	x	x	x	x
P1[15]	IOCON_P1_15	R/W	0x030	0x4002 C0BC	D (tables 82, 83)	x	x	x	x
P1[16]	IOCON_P1_16	R/W	0x030	0x4002 C0C0	W (tables 90, 91)	x	x	x	-
P1[17]	IOCON_P1_17	R/W	0x030	0x4002 C0C4	W (tables 90, 91)	x	x	x	-
P1[18]	IOCON_P1_18	R/W	0x030	0x4002 C0C8	D (tables 82, 83)	x	x	x	x
P1[19]	IOCON_P1_19	R/W	0x030	0x4002 C0CC	D (tables 82, 83)	x	x	x	x
P1[20]	IOCON_P1_20	R/W	0x030	0x4002 C0D0	D (tables 82, 83)	x	x	x	x
P1[21]	IOCON_P1_21	R/W	0x030	0x4002 C0D4	D (tables 82, 83)	x	x	x	-
P1[22]	IOCON_P1_22	R/W	0x030	0x4002 C0D8	D (tables 82, 83)	x	x	x	x
P1[23]	IOCON_P1_23	R/W	0x030	0x4002 C0DC	D (tables 82, 83)	x	x	x	x
P1[24]	IOCON_P1_24	R/W	0x030	0x4002 C0E0	D (tables 82, 83)	x	x	x	x
P1[25]	IOCON_P1_25	R/W	0x030	0x4002 C0E4	D (tables 82, 83)	x	x	x	x
P1[26]	IOCON_P1_26	R/W	0x030	0x4002 C0E8	D (tables 82, 83)	x	x	x	x
P1[27]	IOCON_P1_27	R/W	0x030	0x4002 C0EC	D (tables 82, 83)	x	x	x	-
P1[28]	IOCON_P1_28	R/W	0x030	0x4002 C0F0	D (tables 82, 83)	x	x	x	x
P1[29]	IOCON_P1_29	R/W	0x030	0x4002 C0F4	D (tables 82, 83)	x	x	x	x
P1[30]	IOCON_P1_30	R/W	0x1B0	0x4002 C0F8	A (tables 84, 85)	x	x	x	x
P1[31]	IOCON_P1_31	R/W	0x1B0	0x4002 C0FC	A (tables 84, 85)	x	x	x	x

[1] Reset Value reflects the data stored in used bits only. It does not include reserved bits content.

Registros IOCON de los pines del puerto 2

Table 78. I/O Control registers for port 2

Port pin	Register	Access	Reset Value[1]	Address	IOCON type	208-pin	180-pin	144-pin	80-pin
P2[0]	IOCON_P2_00	R/W	0x030	0x4002 C100	D (tables 82, 83)	x	x	x	x
P2[1]	IOCON_P2_01	R/W	0x030	0x4002 C104	D (tables 82, 83)	x	x	x	x
P2[2]	IOCON_P2_02	R/W	0x030	0x4002 C108	D (tables 82, 83)	x	x	x	x
P2[3]	IOCON_P2_03	R/W	0x030	0x4002 C10C	D (tables 82, 83)	x	x	x	x
P2[4]	IOCON_P2_04	R/W	0x030	0x4002 C110	D (tables 82, 83)	x	x	x	x
P2[5]	IOCON_P2_05	R/W	0x030	0x4002 C114	D (tables 82, 83)	x	x	x	x
P2[6]	IOCON_P2_06	R/W	0x030	0x4002 C118	D (tables 82, 83)	x	x	x	x
P2[7]	IOCON_P2_07	R/W	0x030	0x4002 C11C	D (tables 82, 83)	x	x	x	x
P2[8]	IOCON_P2_08	R/W	0x030	0x4002 C120	D (tables 82, 83)	x	x	x	x
P2[9]	IOCON_P2_09	R/W	0x030	0x4002 C124	D (tables 82, 83)	x	x	x	x
P2[10]	IOCON_P2_10	R/W	0x030	0x4002 C128	D (tables 82, 83)	x	x	x	x
P2[11]	IOCON_P2_11	R/W	0x030	0x4002 C12C	D (tables 82, 83)	x	x	x	-
P2[12]	IOCON_P2_12	R/W	0x030	0x4002 C130	D (tables 82, 83)	x	x	x	-
P2[13]	IOCON_P2_13	R/W	0x030	0x4002 C134	D (tables 82, 83)	x	x	x	-
P2[14]	IOCON_P2_14	R/W	0x030	0x4002 C138	D (tables 82, 83)	x	-	-	-
P2[15]	IOCON_P2_15	R/W	0x030	0x4002 C13C	D (tables 82, 83)	x	-	-	-
P2[16]	IOCON_P2_16	R/W	0x030	0x4002 C140	D (tables 82, 83)	x	x	-	-
P2[17]	IOCON_P2_17	R/W	0x030	0x4002 C144	D (tables 82, 83)	x	x	-	-
P2[18]	IOCON_P2_18	R/W	0x030	0x4002 C148	D (tables 82, 83)	x	x	-	-
P2[19]	IOCON_P2_19	R/W	0x030	0x4002 C14C	D (tables 82, 83)	x	x	-	-
P2[20]	IOCON_P2_20	R/W	0x030	0x4002 C150	D (tables 82, 83)	x	x	-	-
P2[21]	IOCON_P2_21	R/W	0x030	0x4002 C154	D (tables 82, 83)	x	x	-	-
P2[22]	IOCON_P2_22	R/W	0x030	0x4002 C158	D (tables 82, 83)	x	-	-	-
P2[23]	IOCON_P2_23	R/W	0x030	0x4002 C15C	D (tables 82, 83)	x	-	-	-
P2[24]	IOCON_P2_24	R/W	0x030	0x4002 C160	D (tables 82, 83)	x	x	-	-
P2[25]	IOCON_P2_25	R/W	0x030	0x4002 C164	D (tables 82, 83)	x	x	-	-
P2[26]	IOCON_P2_26	R/W	0x030	0x4002 C168	D (tables 82, 83)	x	-	-	-
P2[27]	IOCON_P2_27	R/W	0x030	0x4002 C16C	D (tables 82, 83)	x	-	-	-
P2[28]	IOCON_P2_28	R/W	0x030	0x4002 C170	D (tables 82, 83)	x	x	-	-
P2[29]	IOCON_P2_29	R/W	0x030	0x4002 C174	D (tables 82, 83)	x	x	-	-
P2[30]	IOCON_P2_30	R/W	0x030	0x4002 C178	D (tables 82, 83)	x	-	-	-
P2[31]	IOCON_P2_31	R/W	0x030	0x4002 C17C	D (tables 82, 83)	x	-	-	-

[1] Reset Value reflects the data stored in used bits only. It does not include reserved bits content.

Registros IOCON de los pines del puerto 3

Table 79. I/O Control registers for port 3

Port pin	Register	Access	Reset Value[1]	Address	IOCON type	208-pin	180-pin	144-pin	80-pin
P3[0]	IOCON_P3_00	R/W	0x030	0x4002 C180	D (tables 82, 83)	x	x	x	-
P3[1]	IOCON_P3_01	R/W	0x030	0x4002 C184	D (tables 82, 83)	x	x	x	-
P3[2]	IOCON_P3_02	R/W	0x030	0x4002 C188	D (tables 82, 83)	x	x	x	-
P3[3]	IOCON_P3_03	R/W	0x030	0x4002 C18C	D (tables 82, 83)	x	x	x	-
P3[4]	IOCON_P3_04	R/W	0x030	0x4002 C190	D (tables 82, 83)	x	x	x	-
P3[5]	IOCON_P3_05	R/W	0x030	0x4002 C194	D (tables 82, 83)	x	x	x	-
P3[6]	IOCON_P3_06	R/W	0x030	0x4002 C198	D (tables 82, 83)	x	x	x	-
P3[7]	IOCON_P3_07	R/W	0x030	0x4002 C19C	D (tables 82, 83)	x	x	x	-
P3[8]	IOCON_P3_08	R/W	0x030	0x4002 C1A0	D (tables 82, 83)	x	x	-	-
P3[9]	IOCON_P3_09	R/W	0x030	0x4002 C1A4	D (tables 82, 83)	x	x	-	-
P3[10]	IOCON_P3_10	R/W	0x030	0x4002 C1A8	D (tables 82, 83)	x	x	-	-
P3[11]	IOCON_P3_11	R/W	0x030	0x4002 C1AC	D (tables 82, 83)	x	x	-	-
P3[12]	IOCON_P3_12	R/W	0x030	0x4002 C1B0	D (tables 82, 83)	x	x	-	-
P3[13]	IOCON_P3_13	R/W	0x030	0x4002 C1B4	D (tables 82, 83)	x	x	-	-
P3[14]	IOCON_P3_14	R/W	0x030	0x4002 C1B8	D (tables 82, 83)	x	x	-	-
P3[15]	IOCON_P3_15	R/W	0x030	0x4002 C1BC	D (tables 82, 83)	x	x	-	-
P3[16]	IOCON_P3_16	R/W	0x030	0x4002 C1C0	D (tables 82, 83)	x	-	-	-
P3[17]	IOCON_P3_17	R/W	0x030	0x4002 C1C4	D (tables 82, 83)	x	-	-	-
P3[18]	IOCON_P3_18	R/W	0x030	0x4002 C1C8	D (tables 82, 83)	x	-	-	-
P3[19]	IOCON_P3_19	R/W	0x030	0x4002 C1CC	D (tables 82, 83)	x	-	-	-
P3[20]	IOCON_P3_20	R/W	0x030	0x4002 C1D0	D (tables 82, 83)	x	-	-	-
P3[21]	IOCON_P3_21	R/W	0x030	0x4002 C1D4	D (tables 82, 83)	x	-	-	-
P3[22]	IOCON_P3_22	R/W	0x030	0x4002 C1D8	D (tables 82, 83)	x	-	-	-
P3[23]	IOCON_P3_23	R/W	0x030	0x4002 C1DC	D (tables 82, 83)	x	x	x	-
P3[24]	IOCON_P3_24	R/W	0x030	0x4002 C1E0	D (tables 82, 83)	x	x	x	-
P3[25]	IOCON_P3_25	R/W	0x030	0x4002 C1E4	D (tables 82, 83)	x	x	x	-
P3[26]	IOCON_P3_26	R/W	0x030	0x4002 C1E8	D (tables 82, 83)	x	x	x	-
P3[27]	IOCON_P3_27	R/W	0x030	0x4002 C1EC	D (tables 82, 83)	x	-	-	-
P3[28]	IOCON_P3_28	R/W	0x030	0x4002 C1F0	D (tables 82, 83)	x	-	-	-
P3[29]	IOCON_P3_29	R/W	0x030	0x4002 C1F4	D (tables 82, 83)	x	-	-	-
P3[30]	IOCON_P3_30	R/W	0x030	0x4002 C1F8	D (tables 82, 83)	x	-	-	-
P3[31]	IOCON_P3_31	R/W	0x030	0x4002 C1FC	D (tables 82, 83)	x	-	-	-

[1] Reset Value reflects the data stored in used bits only. It does not include reserved bits content.

Registros IOCON de los pines del puerto 4

Table 80. I/O Control registers for port 4

Port pin	Register	Access	Reset Value[1]	Address	IOCON type	208-pin	180-pin	144-pin	80-pin
P4[0]	IOCON_P4_00	R/W	0x030	0x4002 C200	D (tables 82, 83)	x	x	x	-
P4[1]	IOCON_P4_01	R/W	0x030	0x4002 C204	D (tables 82, 83)	x	x	x	-
P4[2]	IOCON_P4_02	R/W	0x030	0x4002 C208	D (tables 82, 83)	x	x	x	-
P4[3]	IOCON_P4_03	R/W	0x030	0x4002 C20C	D (tables 82, 83)	x	x	x	-
P4[4]	IOCON_P4_04	R/W	0x030	0x4002 C210	D (tables 82, 83)	x	x	x	-
P4[5]	IOCON_P4_05	R/W	0x030	0x4002 C214	D (tables 82, 83)	x	x	x	-
P4[6]	IOCON_P4_06	R/W	0x030	0x4002 C218	D (tables 82, 83)	x	x	x	-
P4[7]	IOCON_P4_07	R/W	0x030	0x4002 C21C	D (tables 82, 83)	x	x	x	-
P4[8]	IOCON_P4_08	R/W	0x030	0x4002 C220	D (tables 82, 83)	x	x	x	-
P4[9]	IOCON_P4_09	R/W	0x030	0x4002 C224	D (tables 82, 83)	x	x	x	-
P4[10]	IOCON_P4_10	R/W	0x030	0x4002 C228	D (tables 82, 83)	x	x	x	-
P4[11]	IOCON_P4_11	R/W	0x030	0x4002 C22C	D (tables 82, 83)	x	x	x	-
P4[12]	IOCON_P4_12	R/W	0x030	0x4002 C230	D (tables 82, 83)	x	x	x	-
P4[13]	IOCON_P4_13	R/W	0x030	0x4002 C234	D (tables 82, 83)	x	x	x	-
P4[14]	IOCON_P4_14	R/W	0x030	0x4002 C238	D (tables 82, 83)	x	x	x	-
P4[15]	IOCON_P4_15	R/W	0x030	0x4002 C23C	D (tables 82, 83)	x	x	x	-
P4[16]	IOCON_P4_16	R/W	0x030	0x4002 C240	D (tables 82, 83)	x	x	-	-
P4[17]	IOCON_P4_17	R/W	0x030	0x4002 C244	D (tables 82, 83)	x	x	-	-
P4[18]	IOCON_P4_18	R/W	0x030	0x4002 C248	D (tables 82, 83)	x	x	-	-
P4[19]	IOCON_P4_19	R/W	0x030	0x4002 C24C	D (tables 82, 83)	x	x	-	-
P4[20]	IOCON_P4_20	R/W	0x030	0x4002 C250	D (tables 82, 83)	x	-	-	-
P4[21]	IOCON_P4_21	R/W	0x030	0x4002 C254	D (tables 82, 83)	x	-	-	-
P4[22]	IOCON_P4_22	R/W	0x030	0x4002 C258	D (tables 82, 83)	x	-	-	-
P4[23]	IOCON_P4_23	R/W	0x030	0x4002 C25C	D (tables 82, 83)	x	-	-	-
P4[24]	IOCON_P4_24	R/W	0x030	0x4002 C260	D (tables 82, 83)	x	x	x	-
P4[25]	IOCON_P4_25	R/W	0x030	0x4002 C264	D (tables 82, 83)	x	x	x	-
P4[26]	IOCON_P4_26	R/W	0x030	0x4002 C268	D (tables 82, 83)	x	x	-	-
P4[27]	IOCON_P4_27	R/W	0x030	0x4002 C26C	D (tables 82, 83)	x	x	-	-
P4[28]	IOCON_P4_28	R/W	0x030	0x4002 C270	D (tables 82, 83)	x	x	x	x
P4[29]	IOCON_P4_29	R/W	0x030	0x4002 C274	D (tables 82, 83)	x	x	x	x
P4[30]	IOCON_P4_30	R/W	0x030	0x4002 C278	D (tables 82, 83)	x	x	x	-
P4[31]	IOCON_P4_31	R/W	0x030	0x4002 C27C	D (tables 82, 83)	x	x	x	-

[1] Reset Value reflects the data stored in used bits only. It does not include reserved bits content.

Registros IOCON de los pines del puerto 5

Table 81. I/O Control registers for port 5

Port pin	Register	Access	Reset Value[1]	Address	IOCON type	208-pin	180-pin	144-pin	80-pin
P5[0]	IOCON_P5_00	R/W	0x030	0x4002 C280	D (tables 82, 83)	x	x	x	-
P5[1]	IOCON_P5_01	R/W	0x030	0x4002 C284	D (tables 82, 83)	x	x	x	-
P5[2]	IOCON_P5_02	R/W	0	0x4002 C288	I (tables 88, 89)	x	x	x	-
P5[3]	IOCON_P5_03	R/W	0	0x4002 C28C	I (tables 88, 89)	x	x	x	-
P5[4]	IOCON_P5_04	R/W	0x030	0x4002 C290	D (tables 82, 83)	x	x	x	-

[1] Reset Value reflects the data stored in used bits only. It does not include reserved bits content.

Tipos de pines en el LPC4088

- Según el tipo de configuración que admiten se distinguen:
  - **Pines tipo D**: pines estándar.
  - **Pines tipo A**: pines que incluyen una función analógica.
  - **Pines tipo U**: pines que incluyen funciones USB D+ o D–.
  - **Pines tipo I**: pines que incluyen funciones I^2C especializadas.
  - **Pines tipo W**: pines que incluyen un filtro de *glitch*.

Registros IOCON de pines tipo D

Table 82. Type D IOCON registers bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. See Table 83 for specific values.	000
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control). See Section 7.3.2 “Pin mode”.	10
		00	Inactive (no pull-down/pull-up resistor enabled).	
		01	Pull-down resistor enabled.	
		10	Pull-up resistor enabled.	
		11	Repeater mode.	
5	HYS		Hysteresis. See Section 7.3.3 “Hysteresis”.	1
		0	Disable.	
		1	Enable.	
6	INV		Input polarity. See Section 7.3.4 “Input Inversion”.	0
		0	Input is not inverted (a HIGH on the pin reads as 1)	
		1	Input is inverted (a HIGH on the pin reads as 0)	
8:7	-		Reserved. Read value is undefined, only zero should be written.	NA
9	SLEW		Driver slew rate. See Section 7.3.7 “Output slew rate”.	0
		0	Standard mode, output slew rate control is enabled. More outputs can be switched simultaneously.	
		1	Fast mode, slew rate control is disabled. Refer to the appropriate specific device data sheet for details.	
10	OD		Controls open-drain mode. See Section 7.3.9 “Open-Drain Mode”.	0
		0	Normal push-pull output	
		1	Simulated open-drain output (high drive disabled)	
31:11	-		Reserved. Read value is undefined, only zero should be written.	NA

Funciones de pines tipo D (1 de 5)

Table 83. Type D I/O Control registers: FUNC values and pin functions

	Value of FUNC field in IOCON register							
Register	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
IOCON_P0_0	P0[0]	CAN_RD1	U3_TXD	I2C1_SDA	U0_TXD			
IOCON_P0_1	P0[1]	CAN_TD1	U3_RXD	I2C1_SCL	U0_RXD			
IOCON_P0_2	P0[2]	U0_TXD	U3_TXD					
IOCON_P0_3	P0[3]	U0_RXD	U3_RXD					
IOCON_P0_4	P0[4]	I2S_RX_SCK	CAN_RD2	T2_CAP0		CMP_ROSC		LCD_VD[0]
IOCON_P0_5	P0[5]	I2S_RX_WS	CAN_TD2	T2_CAP1		CMP_RESET		LCD_VD[1]
IOCON_P0_6	P0[6]	I2S_RX_SDA	SSP1_SSEL	T2_MAT0	U1_RTS	CMP_ROSC		LCD_VD[8]
IOCON_P0_10	P0[10]	U2_TXD	I2C2_SDA	T3_MAT0				LCD_VD[5]
IOCON_P0_11	P0[11]	U2_RXD	I2C2_SCL	T3_MAT1				LCD_VD[10]
IOCON_P0_14	P0[14]	$\overline{\text{USB\_HSTEN2}}$	SSP1_SSEL	USB_CONNECT2				
IOCON_P0_15	P0[15]	U1_TXD	SSP0_SCK			SPIFI_IO[2]		
IOCON_P0_16	P0[16]	U1_RXD	SSP0_SSEL			SPIFI_IO[3]		
IOCON_P0_17	P0[17]	U1_CTS	SSP0_MISO			SPIFI_IO[1]		
IOCON_P0_18	P0[18]	U1_DCD	SSP0_MOSI			SPIFI_IO[0]		
IOCON_P0_19	P0[19]	U1_DSR	SD_CLK	I2C1_SDA				LCD_VD[13]
IOCON_P0_20	P0[20]	U1_DTR	SD_CMD	I2C1_SCL				LCD_VD[14]
IOCON_P0_21	P0[21]	U1_RI	SD_PWR	U4_OE	CAN_RD1	U4_SCLK		
IOCON_P0_22	P0[22]	U1_RTS	SD_DAT[0]	U4_TXD	CAN_TD1	SPIFI_CLK		
IOCON_P1_0	P1[0]	ENET_TXD0		T3_CAP1	SSP2_SCK			
IOCON_P1_1	P1[1]	ENET_TXD1		T3_MAT3	SSP2_MOSI			
IOCON_P1_2	P1[2]	ENET_TXD2	SD_CLK	PWM0[1]				
IOCON_P1_3	P1[3]	ENET_TXD3	SD_CMD	PWM0[2]				
IOCON_P1_4	P1[4]	ENET_TX_EN		T3_MAT2	SSP2_MISO			
IOCON_P1_8	P1[8]	ENET_CRS		T3_MAT1	SSP2_SSEL			
IOCON_P1_9	P1[9]	ENET_RXD0		T3_MAT0				
IOCON_P1_10	P1[10]	ENET_RXD1		T3_CAP0				
IOCON_P1_11	P1[11]	ENET_RXD2	SD_DAT[2]	PWM0[6]				
IOCON_P1_12	P1[12]	ENET_RXD3	SD_DAT[3]	PWM0_CAP0		CMP1_OUT		
IOCON_P1_13	P1[13]	ENET_RX_DV						

Funciones de pines tipo D (2 de 5)

Table 83. Type D I/O Control registers: FUNC values and pin functions

	Value of FUNC field in IOCON register							
Register	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
IOCON_P1_15	P1[15]	ENET_RX_CLK		I2C2_SDA				
IOCON_P1_18	P1[18]	USB_UP_LED1	PWM1[1]	T1_CAP0		SSP1_MISO		
IOCON_P1_19	P1[19]	USB_TX_E1	USB_PPWR1	T1_CAP1	MC_0A	SSP1_SCK	U2_OE	
IOCON_P1_20	P1[20]	USB_TX_DP1	PWM1[2]	QEI_PHA	MC_FB0	SSP0_SCK	LCD_VD[6]	LCD_VD[10]
IOCON_P1_21	P1[21]	USB_TX_DM1	PWM1[3]	SSP0_SSEL	MC_ABORT		LCD_VD[7]	LCD_VD[11]
IOCON_P1_22	P1[22]	USB_RCV1	USB_PWRD1	T1_MAT0	MC_0B	SSP1_MOSI	LCD_VD[8]	LCD_VD[12]
IOCON_P1_23	P1[23]	USB_RX_DP1	PWM1[4]	QEI_PHB	MC_FB1	SSP0_MISO	LCD_VD[9]	LCD_VD[13]
IOCON_P1_24	P1[24]	USB_RX_DM1	PWM1[5]	QEI_IDX	MC_FB2	SSP0_MOSI	LCD_VD[10]	LCD_VD[14]
IOCON_P1_25	P1[25]	USB_LS1	USB_HSTEN1	T1_MAT1	MC_1A	CLKOUT	LCD_VD[11]	LCD_VD[15]
IOCON_P1_26	P1[26]	USB_SSPND1	PWM1[6]	T0_CAP0	MC_1B	SSP1_SSEL	LCD_VD[12]	LCD_VD[20]
IOCON_P1_27	P1[27]	USB_INT1	USB_OVRCR1	T0_CAP1	CLKOUT		LCD_VD[13]	LCD_VD[21]
IOCON_P1_28	P1[28]	USB_SCL1	PWM1_CAP0	T0_MAT0	MC_2A	SSP0_SSEL	LCD_VD[14]	LCD_VD[22]
IOCON_P1_29	P1[29]	USB_SDA1	PWM1_CAP1	T0_MAT1	MC_2B	U4_TXD	LCD_VD[15]	LCD_VD[23]
IOCON_P2_0	P2[0]	PWM1[1]	U1_TXD					LCD_PWR
IOCON_P2_1	P2[1]	PWM1[2]	U1_RXD					LCD_LE
IOCON_P2_2	P2[2]	PWM1[3]	U1_CTS	T2_MAT3		TRACEDATA[3]		LCD_DCLK
IOCON_P2_3	P2[3]	PWM1[4]	U1_DCD	T2_MAT2		TRACEDATA[2]		LCD_FP
IOCON_P2_4	P2[4]	PWM1[5]	U1_DSR	T2_MAT1		TRACEDATA[1]		LCD_ENAB_M
IOCON_P2_5	P2[5]	PWM1[6]	U1_DTR	T2_MAT0		TRACEDATA[0]		LCD_LP
IOCON_P2_6	P2[6]	PWM1_CAP0	U1_RI	T2_CAP0	U2_OE	TRACECLK	LCD_VD[0]	LCD_VD[4]
IOCON_P2_7	P2[7]	CAN_RD2	U1_RTS			SPIFI_CS	LCD_VD[1]	LCD_VD[5]
IOCON_P2_8	P2[8]	CAN_TD2	U2_TXD	U1_CTS	ENET_MDC		LCD_VD[2]	LCD_VD[6]
IOCON_P2_9	P2[9]	USB_CONNECT1	U2_RXD	U4_RXD	ENET_MDIO		LCD_VD[3]	LCD_VD[7]
IOCON_P2_10	P2[10]	EINT0	NMI					
IOCON_P2_11	P2[11]	EINT1	SD_DAT[1]	I2S_TX_SCK				LCD_CLKIN
IOCON_P2_12	P2[12]	EINT2	SD_DAT[2]	I2S_TX_WS	LCD_VD[4]	LCD_VD[3]	LCD_VD[8]	LCD_VD[18]
IOCON_P2_13	P2[13]	EINT3	SD_DAT[3]	I2S_TX_SDA		LCD_VD[5]	LCD_VD[9]	LCD_VD[19]
IOCON_P2_14	P2[14]	EMC_CS2	I2C1_SDA	T2_CAP0				
IOCON_P2_15	P2[15]	EMC_CS3	I2C1_SCL	T2_CAP1				
IOCON_P2_16	P2[16]	EMC_CAS						

Funciones de pines tipo D (3 de 5)

Table 83. Type D I/O Control registers: FUNC values and pin functions

	Value of FUNC field in IOCON register							
Register	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
IOCON_P2_17	P2[17]	EMC_RAS						
IOCON_P2_18	P2[18]	EMC_CLK0						
IOCON_P2_19	P2[19]	EMC_CLK1						
IOCON_P2_20	P2[20]	EMC_DYCS0						
IOCON_P2_21	P2[21]	EMC_DYCS1						
IOCON_P2_22	P2[22]	EMC_DYCS2	SSP0_SCK	T3_CAP0				
IOCON_P2_23	P2[23]	EMC_DYCS3	SSP0_SSEL	T3_CAP1				
IOCON_P2_24	P2[24]	EMC_CKE0						
IOCON_P2_25	P2[25]	EMC_CKE1						
IOCON_P2_26	P2[26]	EMC_CKE2	SSP0_MISO	T3_MAT0				
IOCON_P2_27	P2[27]	EMC_CKE3	SSP0_MOSI	T3_MAT1				
IOCON_P2_28	P2[28]	EMC_DQM0						
IOCON_P2_29	P2[29]	EMC_DQM1						
IOCON_P2_30	P2[30]	EMC_DQM2	I2C2_SDA	T3_MAT2				
IOCON_P2_31	P2[31]	EMC_DQM3	I2C2_SCL	T3_MAT3				
IOCON_P3_0	P3[0]	EMC_D[0]						
IOCON_P3_1	P3[1]	EMC_D[1]						
IOCON_P3_2	P3[2]	EMC_D[2]						
IOCON_P3_3	P3[3]	EMC_D[3]						
IOCON_P3_4	P3[4]	EMC_D[4]						
IOCON_P3_5	P3[5]	EMC_D[5]						
IOCON_P3_6	P3[6]	EMC_D[6]						
IOCON_P3_7	P3[7]	EMC_D[7]						
IOCON_P3_8	P3[8]	EMC_D[8]						
IOCON_P3_9	P3[9]	EMC_D[9]						
IOCON_P3_10	P3[10]	EMC_D[10]						
IOCON_P3_11	P3[11]	EMC_D[11]						
IOCON_P3_12	P3[12]	EMC_D[12]						
IOCON_P3_13	P3[13]	EMC_D[13]						
IOCON_P3_14	P3[14]	EMC_D[14]						

Funciones de pines tipo D (4 de 5)

Table 83. Type D I/O Control registers: FUNC values and pin functions

	Value of FUNC field in IOCON register							
Register	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
IOCON_P3_15	P3[15]	EMC_D[15]						
IOCON_P3_16	P3[16]	EMC_D[16]	PWM0[1]	U1_TXD				
IOCON_P3_17	P3[17]	EMC_D[17]	PWM0[2]	U1_RXD				
IOCON_P3_18	P3[18]	EMC_D[18]	PWM0[3]	U1_CTS				
IOCON_P3_19	P3[19]	EMC_D[19]	PWM0[4]	U1_DCD				
IOCON_P3_20	P3[20]	EMC_D[20]	PWM0[5]	U1_DSR				
IOCON_P3_21	P3[21]	EMC_D[21]	PWM0[6]	U1_DTR				
IOCON_P3_22	P3[22]	EMC_D[22]	PWM0_CAP0	U1_RI				
IOCON_P3_23	P3[23]	EMC_D[23]	PWM1_CAP0	T0_CAP0				
IOCON_P3_24	P3[24]	EMC_D[24]	PWM1[1]	T0_CAP1				
IOCON_P3_25	P3[25]	EMC_D[25]	PWM1[2]	T0_MAT0				
IOCON_P3_26	P3[26]	EMC_D[26]	PWM1[3]	T0_MAT1	STCLK			
IOCON_P3_27	P3[27]	EMC_D[27]	PWM1[4]	T1_CAP0				
IOCON_P3_28	P3[28]	EMC_D[28]	PWM1[5]	T1_CAP1				
IOCON_P3_29	P3[29]	EMC_D[29]	PWM1[6]	T1_MAT0				
IOCON_P3_30	P3[30]	EMC_D[30]	U1_RTS	T1_MAT1				
IOCON_P3_31	P3[31]	EMC_D[31]		T1_MAT2				
IOCON_P4_0	P4[0]	EMC_A[0]						
IOCON_P4_1	P4[1]	EMC_A[1]						
IOCON_P4_2	P4[2]	EMC_A[2]						
IOCON_P4_3	P4[3]	EMC_A[3]						
IOCON_P4_4	P4[4]	EMC_A[4]						
IOCON_P4_5	P4[5]	EMC_A[5]						
IOCON_P4_6	P4[6]	EMC_A[6]						
IOCON_P4_7	P4[7]	EMC_A[7]						
IOCON_P4_8	P4[8]	EMC_A[8]						
IOCON_P4_9	P4[9]	EMC_A[9]						
IOCON_P4_10	P4[10]	EMC_A[10]						
IOCON_P4_11	P4[11]	EMC_A[11]						
IOCON_P4_12	P4[12]	EMC_A[12]						

Funciones de pines tipo D (5 de 5)

Table 83. Type D I/O Control registers: FUNC values and pin functions

	Value of FUNC field in IOCON register							
Register	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
IOCON_P4_13	P4[13]	EMC_A[13]						
IOCON_P4_14	P4[14]	EMC_A[14]						
IOCON_P4_15	P4[15]	EMC_A[15]						
IOCON_P4_16	P4[16]	EMC_A[16]						
IOCON_P4_17	P4[17]	EMC_A[17]						
IOCON_P4_18	P4[18]	EMC_A[18]						
IOCON_P4_19	P4[19]	EMC_A[19]						
IOCON_P4_20	P4[20]	EMC_A[20]	I2C2_SDA	SSP1_SCK				
IOCON_P4_21	P4[21]	EMC_A[21]	I2C2_SCL	SSP1_SSEL				
IOCON_P4_22	P4[22]	EMC_A[22]	U2_TXD	SSP1_MISO				
IOCON_P4_23	P4[23]	EMC_A[23]	U2_RXD	SSP1_MOSI				
IOCON_P4_24	P4[24]	$\overline{\text{EMC\_OE}}$						
IOCON_P4_25	P4[25]	$\overline{\text{EMC\_WE}}$						
IOCON_P4_26	P4[26]	$\overline{\text{EMC\_BLS0}}$						
IOCON_P4_27	P4[27]	$\overline{\text{EMC\_BLS1}}$						
IOCON_P4_28	P4[28]	$\overline{\text{EMC\_BLS2}}$	U3_TXD	T2_MAT0		LCD_VD[6]	LCD_VD[10]	LCD_VD[2]
IOCON_P4_29	P4[29]	$\overline{\text{EMC\_BLS3}}$	U3_RXD	T2_MAT1	I2C2_SCL	LCD_VD[7]	LCD_VD[11]	LCD_VD[3]
IOCON_P4_30	P4[30]	$\overline{\text{EMC\_CS0}}$				CMP0_OUT		
IOCON_P4_31	P4[31]	$\overline{\text{EMC\_CS1}}$						
IOCON_P5_0	P5[0]	EMC_A[24]	SSP2_MOSI	T2_MAT2				
IOCON_P5_1	P5[1]	EMC_A[25]	SSP2_MISO	T2_MAT3				
IOCON_P5_4	P5[4]	U0_OE		T3_MAT3	U4_TXD			

Registros IOCON de pines tipo A

Table 84. Type A IOCON registers bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. See Table 85 for specific values.	0
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control). See Section 7.3.2 “Pin mode”.	10
		00	Inactive (no pull-down/pull-up resistor enabled).	
		01	Pull-down resistor enabled.	
		10	Pull-up resistor enabled.	
		11	Repeater mode.	
5	-		Reserved. Read value is undefined, only zero should be written.	NA
6	INVERT		Input polarity. See Section 7.3.4 “Input Inversion”.	0
		0	Input is not inverted (a HIGH on the pin reads as 1)	
		1	Input is inverted (a HIGH on the pin reads as 0)	
7	ADMODE		Select Analog/Digital mode. See Section 7.3.5 “Analog/digital mode”.	1
		0	Analog mode.	
		1	Digital mode.	
8	FILTER		Controls glitch filter. See Section 7.3.6 “Input filter”.	1
		0	Noise pulses below approximately 10 ns are filtered out	
		1	No input filtering is done	
9	-		Reserved. Read value is undefined, only zero should be written.	NA
10	OD		Controls open-drain mode. See Section 7.3.9 “Open-Drain Mode”.	0
		0	Normal push-pull output	
		1	Simulated open-drain output (high drive disabled)	
14:11	-		Reserved. Read value is undefined, only zero should be written.	NA
16	DACEN		DAC enable control. This bit applies only to P0[26], which includes the DAC output function DAC_OUT. See Section 7.3.10 “DAC enable”.	0
		0	DAC is disabled	
		1	DAC is enabled	
31:17	-		Reserved. Read value is undefined, only zero should be written.	NA

Funciones de pines tipo A

Table 85. Type A I/O Control registers: FUNC values and pin functions

	Value of FUNC field in IOCON register							
Register	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
IOCON_P0_12	P0[12]	USB_PPWR2	SSP1_MISO	ADC0[6]				
IOCON_P0_13	P0[13]	USB_UP_LED2	SSP1_MOSI	ADC0[7]				
IOCON_P0_23	P0[23]	ADC0[0]	I2S_RX_SCK	T3_CAP0				
IOCON_P0_24	P0[24]	ADC0[1]	I2S_RX_WS	T3_CAP1				
IOCON_P0_25	P0[25]	ADC0[2]	I2S_RX_SDA	U3_TXD				
IOCON_P0_26	P0[26]	ADC0[3]	DAC_OUT	U3_RXD				
IOCON_P1_30	P1[30]	USB_PWRD2	USB_VBUS	ADC[4]	I2C0_SDA	U3_OE		
IOCON_P1_31	P1[31]	USB_OVRCR2	SSP1_SCK	ADC[5]	I2C0_SCL			

Registros IOCON y funciones de pines tipo U

- Registros IOCON de funciones tipo U.

Table 86. Type U IOCON registers bit description

Bit	Symbol	Description	Reset value
2:0	FUNC	Selects pin function. See Table 87 for specific values.	000
31:3	-	Reserved. Read value is undefined, only zero should be written.	NA

- Funciones de pines tipo U.

Table 87. Type U I/O Control registers: FUNC values and pin functions

	Value of FUNC field in IOCON register							
Register	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
IOCON_P0_29	P0[29]	USB_D+1	EINT0					
IOCON_P0_30	P0[30]	USB_D-1	EINT1					
IOCON_P0_31	P0[31]	USB_D+2						

Registros IOCON de pines tipo I

Table 88. Type I IOCON registers bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. See Table 89 for specific values.	0
5:3	-		Reserved. Read value is undefined, only zero should be written.	NA
6	INVERT		Input polarity. See Section 7.3.4 “Input Inversion”.	0
		0	Input is not inverted (a HIGH on the pin reads as 1)	
		1	Input is inverted (a HIGH on the pin reads as 0)	
7	-		Reserved. Read value is undefined, only zero should be written.	NA
8	HS		Configures I^2C features for standard mode, fast mode, and Fast Mode Plus operation. See Section 7.3.8 “I^2C modes”.	0
		0	I^2C 50ns glitch filter and slew rate control enabled.	
		1	I^2C 50ns glitch filter and slew rate control disabled.	
9	HIDRIVE		Controls sink current capability of the pin, only for P5[2] and P5[3]. See Section 7.3.8 “I^2C modes”.	0
		0	Output drive sink is 4 mA. This is sufficient for standard and fast mode I^2C.	
		1	Output drive sink is 20 mA. This is needed for Fast Mode Plus I^2C. Refer to the appropriate specific device data sheet for details.	
31:10	-		Reserved. Read value is undefined, only zero should be written.	NA

Funciones de pines tipo I

Table 89. Type I I/O Control registers: FUNC values and pin functions

	Value of FUNC field in IOCON register							
Register	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
IOCON_P0_27	P0[27]	I2C0_SDA	USB_SDA1					
IOCON_P0_28	P0[28]	I2C0_SCL	USB_SCL1					
IOCON_P5_2	P5[2]			T3_MAT2		I2C0_SDA		
IOCON_P5_3	P5[3]				U4_RXD	I2C0_SCL		

Registros IOCON de pines tipo W

Table 90. Type W IOCON registers bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. See Table 91 for specific values.	000
4:3	MODE		Selects the output functional mode for the pin (on-chip pull-up/pull-down resistor control). See Section 7.3.2 "Pin mode".	00
		00	Inactive (no pull-down/pull-up resistor enabled).	
		01	Pull-down resistor enabled.	
		10	Pull-up resistor enabled.	
		11	Repeater mode.	
5	HYS		Hysteresis. See Section 7.3.3 "Hysteresis".	1
		0	Disable.	
		1	Enable.	
6	INV		Input polarity. See Section 7.3.4 "Input Inversion".	0
		0	Input is not inverted (a HIGH on the pin reads as 1)	
		1	Input is inverted (a HIGH on the pin reads as 0)	
7	ADMODE		Select Analog/Digital mode. See Section 7.3.5 "Analog/digital mode".	1
		0	Analog mode.	
		1	Digital mode.	
8	FILTER		Controls glitch filter. See Section 7.3.6 "Input filter".	0
		0	Noise pulses below approximately 10 ns are filtered out	
		1	No input filtering is done	
9	SLEW		Driver slew rate. See Section 7.3.7 "Output slew rate".	0
		0	Standard mode, output slew rate control is enabled. More outputs can be switched simultaneously.	
		1	Fast mode, slew rate control is disabled. Refer to the appropriate specific device data sheet for details.	
10	OD		Controls open-drain mode. See Section 7.3.9 "Open-Drain Mode".	0
		0	Normal push-pull output	
		1	Simulated open-drain output (high drive disabled)	
31:11	-		Reserved. Read value is undefined, only zero should be written.	NA

Funciones de pines tipo W

Table 91. Type W I/O Control registers: FUNC values and pin functions

	Value of FUNC field in IOCON register							
Register	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
IOCON_P0_7	P0[7]	I2S_TX_SCK	SSP1_SCK	T2_MAT1	RTC_EV0	CMP_VREF		LCD_VD[9]
IOCON_P0_8	P0[8]	I2S_TX_WS	SSP1_MISO	T2_MAT2	RTC_EV1	CMP1_IN[4]		LCD_VD[16]
IOCON_P0_9	P0[9]	I2S_TX_SDA	SSP1_MOSI	T2_MAT3	RTC_EV2	CMP1_IN[3]		LCD_VD[17]
IOCON_P1_5	P1[5]	ENET_TX_ER	SD_PWR	PWM0[3]		CMP1_IN[2]		
IOCON_P1_6	P1[6]	ENET_TX_CLK	SD_DAT[0]	PWM0[4]		CMP0_IN[4]		
IOCON_P1_7	P1[7]	ENET_COL	SD_DAT[1]	PWM0[5]		CMP1_IN[1]		
IOCON_P1_14	P1[14]	ENET_RX_ER		T2_CAP0		CMP0_IN[1]		
IOCON_P1_16	P1[16]	ENET_MDC	I2S_TX_MCLK			CMP0_IN[2]		
IOCON_P1_17	P1[17]	ENET_MDIO	I2S_RX_MCLK			CMP0_IN[3]		

Procedimiento para seleccionar la función de un pin

1. Buscar el pin en las tablas 76 a 81 del manual.
2. De estas tablas, obtener de qué tipo es el pin.
3. Consultar las funciones del pin en una de las tablas 83, 85, 87, 89, 91.
4. Obtener la combinación del campo `FUNC` para el registro `IOCON` correspondiente.
5. Consultar la estructura del registro `IOCON` correspondiente en una de las tablas 82, 84, 86, 88, 90.
6. Programar la función deseada en los bits 2:0 del registro `IOCON` correspondiente. Si la función es analógica, poner el bit `ADMODE` a 0.

Ejemplo de selección de la función de un pin

- Seleccionar la función AD0[1] para el pin

  P0[24]/**AD0[1]**/I2S_RX_WS/T3_CAP1

1. Localizamos el pin P0[24] en la tabla 76.
2. De la tabla 76 vemos que el pin es de tipo A.
3. Los pines tipo A se recogen en la tabla 85.
4. El valor para el campo FUNC es 001.
5. La estructura de registros IOCON de los pines tipo A se indica en la tabla 84.

```
LPC_IOCON->P0_24 = 1; /* FUNC = 1, ADMODE = 0, sin pull-up/pull-down */
```