Convertidor analógico/digital del LPC4088

Diseño Basado en Microprocesadores

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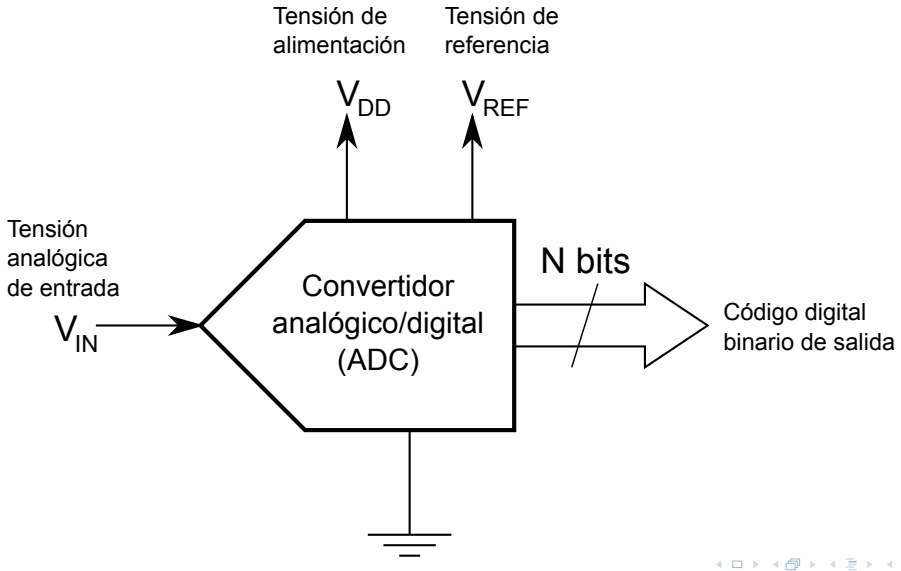
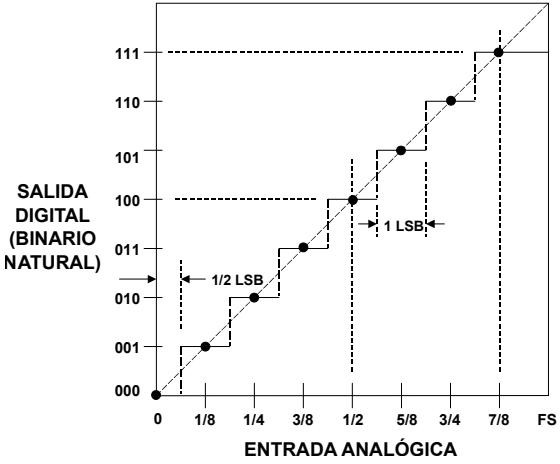
Contenido

Convertidor analógico/digital (ADC) unipolar



Curva de transferencia de un ADC unipolar de 3 bits



- La tensión de referencia determina la tensión de fondo de escala (FS).
- Tensión 1 LSB:
  - Cambio necesario en la tensión de entrada para asegurar el cambio en el LSB del código de salida.
  - También se denomina cuanto (Q) del convertidor.

$$V_{LSB} = Q = \frac{V_{FS}}{2^N}$$

Características del ADC del LPC4088

- Convertidor de aproximaciones sucesivas.
- 12 bits de resolución.
- 8 canales de entrada multiplexados.
- Rango de medida unipolar de GND a V_{REFP} (V_{REFP}: tensión de referencia aplicada externamente).
- Tasa de conversión de hasta 400 kHz.
- Modo ráfaga para convertir sucesivamente varios canales.
- Inicio de conversión por software, timer o pin externo.
- Puede apagarse para reducir el consumo.

Diagrama de bloques

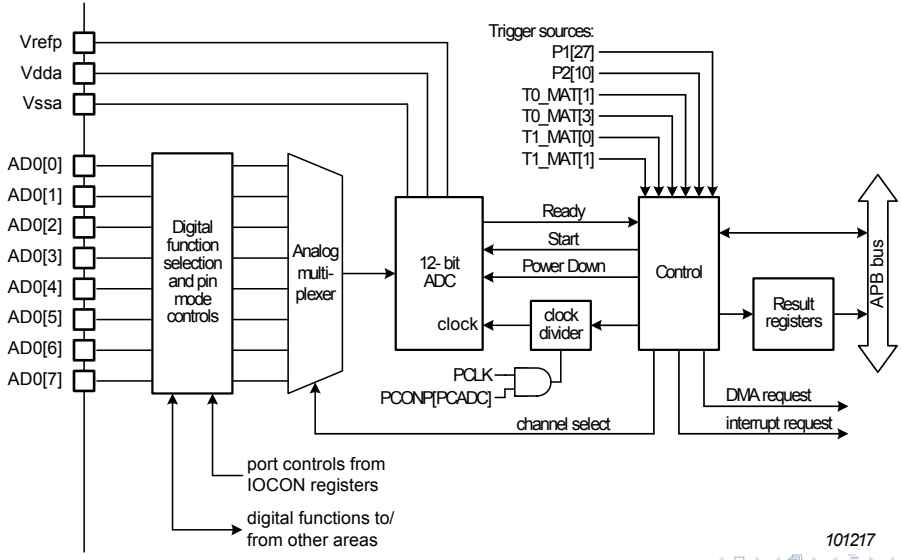


Diagrama de bloques

Table 673. Register overview: ADC (base address 0x4003 4000)

Generic Name	Access	Address offset	Description	Reset value[1]	Table
CR	R/W	0x000	A/D Control Register. The ADCR register must be written to select the operating mode before A/D conversion can occur.	1	674
GDR	R/W	0x004	A/D Global Data Register. This register contains the ADC's DONE bit and the result of the most recent A/D conversion.	NA	675
INTEN	R/W	0x00C	A/D Interrupt Enable Register. This register contains enable bits that allow the DONE flag of each A/D channel to be included or excluded from contributing to the generation of an A/D interrupt.	0x100	676
DR0	RO	0x010	A/D Channel 0 Data Register. This register contains the result of the most recent conversion completed on channel 0.	NA	677
DR1	RO	0x014	A/D Channel 1 Data Register. This register contains the result of the most recent conversion completed on channel 1.	NA	677
DR2	RO	0x018	A/D Channel 2 Data Register. This register contains the result of the most recent conversion completed on channel 2.	NA	677
DR3	RO	0x01C	A/D Channel 3 Data Register. This register contains the result of the most recent conversion completed on channel 3.	NA	677
DR4	RO	0x020	A/D Channel 4 Data Register. This register contains the result of the most recent conversion completed on channel 4.	NA	677
DR5	RO	0x024	A/D Channel 5 Data Register. This register contains the result of the most recent conversion completed on channel 5.	NA	677
DR6	RO	0x028	A/D Channel 6 Data Register. This register contains the result of the most recent conversion completed on channel 6.	NA	677
DR7	RO	0x2C	A/D Channel 7 Data Register. This register contains the result of the most recent conversion completed on channel 7.	NA	677
STAT	RO	0x030	A/D Status Register. This register contains DONE and OVERRUN flags for all of the A/D channels, as well as the A/D interrupt/DMA flag.	0	678
TRM	R/W	0x034	ADC trim register.	0	679

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

Registro de control CR

Table 674: A/D Control Register (CR - address 0x4003 4000) bit description

Bit	Symbol	Value	Description	Reset value
7:0	SEL		Selects which of the AD0[7:0] pins is (are) to be sampled and converted. For AD0, bit 0 selects Pin AD0[0], and bit 7 selects pin AD0[7]. In software-controlled mode, only one of these bits should be 1. In hardware scan mode, any value containing 1 to 8 ones is allowed. All zeroes is equivalent to 0x01.	0x01
15:8	CLKDIV		The APB clock (PCLK) is divided by (this value plus one) to produce the clock for the A/D converter, which should be less than or equal to 12.4 MHz. Typically, software should program the smallest value in this field that yields a clock of 12.4 MHz or slightly less, but in certain cases (such as a high-impedance analog source) a slower clock may be desirable.	0
16	BURST		Burst mode	0
		0	Conversions are software controlled and require 31 clocks.	
		1	The AD converter does repeated conversions at up to 400 kHz, scanning (if necessary) through the pins selected by bits set to ones in the SEL field. The first conversion after the start corresponds to the least-significant 1 in the SEL field, then higher numbered 1-bits (pins) if applicable. Repeated conversions can be terminated by clearing this bit, but the conversion that's in progress when this bit is cleared will be completed. **Remark:** START bits must be 000 when BURST = 1 or conversions will not start.	
20:17	-		Reserved. Read value is undefined, only zero should be written.	NA
21	PDN		Power down mode	0
		0	The A/D converter is in power-down mode.	
		1	The A/D converter is operational.	
23:22	-		Reserved. Read value is undefined, only zero should be written.	NA
26:24	START		When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
		0x0	No start (this value should be used when clearing PDN to 0).	
		0x1	Start conversion now.	
		0x2	Start conversion when the edge selected by bit 27 occurs on the P2[10] pin.	
		0x3	Start conversion when the edge selected by bit 27 occurs on the P1[27] pin.	
		0x4	Start conversion when the edge selected by bit 27 occurs on MAT0.1. Note that this does not require that the MAT0.1 function appear on a device pin.	
		0x5	Start conversion when the edge selected by bit 27 occurs on MAT0.3. Note that it is not possible to cause the MAT0.3 function to appear on a device pin.	
		0x6	Start conversion when the edge selected by bit 27 occurs on MAT1.0. Note that this does not require that the MAT1.0 function appear on a device pin.	
		0x7	Start conversion when the edge selected by bit 27 occurs on MAT1.1. Note that this does not require that the MAT1.1 function appear on a device pin.	
27	EDGE		This bit is significant only when the START field contains 010-111. In these cases:	0
		1	Start conversion on a falling edge on the selected CAP/MAT signal.	
		0	Start conversion on a rising edge on the selected CAP/MAT signal.	
31:28	-		Reserved. Read value is undefined, only zero should be written.	NA

Registro de datos global GDR

Table 675: A/D Global Data Register (GDR - address 0x4003 4004) bit description

Bit	Symbol	Description	Reset value
3:0	-	Reserved. Read value is undefined, only zero should be written.	NA
15:4	RESULT	When DONE is 1, this field contains a binary fraction representing the voltage on the AD0[n] pin selected by the SEL field, as it falls within the range of V_{REFP} to V_{SS}. Zero in the field indicates that the voltage on the input pin was less than, equal to, or close to that on V_{SS}, while 0xFFF indicates that the voltage on the input was close to, equal to, or greater than that on V_{REFP}.	NA
23:16	-	Reserved. Read value is undefined, only zero should be written.	NA
26:24	CHN	These bits contain the channel from which the RESULT bits were converted (e.g. 000 identifies channel 0, 001 channel 1...).	NA
29:27	-	Reserved. Read value is undefined, only zero should be written.	NA
30	OVERRUN	This bit is 1 in burst mode if the results of one or more conversions was (were) lost and overwritten before the conversion that produced the result in the RESULT bits. This bit is cleared by reading this register.	0
31	DONE	This bit is set to 1 when an A/D conversion completes. It is cleared when this register is read and when the ADCR is written. If the ADCR is written while a conversion is still in progress, this bit is set and a new conversion is started.	0

Registros de datos individuales DRx

Table 677: A/D Data Registers (DR[0:7] - addresses 0x4003 4010 (DR0) to 0x4003 402C (DR7)) bit description

Bit	Symbol	Description	Reset value
3:0	-	Reserved. Read value is undefined, only zero should be written.	NA
15:4	RESULT	When DONE is 1, this field contains a binary fraction representing the voltage on the AD0[n] pin, as it falls within the range of V_{REFP} to V_{SS}. Zero in the field indicates that the voltage on the input pin was less than, equal to, or close to that on V_{SS}, while 0xFFF indicates that the voltage on the input was close to, equal to, or greater than that on V_{REFP}.	NA
29:16	-	Reserved. Read value is undefined, only zero should be written.	NA
30	OVERRUN	This bit is 1 in burst mode if the results of one or more conversions was (were) lost and overwritten before the conversion that produced the result in the RESULT bits.This bit is cleared by reading this register.	
31	DONE	This bit is set to 1 when an A/D conversion completes. It is cleared when this register is read.	NA

Registro de interrupción INTEN

Table 676: A/D Interrupt Enable register (INTEN - address 0x4003 400C) bit description

Bit	Symbol	Value	Description	Reset value
0	ADINTEN0		Interrupt enable	0
		0	Completion of a conversion on ADC channel 0 will not generate an interrupt.	
		1	Completion of a conversion on ADC channel 0 will generate an interrupt.	
1	ADINTEN1		Interrupt enable	0
		0	Completion of a conversion on ADC channel 1 will not generate an interrupt.	
		1	Completion of a conversion on ADC channel 1 will generate an interrupt.	
2	ADINTEN2		Interrupt enable	0
		0	Completion of a conversion on ADC channel 2 will not generate an interrupt.	
		1	Completion of a conversion on ADC channel 2 will generate an interrupt.	
3	ADINTEN3		Interrupt enable	0
		0	Completion of a conversion on ADC channel 3 will not generate an interrupt.	
		1	Completion of a conversion on ADC channel 3 will generate an interrupt.	
4	ADINTEN4		Interrupt enable	0
		0	Completion of a conversion on ADC channel 4 will not generate an interrupt.	
		1	Completion of a conversion on ADC channel 4 will generate an interrupt.	
5	ADINTEN5		Interrupt enable	0
		0	Completion of a conversion on ADC channel 5 will not generate an interrupt.	
		1	Completion of a conversion on ADC channel 5 will generate an interrupt.	
6	ADINTEN6		Interrupt enable	0
		0	Completion of a conversion on ADC channel 6 will not generate an interrupt.	
		1	Completion of a conversion on ADC channel 6 will generate an interrupt.	
7	ADINTEN7		Interrupt enable	0
		0	Completion of a conversion on ADC channel 7 will not generate an interrupt.	
		1	Completion of a conversion on ADC channel 7 will generate an interrupt.	
8	ADGINTEN		Interrupt enable	1
		0	Only the individual ADC channels enabled by ADINTEN7:0 will generate interrupts.	
		1	The global DONE flag in ADDR is enabled to generate an interrupt in addition to any individual ADC channels that are enabled to generate interrupts.	
31:9	-		Reserved. Read value is undefined, only zero should be written.	NA

Registro de estado STAT

Table 678: A/D Status register (STAT - address 0x4003 4030) bit description

Bit	Symbol	Description	Reset value
0	DONE0	This bit mirrors the DONE status flag from the result register for A/D channel 0.	0
1	DONE1	This bit mirrors the DONE status flag from the result register for A/D channel 1.	0
2	DONE2	This bit mirrors the DONE status flag from the result register for A/D channel 2.	0
3	DONE3	This bit mirrors the DONE status flag from the result register for A/D channel 3.	0
4	DONE4	This bit mirrors the DONE status flag from the result register for A/D channel 4.	0
5	DONE5	This bit mirrors the DONE status flag from the result register for A/D channel 5.	0
6	DONE6	This bit mirrors the DONE status flag from the result register for A/D channel 6.	0
7	DONE7	This bit mirrors the DONE status flag from the result register for A/D channel 7.	0
8	OVERRUN0	This bit mirrors the OVERRRUN status flag from the result register for A/D channel 0.	0
9	OVERRUN1	This bit mirrors the OVERRRUN status flag from the result register for A/D channel 1.	0
10	OVERRUN2	This bit mirrors the OVERRRUN status flag from the result register for A/D channel 2.	0
11	OVERRUN3	This bit mirrors the OVERRRUN status flag from the result register for A/D channel 3.	0
12	OVERRUN4	This bit mirrors the OVERRRUN status flag from the result register for A/D channel 4.	0
13	OVERRUN5	This bit mirrors the OVERRRUN status flag from the result register for A/D channel 5.	0
14	OVERRUN6	This bit mirrors the OVERRRUN status flag from the result register for A/D channel 6.	0
15	OVERRUN7	This bit mirrors the OVERRRUN status flag from the result register for A/D channel 7.	0
16	ADINT	This bit is the A/D interrupt flag. It is one when any of the individual A/D channel Done flags is asserted and enabled to contribute to the A/D interrupt via the ADINTEN register.	0
31:17	-	Reserved. Read value is undefined, only zero should be written.	NA

Registro de ajuste TRM

Table 679: A/D Trim register (TRM - address 0x4003 4034) bit description

Bit	Symbol	Description	Reset value
3:0	-	Reserved. Read value is undefined, only zero should be written.	NA
7:4	ADCOFFS	Offset trim bits for ADC operation. Initialized by the boot code. Can be overwritten by the user.	0
11:8	TRIM	written-to by boot code. Can **not** be overwritten by the user. These bits are locked after boot code write.	0
31:12	-	Reserved. Read value is undefined, only zero should be written.	NA

Control de consumo en el registro PCONP

Table 16. Power Control for Peripherals register (PCONP - address 0x400F C0C4) bit description

Bit	Symbol	Description	Reset value
0	PCLCD	LCD controller power/clock control bit.	0
1	PCTIM0	Timer/Counter 0 power/clock control bit.	1
2	PCTIM1	Timer/Counter 1 power/clock control bit.	1
3	PCUART0	UART0 power/clock control bit.	1
4	PCUART1	UART1 power/clock control bit.	1
5	PCPWM0	PWM0 power/clock control bit.	0
6	PCPWM1	PWM1 power/clock control bit.	0
7	PCI2C0	I^2C0 interface power/clock control bit.	1
8	PCUART4	UART4 power/clock control bit.	0
9	PCRTC	RTC and Event Monitor/Recorder power/clock control bit.	1
10	PCSSP1	SSP 1 interface power/clock control bit.	0
11	PCEMC	External Memory Controller power/clock control bit.	0
12	PCADC	A/D converter (ADC) power/clock control bit. **Note:** Clear the PDN bit in the AD0CR before clearing this bit, and set this bit before attempting to set PDN.	0
13	PCCAN1	CAN Controller 1 power/clock control bit.	0
14	PCCAN2	CAN Controller 2 power/clock control bit.	0
15	PCGPIO	Power/clock control bit for IOCON, GPIO, and GPIO interrupts.	1
16	PCSPIFI	SPI Flash Interface power/clock control bit.	0
17	PCMCPWM	Motor Control PWM power/clock control bit.	0
18	PCQEI	Quadrature Encoder Interface power/clock control bit.	0
19	PCI2C1	I^2C1 interface power/clock control bit.	1
20	PCSSP2	SSP2 interface power/clock control bit.	0
21	PCSSP0	SSP0 interface power/clock control bit.	0
22	PCTIM2	Timer 2 power/clock control bit.	0
23	PCTIM3	Timer 3 power/clock control bit.	0
24	PCUART2	UART 2 power/clock control bit.	0
25	PCUART3	UART 3 power/clock control bit.	0
26	PCI2C2	I^2C interface 2 power/clock control bit.	1
27	PCI2S	I^2S interface power/clock control bit.	0
28	PCSDC	SD Card interface power/clock control bit.	0
29	PCGPDMA	GPDMA function power/clock control bit.	0
30	PCENET	Ethernet block power/clock control bit.	0
31	PCUSB	USB interface power/clock control bit.	0

Pasos para configurar el ADC

1. En el registro `PCONP`: poner a 1 el bit `PCADC` (bit 12).
2. En el registro `CR` del ADC:
   - Poner a 1 el bit `PDN` (bit 21).
   - Programar `CLKDIV` (bits 8 a 15) para que reloj $\leq$ 12.4 MHz.
3. En los registros `IOCON` de los pines de entrada analógicos que se vayan a usar:
   - Seleccionar entrada analógica en el campo `FUNC` (bits 0 a 3).
   - Poner a cero el bit `ADMODE` (bit 7).

Función de configuración

```
void adc_inicializar(uint32_t frecuencia_adc, uint32_t canales)
{
    const uint32_t puertos[8] =   { 0,  0,  0,  0,  1,  1,  0,  0}; /* Puerto donde está cada canal analógico. */
    const uint32_t pines[8] =     {23, 24, 25, 26, 30, 31, 12, 13}; /* Pin donde está cada canal analógico. */
    const uint32_t funciones[8] = { 1,  1,  1,  1,  3,  3,  3,  3}; /* Número de función para registros IOCON. */
    uint32_t i;
    volatile uint32_t *iocon_reg;

    ASSERT(frecuencia_adc >= PeripheralClock/255, "Frecuencia ADC demasiado baja.");
    ASSERT(frecuencia_adc < 12400000, "Frecuencia ADC debe ser < 12500000.");
    ASSERT(canales < 256, "Canales incorrectos.");

    LPC_SC->PCONP |= 1u << 12;  /* Activar el bit PCADC en el registro PCONP. */

    LPC_ADC->CR = (1u << 21) | ((PeripheralClock/frecuencia_adc - 1) << 8); /* CR:  activar PDN, ajustar CLKDIV según frecuencia_adc. */

    for (i = 0; i < 8; i++) /* Configurar como entradas analógicas los pines indicados por canales. */
    {
        if (canales & (1u << i))
        {
            iocon_reg = ((uint32_t*)LPC_IOCON) + puertos[i]*32 + pines[i];
            *iocon_reg = funciones[i];
        }
    }
}
```

Realización de conversiones controladas por software

1. En el registro `CR` del ADC:
   - Poner a 1 el bit del campo `SEL` (bits 0 a 7) correspondiente al canal que se desea convertir. Poner el resto del campo `SEL` a 0.
   - Iniciar la conversión poniendo a 1 el bit 24.
2. Esperar hasta que bit `DONE` (bit 31) del registro `GDR` del ADC se ponga a 1.
3. Recoger el resultado del campo `RESULT` (bits 3 a 15) del registro `GDR` del ADC.

```
uint32_t adc_convertir(uint32_t canal)
{
    ASSERT(canal <= 7, "Canal ADC incorrecto");
    LPC_ADC->CR = (LPC_ADC->CR & 0xFFFFFF00) | (1u << canal) | (1u << 24);
    while ((LPC_ADC->GDR & (1u << 31)) == 0) {}
    return (LPC_ADC->GDR >> 4) & 0xFFF;
}
```

Tensión de entrada en función del resultado del ADC

Relación entre resultado y tensión de entrada

$$Q = \frac{V_{FS}}{2^N} = \frac{V_{REFP}}{2^N}$$

$$V_{ADCIN} = Q \cdot RESULT_{ADC} \pm \frac{1}{2} \cdot Q$$

donde:

- Q Cuanto del convertidor.
- V_{REFP} tensión de referencia aplicada a la patilla VREFP. La tensión de fondo de escala (V_{FS}) es igual a V_{REFP}
- N número de bits de resolución del ADC.
- V_{ADCIN} tensión aplicada a la entrada del ADC.
- $RESULT_{ADC}$ dato obtenido como resultado de la conversión.

Tensión de entrada en función del resultado del ADC

Sustituyendo $V_{REFP} = 3.3$, $N = 12$

$$V_{ADCIN} = \frac{3.3}{4096} \cdot RESULT_{ADC} \pm \frac{1}{2} \cdot \frac{3.3}{4096}$$