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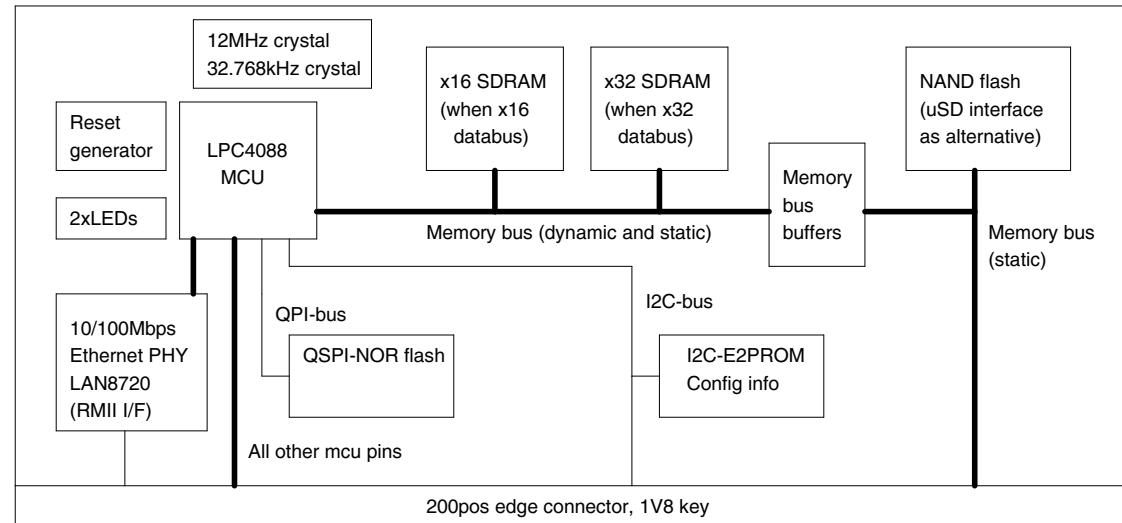
NAND flash

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LEDs and configuration I2C-E2PROM

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SODIMM edge connector



UL = UnLoaded = normally not mounted component.

Default jumper settings are indicated in the schematic.
However, always check jumper positions on actual boards
since there is no guarantee that all jumpers are in default place.

Rev B

Changed Ethernet PHY reset to RESET_IN.
Changed C35 to 470pF and R22 to 2K.

Rev A

Added pull-up on P5.2 and P5.3. Added R100.
Removed SJ12, SJ14, SJ15, SJ16.

Rev PA1

First revision



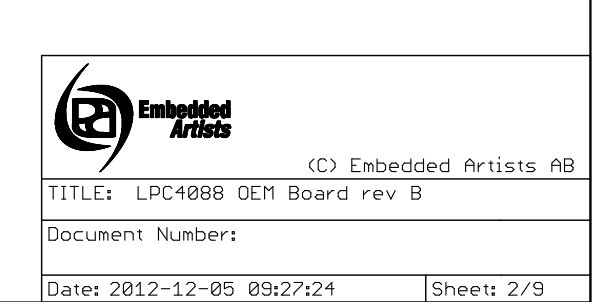
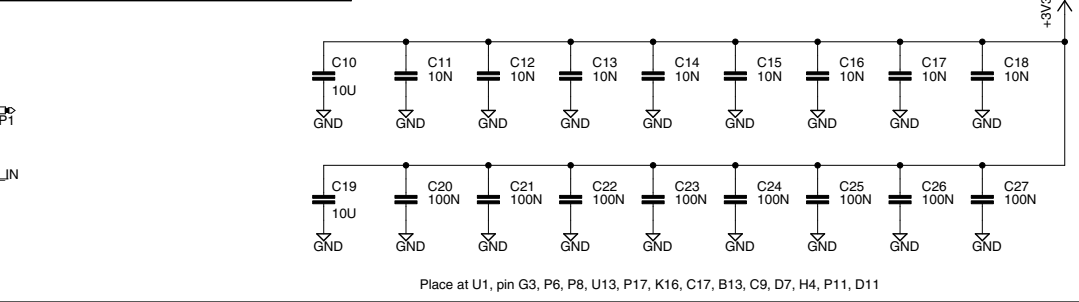
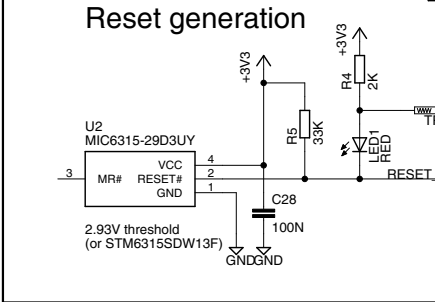
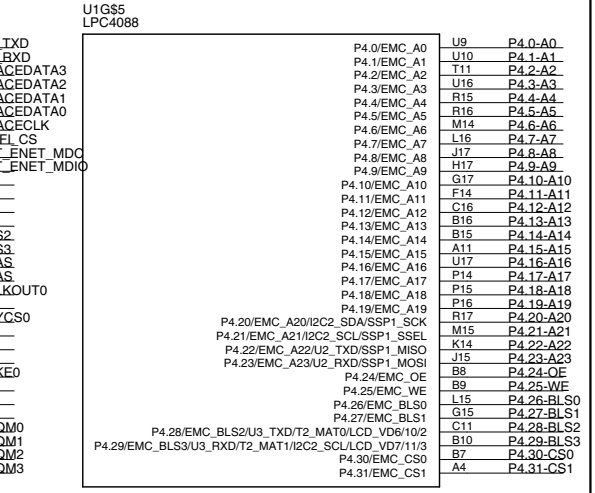
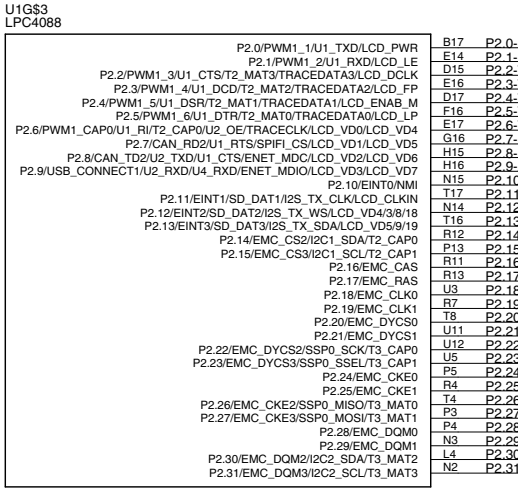
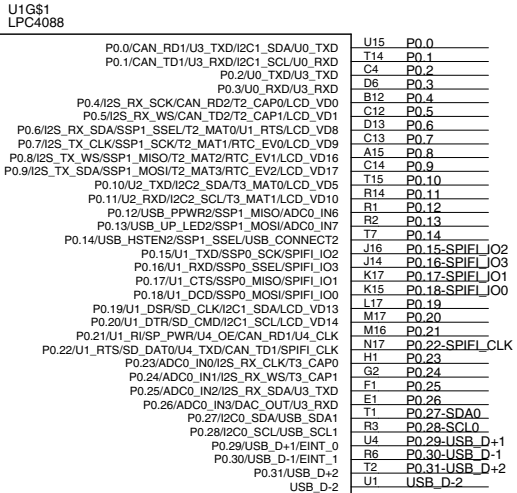
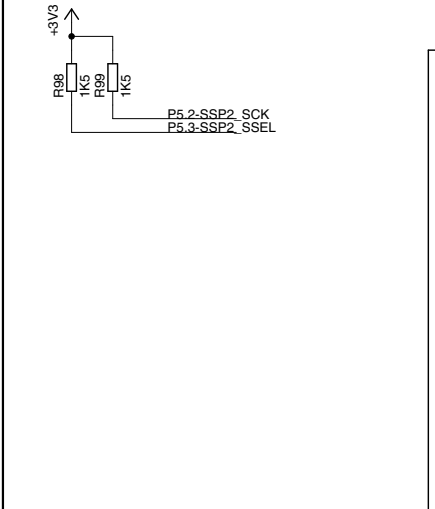
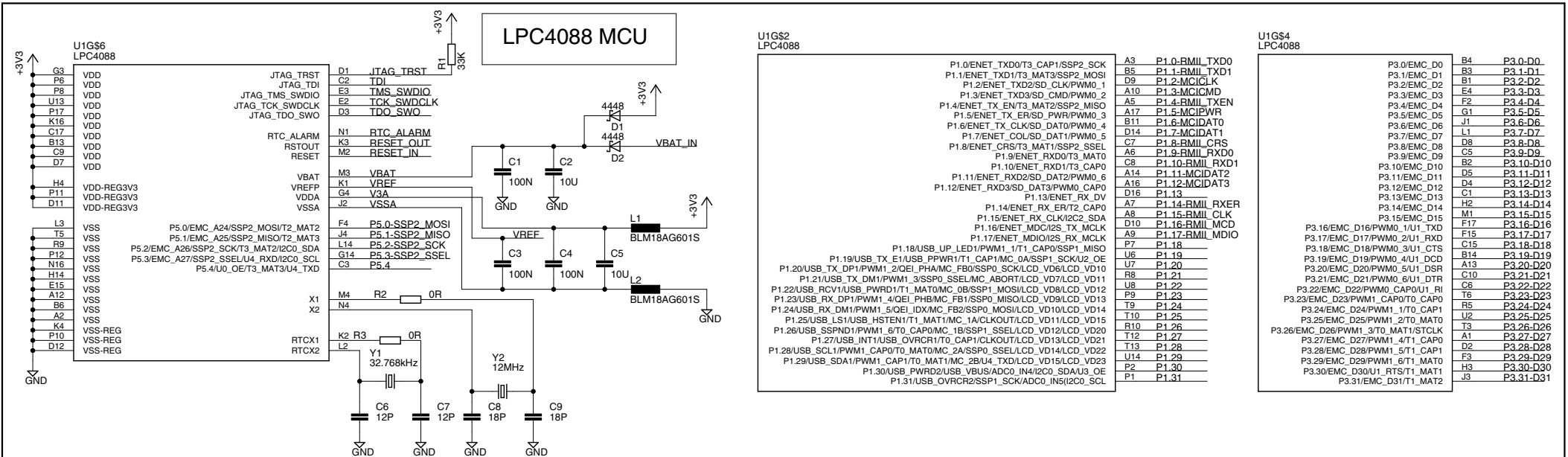
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Document Number:

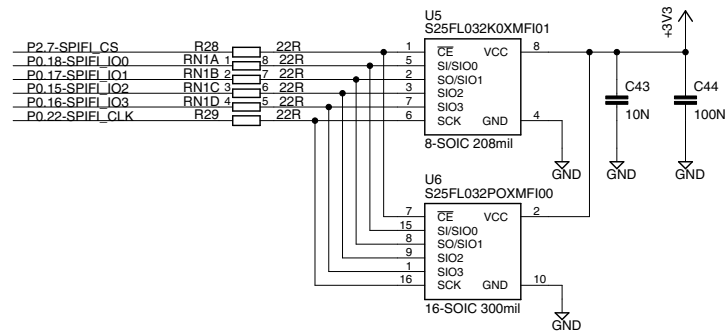
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QSPI FLASH

32Mbit QSPI Flash (SPIFI)



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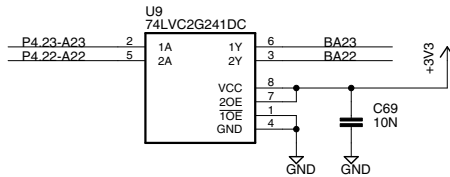
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Buffers for external memory bus

Address and Control Buffers

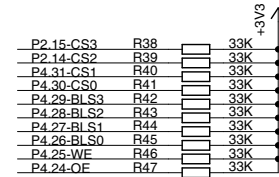
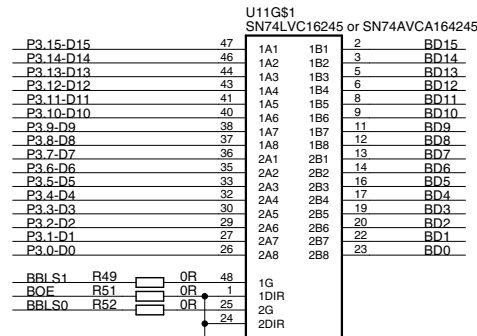
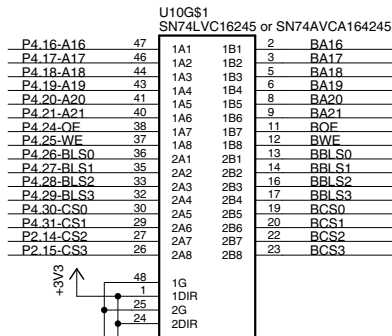


Databus Buffers

Pullups

Buffered bus for static memories:

CS0 = 0x8000 0000 - 0x83FF FFFF
 CS1 = 0x9000 0000 - 0x93FF FFFF
 CS2 = 0x9800 0000 - 0x9BFF FFFF
 CS3 = 0x9C00 0000 - 0x9FFF FFFF

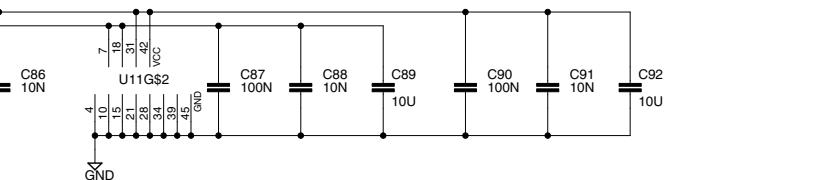
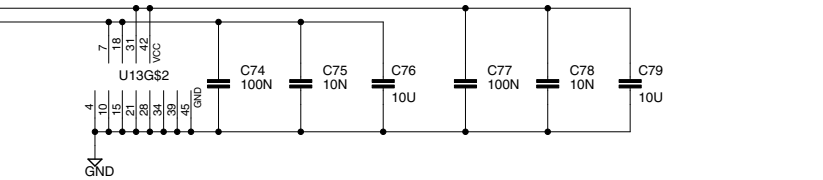
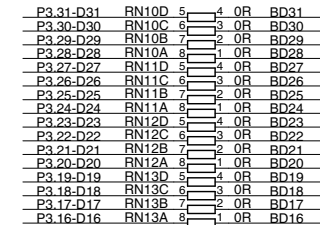
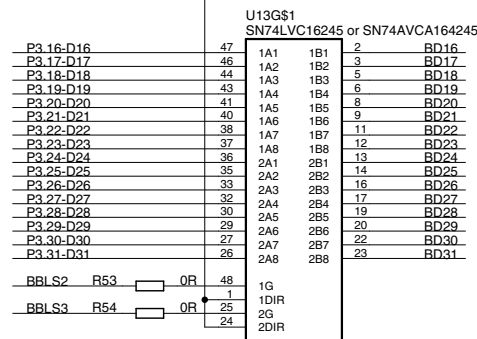


Boot control (not used)



32-bit databus version (P3.16 - P3.31 are buffered)

16-bit databus version (P3.16 - P3.31 are not buffered)



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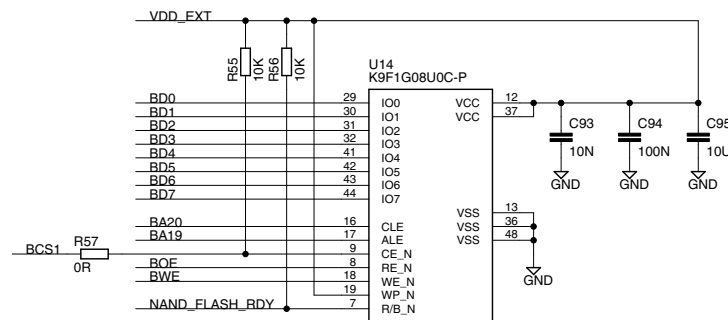
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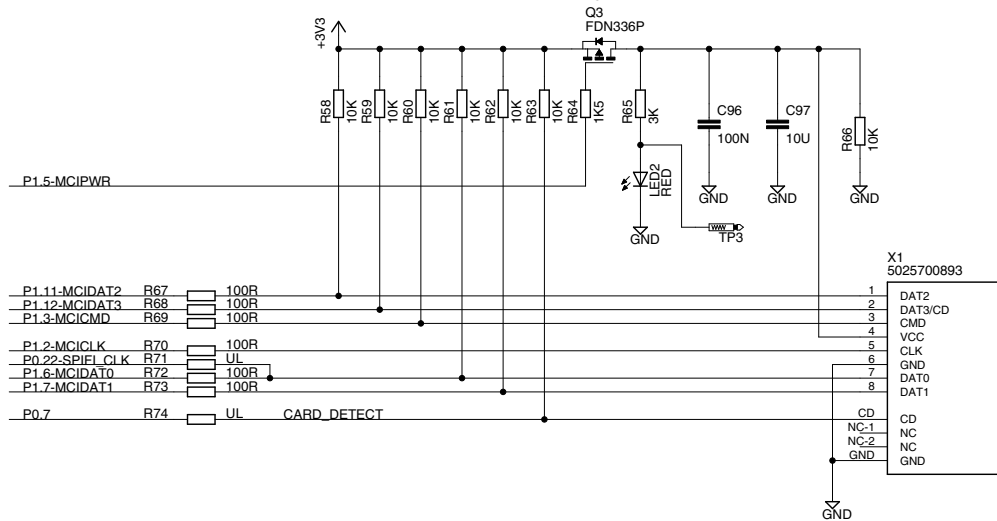
NAND Flash memory (on buffered bus)

1Gbit (128MByte) NAND FLASH
(CS1 = 0x9000 0000 - 0x93FF FFFF)



U16 and X3 on overlapping pads (cannot be mounted simultaneously)

uSD/Transflash Memory Card I/F
(normally not mounted)



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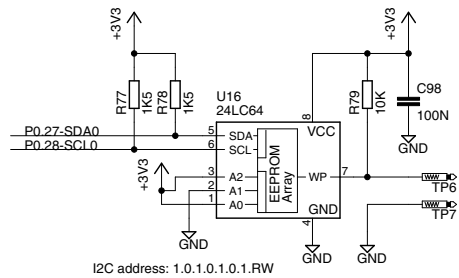
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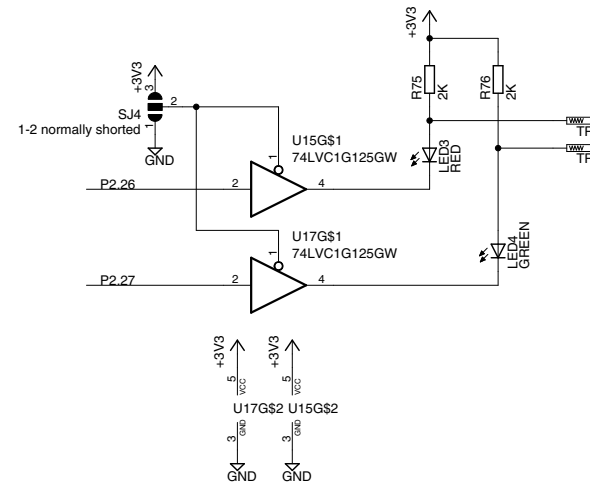
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Configuration I2C-E2PROM and LEDs

64kbit Configuration EEPROM (write protected)



LEDs



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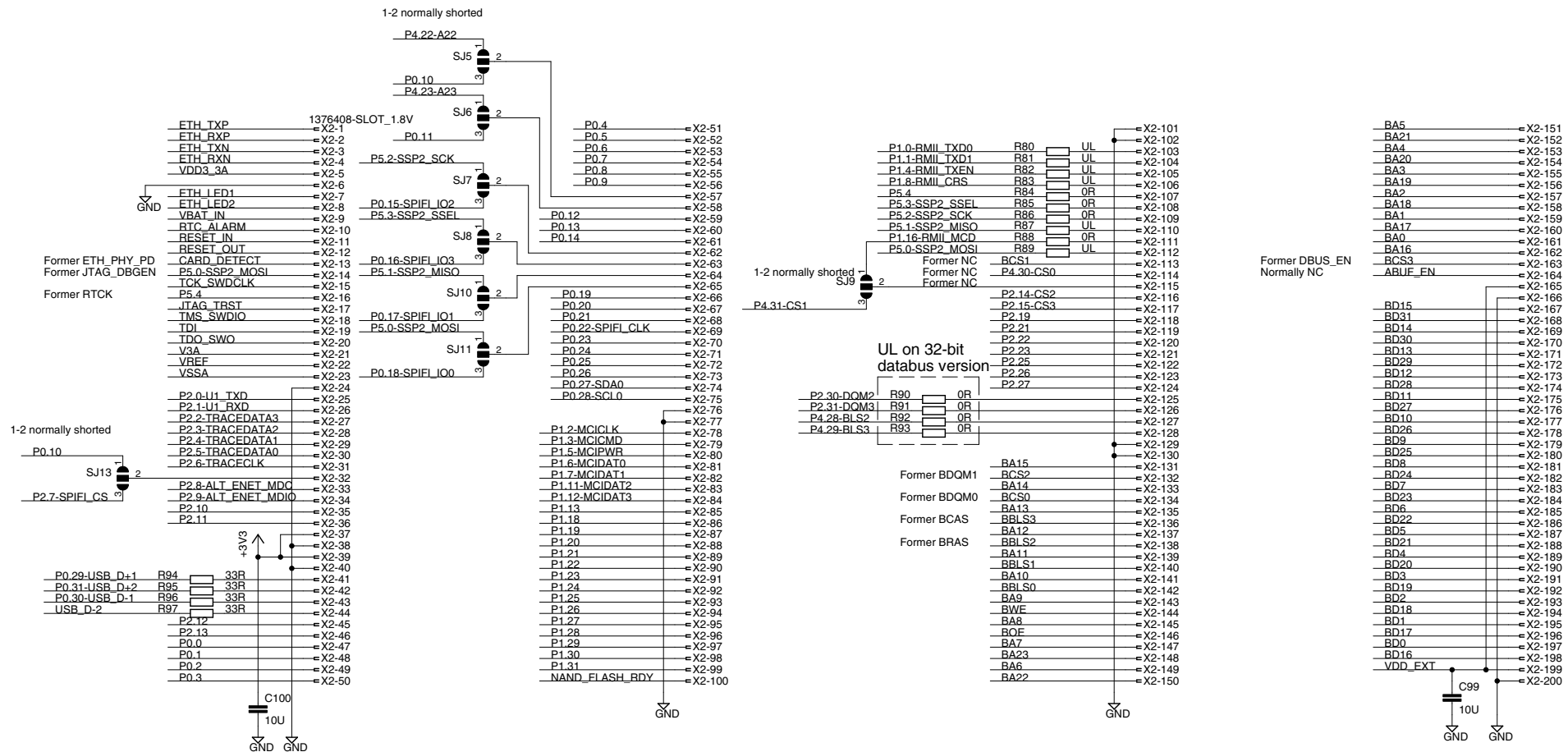
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Expansion Connector (SODIMM Edge Connector)



Note: P2.7 position replaced by P0.10 (since P2.7 used by SPIFI).

Note: SSP0 pins replaced by SSP2 pins (since SSP0 pins used by SPIFI).

Note P0.10/11 replaced by P4.22/23 (since P0.10/11 used for LCD).



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