UARTs del LPC4088

Diseño Basado en Microprocesadores

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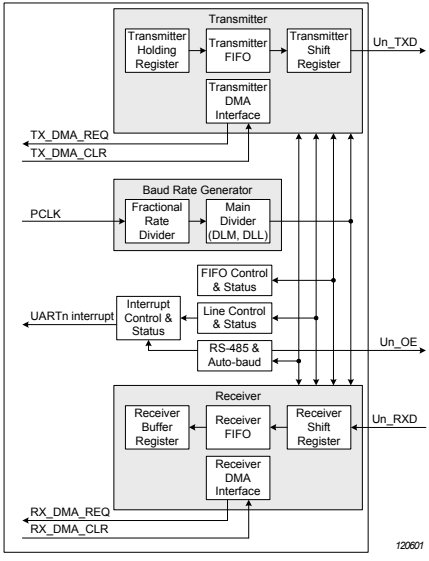
Contenido

UARTs del microcontrolador LPC4088

- Cinco UARTs: UART0 a UART4.
- Sólo la UART1 tiene señales de protocolo DTR, DSR, RTS, CTS, DCD y RI.
- Buffers FIFO.
- DMA.
- Modo IrDA para comunicación por infrarrojos.
- UART4: modo Smart Card para conunicación con tarjetas inteligentes.
- Las UARTs 0 y 1 están alimentadas por defecto.
- Las UARTs 2, 3 y 4 están apagadas por defecto.
- Estudiaremos las UART0/2/3 por ser las más sencillas.

Diagrama de bloques de la UART0/2/3



Pines de la UART0/2/3

Table 386: UARTn Pin description

Pin	Type	Description
U0_RXD, U2_RXD, U3_RXD	Input	**Serial Input.** Serial receive data.
U0_TXD, U2_TXD, U3_TXD	Output	**Serial Output.** Serial transmit data.
U0_OE, U2_OE, U3_OE	Output	**Output Enable.** RS-485/EIA-485 output enable.

Registros de la UART0/2/3

Table 387. Register overview: UART0/2/3 (base address: 0x4000 C000, 0x4008 8000, 0x4009 C000)

Name	Access	Address offset	Description	Reset value[1]	Table
RBR	RO	0x000	Receiver Buffer Register. Contains the next received character to be read .	NA	388
THR	WO	0x000	Transmit Holding Register. The next character to be transmitted is written here (DLAB =0).	NA	389
DLL	R/W	0x000	Divisor Latch LSB. Least significant byte of the baud rate divisor value. The full divisor is used to generate a baud rate from the fractional rate divider (DLAB =1).	0x01	390
DLM	R/W	0x004	Divisor Latch MSB. Most significant byte of the baud rate divisor value. The full divisor is used to generate a baud rate from the fractional rate divider (DLAB =1).	0	391
IER	R/W	0x004	Interrupt Enable Register. Contains individual interrupt enable bits for the 7 potential UART interrupts (DLAB =0).	0	392
IIR	RO	0x008	Interrupt ID Register. Identifies which interrupt(s) are pending.	0x01	393
FCR	WO	0x008	FIFO Control Register. Controls UART FIFO usage and modes.	0	395
LCR	R/W	0x00C	Line Control Register. Contains controls for frame formatting and break generation.	0	396
-	-	0x010	Reserved.	-	-
LSR	RO	0x014	Line Status Register. Contains flags for transmit and receive status, including line errors.	0x60	397
-	-	0x018	Reserved.	-	-
SCR	R/W	0x01C	Scratch Pad Register. 8-bit temporary storage for software.	0	398
ACR	R/W	0x020	Auto-baud Control Register. Contains controls for the auto-baud feature.	0	399
FDR	R/W	0x028	Fractional Divider Register. Generates a clock input for the baud rate divider.	0x10	400
-	-	0x02C	Reserved.	-	-
TER	R/W	0x030	Transmit Enable Register. Turns off UART transmitter for use with software flow control.	0x80	402
-	-	0x034 to 0x048	Reserved.	-	-
RS485CTRL	R/W	0x04C	RS-485/EIA-485 Control. Contains controls to configure various aspects of RS-485/EIA-485 modes.	0	403
RS485 ADRMATCH	R/W	0x050	RS-485/EIA-485 address match. Contains the address match value for RS-485/EIA-485 mode.	0	404
RS485DLY	R/W	0x054	RS-485/EIA-485 direction control delay.	0	405

Registros RBR y THR

- RBR (Receive Buffer Register): contiene el dato más antiguo recibido por la UART.

Table 388: UARTn Receiver Buffer Register when DLAB = 0, read only (RBR - address 0x4000 C000 (UART0), 0x4009 8000 (UART2), 04009 C000 (UART3)) bit description

Bit	Symbol	Description	Reset Value
7:0	RBR	The UARTn Receiver Buffer Register contains the oldest received byte in the UARTn Rx FIFO.	Undefined
31:8	-	Reserved, the value read from a reserved bit is not defined.	NA

- THR (Transmit Holding Register): el dato escrito en este registro entra en la FIFO de transmisión.

Table 389: UARTn Transmit Holding Register when DLAB = 0, write only (THR - address 0x4000 C000 (UART0), 0x4009 8000 (UART2), 0x4009 C000 (UART3)) bit description

Bit	Symbol	Description
7:0	THR	Writing to the UARTn Transmit Holding Register causes the data to be stored in the UARTn transmit FIFO. The byte will be sent when it reaches the bottom of the FIFO and the transmitter is available.
31:8	-	Reserved. Read value is undefined, only zero should be written.

Registros divisores de reloj DLL y DLM

- Dividen el reloj PCLK para obtener la tasa de comunicación en baudios.
- Para acceder a ellos debe activarse el bit DLAB del registro LCR.

Table 390: UARTn Divisor Latch LSB register when DLAB = 1 (DLL - address 0x4000 C000 (UART0), 0x4009 8000 (UART2), 0x4009 C000 (UART3)) bit description

Bit	Symbol	Description	Reset Value
7:0	DLLSB	The UARTn Divisor Latch LSB Register, along with the UnDLM register, determines the baud rate of the UARTn.	0x01
31:8	-	Reserved. Read value is undefined, only zero should be written.	NA

Table 391: UARTn Divisor Latch MSB register when DLAB = 1 (DLM - address 0x4000 C004 (UART0), 0x4009 8004 (UART2), 0x4009 C004 (UART3)) bit description

Bit	Symbol	Description	Reset Value
7:0	DLMSB	The UARTn Divisor Latch MSB Register, along with the U0DLL register, determines the baud rate of the UARTn.	0
31:8	-	Reserved. Read value is undefined, only zero should be written.	NA

Registro Fractional Divider Register FDR

- Añaden una parte fraccionaria al factor de división conseguido con DLL y DLM.

Table 400: UARTn Fractional Divider Register (FDR - address 0x4000 C028 (UART0), 0x4009 8028 (UART2), 0x4009 C028 (UART3)) bit description

Bit	Function	Value	Description	Reset value
3:0	DIVADDVAL	0	Baud Rate generation pre-scaler divisor value. If this field is 0, fractional baud rate generator will not impact the UARTn baud rate.	0
7:4	MULVAL	1	Baud Rate pre-scaler multiplier value. This field must be greater or equal 1 for UARTn to operate properly, regardless of whether the fractional baud rate generator is used or not.	1
31:8	-		Reserved. Read value is undefined, only zero should be written.	0

- La tasa en baudios resultante es

$$UART_{baudrate} = \frac{PCLK}{16 \cdot (256 \cdot DLM + DLL) \cdot \left(1 + \frac{DIVADDVAL}{MULVAL}\right)}$$

Registro Line Control Register LCR

Table 396: UARTn Line Control Register (LCR - address 0x4000 C00C (UART0), 0x4009 800C (UART2), 0x4009 C00C (UART3)) bit description

Bit	Symbol	Value	Description	Reset Value
1:0	WLS		Word Length Select.	0
		0x0	5-bit character length	
		0x1	6-bit character length	
		0x2	7-bit character length	
		0x3	8-bit character length	
2	SBS		Stop Bit Select	0
		0	1 stop bit.	
		1	2 stop bits (1.5 if UnLCR[1:0]=00).	
3	PE		Parity Enable.	0
		0	Disable parity generation and checking.	
		1	Enable parity generation and checking.	
5:4	PS		Parity Select	0
		0x0	Odd parity. Number of 1s in the transmitted character and the attached parity bit will be odd.	
		0x1	Even Parity. Number of 1s in the transmitted character and the attached parity bit will be even.	
		0x2	Forced 1 stick parity.	
		0x3	Forced 0 stick parity.	
6	BC		Break Control	0
		0	Disable break transmission.	
		1	Enable break transmission. Output pin UARTn TXD is forced to logic 0 when UnLCR[6] is active high.	
7	DLAB		Divisor Latch Access Bit	0
		0	Disable access to Divisor Latches.	
		1	Enable access to Divisor Latches.	
31:8	-		Reserved. Read value is undefined, only zero should be written.	NA

Registro Line Status Register LSR

Table 397: UARTn Line Status Register (LSR - address 0x4000 C014 (UART0), 0x4009 8014 (UART2), 0x4009 C014 (UART3)) bit description

Bit	Symbol	Value	Description	Reset Value
0	RDR		Receiver Data Ready. UnLSR[0] is set when the UnRBR holds an unread character and is cleared when the UARTn RBR FIFO is empty.	0
		0	The UARTn receiver FIFO is empty.	
		1	The UARTn receiver FIFO is not empty.	
1	OE		Overrun Error. The overrun error condition is set as soon as it occurs. An UnLSR read clears UnLSR[1]. UnLSR[1] is set when UARTn RSR has a new character assembled and the UARTn RBR FIFO is full. In this case, the UARTn RBR FIFO will not be overwritten and the character in the UARTn RSR will be lost.	0
		0	Overrun error status is inactive.	
		1	Overrun error status is active.	
2	PE		Parity Error. When the parity bit of a received character is in the wrong state, a parity error occurs. An UnLSR read clears UnLSR[2]. Time of parity error detection is dependent on UnFCR[0]. **Note:** A parity error is associated with the character at the top of the UARTn RBR FIFO.	0
		0	Parity error status is inactive.	
		1	Parity error status is active.	
3	FE		Framing Error. When the stop bit of a received character is a logic 0, a framing error occurs. An UnLSR read clears UnLSR[3]. The time of the framing error detection is dependent on UnFCR[0]. Upon detection of a framing error, the Rx will attempt to resynchronize to the data and assume that the bad stop bit is actually an early start bit. However, it cannot be assumed that the next received byte will be correct even if there is no Framing Error. **Note:** A framing error is associated with the character at the top of the UARTn RBR FIFO.	0
		0	Framing error status is inactive.	
		1	Framing error status is active.	
4	BI		Break Interrupt. When RXDn is held in the spacing state (all zeroes) for one full character transmission (start, data, parity, stop), a break interrupt occurs. Once the break condition has been detected, the receiver goes idle until RXDn goes to marking state (all ones). An UnLSR read clears this status bit. The time of break detection is dependent on UnFCR[0]. **Note:** The break interrupt is associated with the character at the top of the UARTn RBR FIFO.	0
		0	Break interrupt status is inactive.	
		1	Break interrupt status is active.	
5	THRE		Transmitter Holding Register Empty. THRE is set immediately upon detection of an empty UARTn THR and is cleared on a UnTHR write.	1
		0	UnTHR contains valid data.	
		1	UnTHR is empty.	
6	TEMT		Transmitter Empty. TEMT is set when both UnTHR and UnTSR are empty; TEMT is cleared when either the UnTSR or the UnTHR contain valid data.	1
		0	UnTHR and/or the UnTSR contains valid data.	
		1	UnTHR and the UnTSR are empty.	

Registro Line Status Register LSR (continuación)

Table 397: UARTn Line Status Register (LSR - address 0x4000 C014 (UART0), 0x4009 8014 (UART2), 0x4009 C014 (UART3)) bit description

Bit	Symbol	Value	Description	Reset Value
7	RXFE		Error in RX FIFO . UnLSR[7] is set when a character with a Rx error such as framing error, parity error or break interrupt, is loaded into the UnRBR. This bit is cleared when the UnLSR register is read and there are no subsequent errors in the UARTn FIFO.	0
		0	UnRBR contains no UARTn RX errors or UnFCR[0]=0.	
		1	UARTn RBR contains at least one UARTn RX error.	
31:8	-		Reserved. The value read from a reserved bit is not defined.	NA

Registro FIFO Control Register FCR

Table 395: UARTn FIFO Control Register, write only (FCR - address 0x4000 C008 (UART0), 0x4009 8008 (UART2), 0x4007 C008 (UART3)) bit description

Bit	Symbol	Value	Description	Reset Value
0	FIFOEN		FIFO Enable.	0
		0	UARTn FIFOs are disabled. Must not be used in the application.	
		1	Active high enable for both UARTn Rx and TX FIFOs and UnFCR[7:1] access. This bit must be set for proper UART operation. Any transition on this bit will automatically clear the related UART FIFOs.	
1	RXFIFORES		RX FIFO Reset.	0
		0	No impact on either of UARTn FIFOs.	
		1	Writing a logic 1 to UnFCR[1] will clear all bytes in UARTn Rx FIFO, reset the pointer logic. This bit is self-clearing.	
2	TXFIFORES		TX FIFO Reset.	0
		0	No impact on either of UARTn FIFOs.	
		1	Writing a logic 1 to UnFCR[2] will clear all bytes in UARTn TX FIFO, reset the pointer logic. This bit is self-clearing.	
3	DMAMODE		DMA Mode Select. When the FIFO enable (bit 0 of this register) is set, this bit selects the DMA mode. See Section 18.6.6.1.	0
5:4	-		Reserved. Read value is undefined, only zero should be written.	NA
7:6	RXTRIGLVL		RX Trigger Level. These two bits determine how many receiver UARTn FIFO characters must be written before an interrupt or DMA request is activated.	0
		0x0	Trigger level 0 (1 character or 0x01).	
		0x1	Trigger level 1 (4 characters or 0x04).	
		0x2	Trigger level 2 (8 characters or 0x08).	
		0x3	Trigger level 3 (14 characters or 0x0E).	
31:8	-		Reserved. Read value is undefined, only zero should be written.	NA