Microproject Report

221TEC007 (FPGA Based System Desgin)

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Semester :01

Stream: VLSI And Embedded systems

UART Factorial Calculator

INTRODUCTION

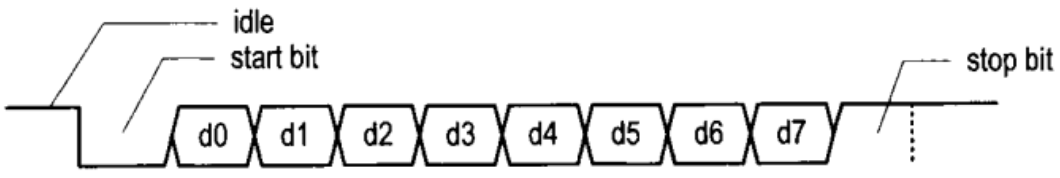
A universal asynchronous receiver and transmitter (UART) is a circuit that sends parallel data through a serial line. UARTs are frequently used in conjunction with the EIA (Electronic Industries Alliance) RS-232 standard, which specifies the electrical, mechanical, functional, and procedural characteristics of two data communication equipment. The main function of UART is to serial data communication. In serial data communication, the data can be transferred through a single cable or line in a bit- by- bit form and it requires just two cables. Serial data communication is not expensive when we compared with parallel communication.

It requires very less circuitry as well as wires. Thus, this communication is very useful in compound circuits compared with parallel communication. For this, simply two cables are required to communicate between two UARTs. The flow of data will be from both the transmitting (Tx) & receiving (Rx) pins of the UARTs. In UART, the data transmission from Tx UART to Rx UART can be done asynchronously. The data transmission of a UART can be done by using a data bus in the form of parallel by other devices like a microcontroller, memory, CPU, etc. After receiving the parallel data from the bus, it forms a data packet by adding three bits like start, stop and parity. It reads the data packet bit by bit and converts the received data into the parallel form to eliminate the three bits of the data packet.

A UART includes a transmitter and a receiver.

- The transmitter is essentially a special shift register that loads data in parallel and then shifts it out bit by bit at a specific rate.
- The receiver, on the other hand, shifts in data bit by bit and then reassembles the data

Transmission with 8 data bits, no parity, and 1 stop bit is shown in Figure 1. Note that the LSB of the data word is transmitted first. No clock information is conveyed through the serial line. Before the transmission starts, the transmitter and receiver must agree on a set of parameters in advance, which include the baud rate (i.e., number of bits per second), the number of data bits and stop bits, and use of the parity bit.



“ The "UART-Controlled Factorial Calculator Numbers" is a project that combines the power of digital logic design and serial communication to calculate the Factorial of a integers. This project is implemented using Verilog HDL and leverages the Universal Asynchronous Receiver/Transmitter (UART) protocol to facilitate communication between the user and the system. ”

OBJECTIVES

The primary objectives of this project are:

- To design and simulate a Verilog-based Factorial calculator.
- To utilize the UART protocol for user input and output communication.
- To explore and demonstrate the efficient use of hardware description language for arithmetic computations.
- To provide a real-time, interactive simulation platform for computing the Factorial numbers.

METHODOLOGY

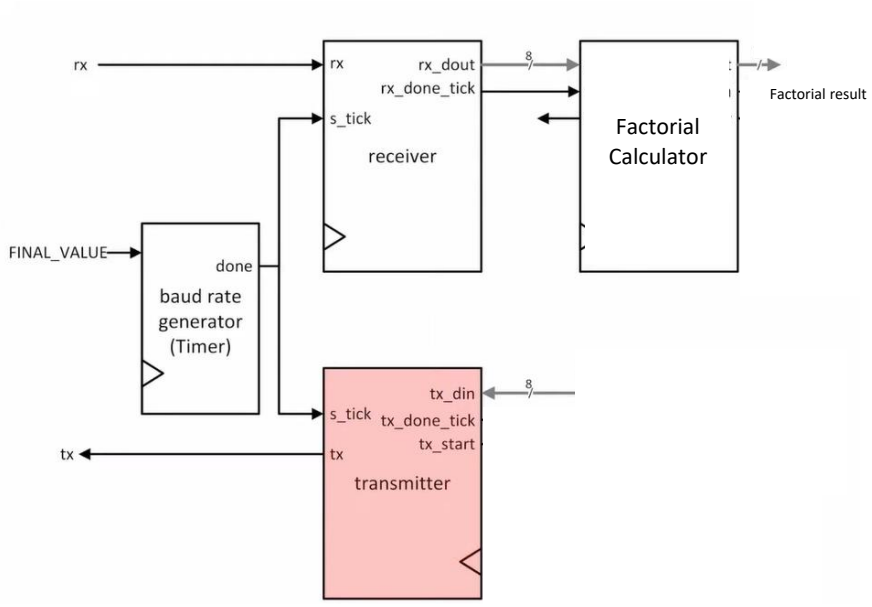
- The project started by defining requirements, focusing on UART communication and Factorial calculation.
- algorithm was implemented in Verilog to iteratively compute the Factorial.
- UART transmitter and receiver modules were developed to handle serial communication, ensuring proper data framing and synchronization.
- These modules were integrated with the Factorial computation logic to enable seamless data transfer.
- A tb module was designed to check the overall system operation.
- Extensive simulation was performed to validate the design, ensuring correct data transmission, computation, and result output.

Algorithm: Factorial Calculator

1. **Start**
2. **Input: Accept an integer n from the user.**
3. **Initialize: Set result = 1.**
4. **Calculate Factorial:**
    - **For each integer i from 1 to n:**
        - **Multiply result by i.**
        - **Update result = result * i.**
5. **Output: Print the value of result.**
6. **End**

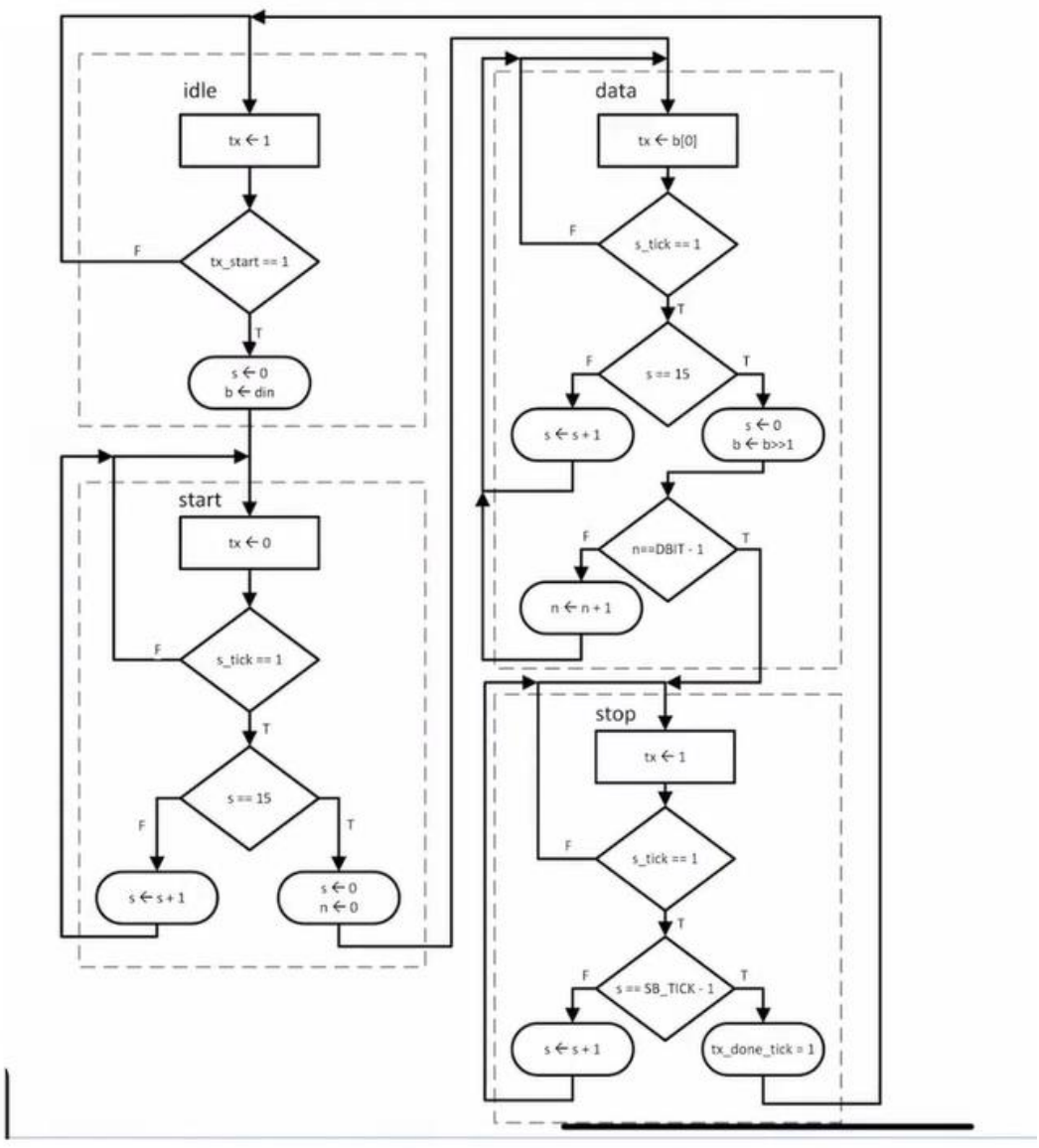
BLOCK DIAGRAM

The block diagram shows that the Factorial calculator using UART,it consist of Transmitter and Receiver and Calculator blocks. Transmitter transmits the data and receiver receives the data and calculation operations will be done and displayed in the Factorial result.

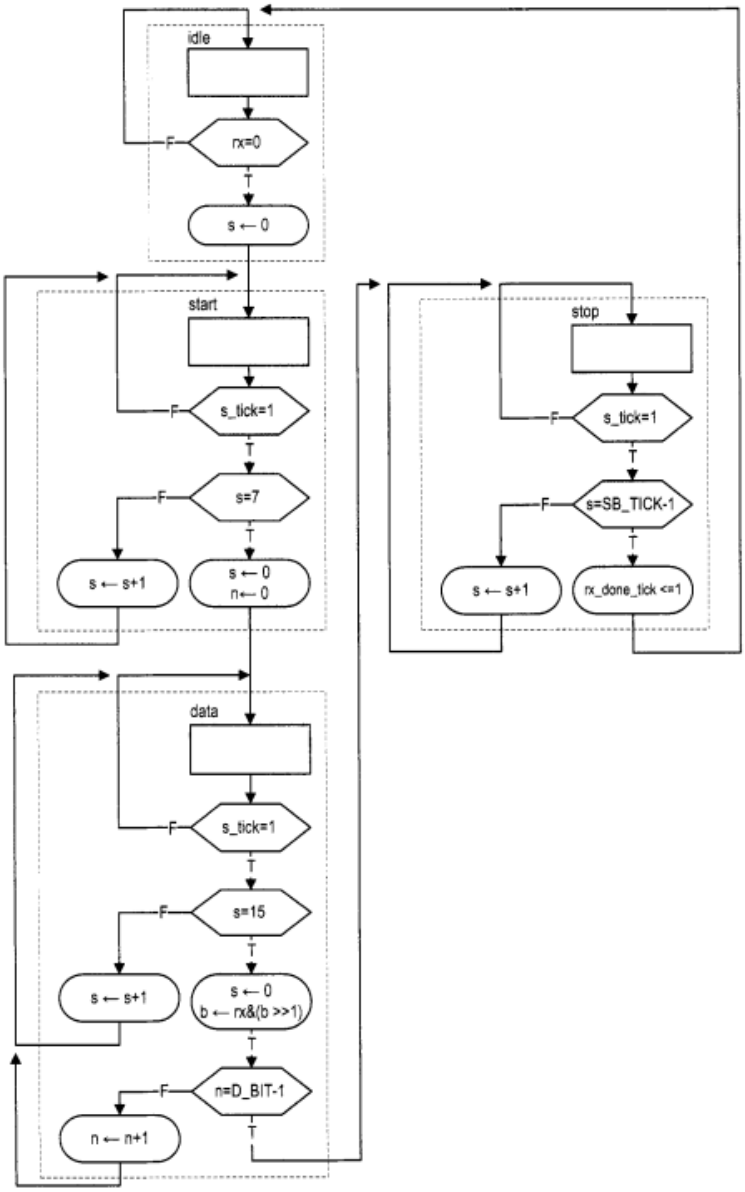


UART ASMD CHART

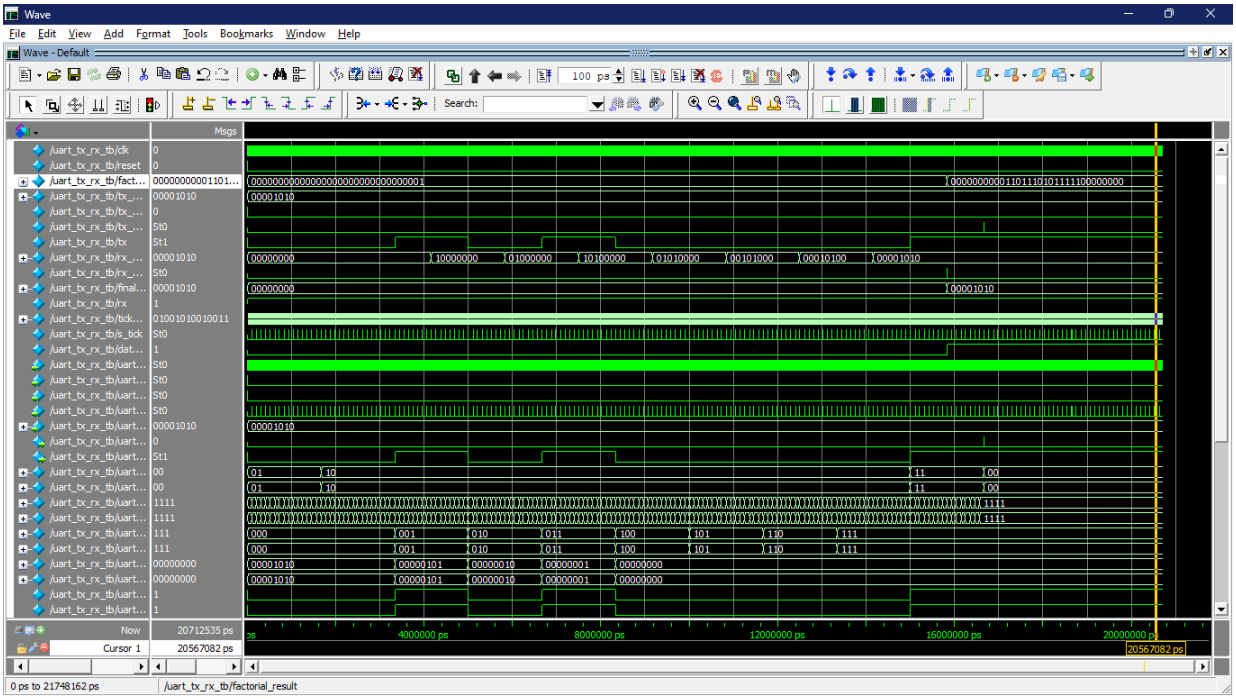
a) ASMD For Transmitter



b) ASMD Receiver



SIMULATED RESULT



The UART-Controlled Factorial Calculator demonstrates the practicality and flexibility of hardware description languages for real-time computations. This project successfully integrates hardware-based arithmetic computation with serial communication in a simulated environment, enabling interactive numerical processing. By calculating the factorial of a given number, such as “10”, which yields the result “3628800”, the system showcases the efficiency of modular design and resource optimization in digital system development. Additionally, the inclusion of a simulated output graph provides a visual representation of the data flow and computational results, enhancing the understanding and verification of system functionality.

REFERENCES

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3. J. Bhasker, *Verilog HDL Synthesis: A Practical Primer*.