

1. Description

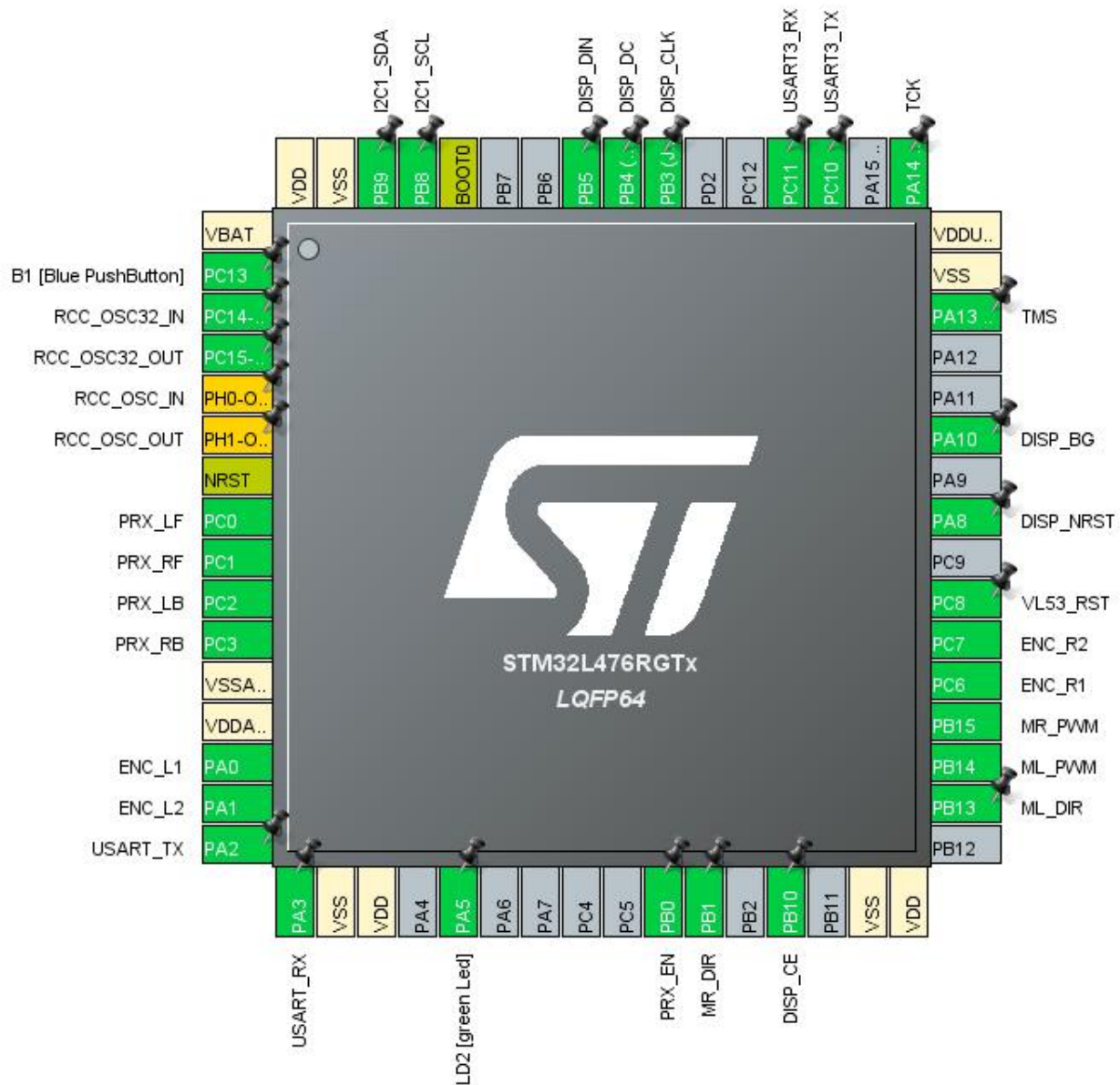
1.1. Project

| | |
|-----------------|-------------------|
| Project Name | I4-deskcovery |
| Board Name | NUCLEO-L476RG |
| Generated with: | STM32CubeMX 5.3.0 |
| Date | 09/18/2019 |

1.2. MCU

| | |
|----------------|---------------|
| MCU Series | STM32L4 |
| MCU Line | STM32L4x6 |
| MCU name | STM32L476RGTx |
| MCU Package | LQFP64 |
| MCU Pin number | 64 |

2. Pinout Configuration



3. Pins Configuration

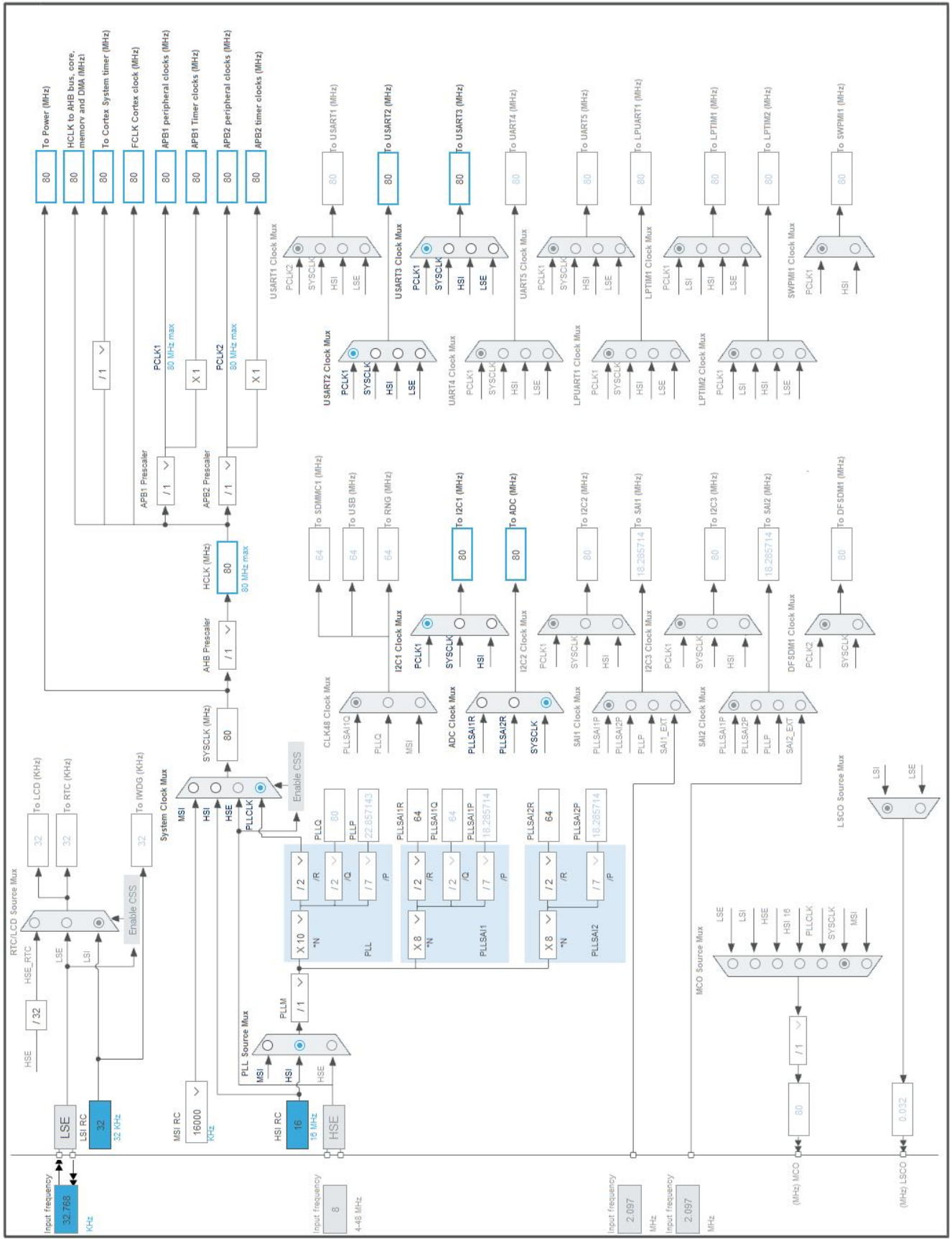
| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|----------------------|---------------------------------------|----------|--------------------------|----------------------|
| 1 | VBAT | Power | | |
| 2 | PC13 | I/O | GPIO_EXTI13 | B1 [Blue PushButton] |
| 3 | PC14-OSC32_IN (PC14) | I/O | RCC_OSC32_IN | |
| 4 | PC15-OSC32_OUT (PC15) | I/O | RCC_OSC32_OUT | |
| 5 | PH0-OSC_IN (PH0) * | I/O | RCC_OSC_IN | |
| 6 | PH1-OSC_OUT (PH1) * | I/O | RCC_OSC_OUT | |
| 7 | NRST | Reset | | |
| 8 | PC0 | I/O | ADC1_IN1 | PRX_LF |
| 9 | PC1 | I/O | ADC1_IN2 | PRX_RF |
| 10 | PC2 | I/O | ADC1_IN3 | PRX_LB |
| 11 | PC3 | I/O | ADC1_IN4 | PRX_RB |
| 12 | VSSA/VREF- | Power | | |
| 13 | VDDA/VREF+ | Power | | |
| 14 | PA0 | I/O | TIM5_CH1 | ENC_L1 |
| 15 | PA1 | I/O | TIM5_CH2 | ENC_L2 |
| 16 | PA2 | I/O | USART2_TX | USART_TX |
| 17 | PA3 | I/O | USART2_RX | USART_RX |
| 18 | VSS | Power | | |
| 19 | VDD | Power | | |
| 21 | PA5 ** | I/O | GPIO_Output | LD2 [green Led] |
| 26 | PB0 ** | I/O | GPIO_Output | PRX_EN |
| 27 | PB1 ** | I/O | GPIO_Output | MR_DIR |
| 29 | PB10 ** | I/O | GPIO_Output | DISP_CE |
| 31 | VSS | Power | | |
| 32 | VDD | Power | | |
| 34 | PB13 ** | I/O | GPIO_Output | ML_DIR |
| 35 | PB14 | I/O | TIM15_CH1 | ML_PWM |
| 36 | PB15 | I/O | TIM15_CH2 | MR_PWM |
| 37 | PC6 | I/O | TIM8_CH1 | ENC_R1 |
| 38 | PC7 | I/O | TIM8_CH2 | ENC_R2 |
| 39 | PC8 ** | I/O | GPIO_Output | VL53_RST |
| 41 | PA8 ** | I/O | GPIO_Output | DISP_NRST |
| 43 | PA10 | I/O | TIM1_CH3 | DISP_BG |
| 46 | PA13 (JTMS-SWDIO) | I/O | SYS_JTMS-SWDIO | TMS |
| 47 | VSS | Power | | |
| 48 | VDDUSB | Power | | |

| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|----------------------|---------------------------------------|----------|--------------------------|----------|
| 49 | PA14 (JTCK-SWCLK) | I/O | SYS_JTCK-SWCLK | TCK |
| 51 | PC10 | I/O | USART3_TX | |
| 52 | PC11 | I/O | USART3_RX | |
| 55 | PB3 (JTDO-TRACESWO) ** | I/O | GPIO_Output | DISP_CLK |
| 56 | PB4 (NJTRST) ** | I/O | GPIO_Output | DISP_DC |
| 57 | PB5 ** | I/O | GPIO_Output | DISP_DIN |
| 60 | BOOT0 | Boot | | |
| 61 | PB8 | I/O | I2C1_SCL | |
| 62 | PB9 | I/O | I2C1_SDA | |
| 63 | VSS | Power | | |
| 64 | VDD | Power | | |

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

| Name | Value |
|-----------------------------------|-------------------------|
| Project Name | I4-deskcovery |
| Project Folder | C:\work\I4-deskcovery |
| Toolchain / IDE | SW4STM32 |
| Firmware Package Name and Version | STM32Cube FW_L4 V1.14.0 |

5.2. Code Generation Settings

| Name | Value |
|---|---------------------------------------|
| STM32Cube MCU packages and embedded software | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files | No |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |

6. Power Consumption Calculator report

6.1. Microcontroller Selection

| | |
|-----------|---------------|
| Series | STM32L4 |
| Line | STM32L4x6 |
| MCU | STM32L476RGTx |
| Datasheet | 025976_Rev4 |

6.2. Parameter Selection

| | |
|-------------|-----|
| Temperature | 25 |
| Vdd | 3.0 |

7. IPs and Middleware Configuration

7.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

| | |
|-------------------------------|---|
| Clock Prescaler | Asynchronous clock mode divided by 256 * |
| Resolution | ADC 12-bit resolution |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Enabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| End Of Conversion Selection | End of sequence of conversion * |
| Overrun behaviour | Overrun data preserved |
| Low Power Auto Wait | Disabled |

ADC_Regular_ConversionMode:

Enable Regular Conversions **Disable ***

ADC_Injected_ConversionMode:

| | |
|----------------------------------|--|
| Enable Injected Conversions | Enable * |
| Enable Injected Oversampling | Disable |
| Number Of Conversions | 4 * |
| External Trigger Source | Injected Conversion launched by software |
| External Trigger Conversion Edge | None |
| Injected Conversion Mode | None |
| Injected Queue | Injected Queue Disable |
| <u>Rank</u> | 1 |
| Channel | Channel 1 |
| Sampling Time | 640.5 Cycles * |
| Offset Number | No offset |
| <u>Rank</u> | 2 * |
| Channel | Channel 2 * |
| Sampling Time | 640.5 Cycles * |

| | |
|------------------------------|-----------------------|
| Offset Number | No offset |
| <u>Rank</u> | 3 * |
| Channel | Channel 3 * |
| Sampling Time | 640.5 Cycles * |
| Offset Number | No offset |
| <u>Rank</u> | 4 * |
| Channel | Channel 4 * |
| Sampling Time | 640.5 Cycles * |
| Offset Number | No offset |
| Analog Watchdog 1: | |
| Enable Analog WatchDog1 Mode | false |
| Analog Watchdog 2: | |
| Enable Analog WatchDog2 Mode | false |
| Analog Watchdog 3: | |
| Enable Analog WatchDog3 Mode | false |

7.2. I2C1

I2C: I2C

7.2.1. Parameter Settings:

Timing configuration:

| | |
|-------------------------------|---------------|
| I2C Speed Mode | Standard Mode |
| I2C Speed Frequency (KHz) | 100 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | 0x10909CEC |

Slave Features:

| | |
|----------------------------------|----------|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

7.3. RCC

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

| | |
|-------------------|--------------------|
| VDD voltage (V) | 3.3 |
| Instruction Cache | Enabled |
| Prefetch Buffer | Enabled * |
| Data Cache | Enabled |
| Flash Latency(WS) | 4 WS (5 CPU cycle) |

RCC Parameters:

| | |
|--------------------------------|----------|
| HSI Calibration Value | 16 |
| MSI Calibration Value | 0 |
| MSI Auto Calibration | Disabled |
| HSE Startup Timeout Value (ms) | 100 |
| LSE Startup Timeout Value (ms) | 5000 |

Power Parameters:

| | |
|-------------------------------|---------------------------------|
| Power Regulator Voltage Scale | Power Regulator Voltage Scale 1 |
|-------------------------------|---------------------------------|

7.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.5. TIM1

Clock Source : Internal Clock

Channel3: PWM Generation CH3

7.5.1. Parameter Settings:

Counter Settings:

| | |
|---|--------------|
| Prescaler (PSC - 16 bits value) | 100 * |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value) | 98 * |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |
| auto-reload preload | Disable |

Trigger Output (TRGO) Parameters:

| | |
|-----------------------------|--|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
|-----------------------------|--|

| | |
|-------------------------------|------------------------------|
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |
| Trigger Event Selection TRGO2 | Reset (UG bit from TIMx_EGR) |

Break And Dead Time management - BRK Configuration:

| | |
|---------------------------|---------|
| BRK State | Disable |
| BRK Polarity | High |
| BRK Filter (4 bits value) | 0 |
| BRK Sources Configuration | |
| - Digital Input | Disable |
| - COMP1 | Disable |
| - COMP2 | Disable |
| - DFSDM | Disable |

Break And Dead Time management - BRK2 Configuration:

| | |
|----------------------------|---------|
| BRK2 State | Disable |
| BRK2 Polarity | High |
| BRK2 Filter (4 bits value) | 0 |
| BRK2 Sources Configuration | |
| - Digital Input | Disable |
| - COMP1 | Disable |
| - COMP2 | Disable |
| - DFSDM | Disable |

Break And Dead Time management - Output Configuration:

| | |
|--|---------|
| Automatic Output State | Disable |
| Off State Selection for Run Mode (OSSR) | Disable |
| Off State Selection for Idle Mode (OSSI) | Disable |
| Lock Configuration | Off |

Clear Input:

| | |
|--------------------|---------|
| Clear Input Source | Disable |
|--------------------|---------|

PWM Generation Channel 3:

| | |
|-----------------------|-------------|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 20 * |
| Fast Mode | Disable |
| CH Polarity | High |
| CH Idle State | Reset |

7.6. TIM5

Combined Channels: Encoder Mode

7.6.1. Parameter Settings:

Counter Settings:

| | |
|---|----------------|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value) | 65535 * |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

Trigger Output (TRGO) Parameters:

| | |
|------------------------------|--|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

Encoder:

| | |
|------------------------------------|------------------|
| Encoder Mode | Encoder Mode TI1 |
| ____ Parameters for Channel 1 ____ | |
| Polarity | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter | 0 |
| ____ Parameters for Channel 2 ____ | |
| Polarity | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter | 0 |

7.7. TIM8

Combined Channels: Encoder Mode

7.7.1. Parameter Settings:

Counter Settings:

| | |
|---|----------------|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value) | 65535 * |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |
| auto-reload preload | Disable |

Trigger Output (TRGO) Parameters:

| | |
|-------------------------------|--|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |
| Trigger Event Selection TRGO2 | Reset (UG bit from TIMx_EGR) |

Encoder:

| | |
|------------------------------------|------------------|
| Encoder Mode | Encoder Mode TI1 |
| ____ Parameters for Channel 1 ____ | |

| | |
|--------------------------|-------------|
| Polarity | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter | 0 |

____ Parameters for Channel 2 ____

| | |
|--------------------------|-------------|
| Polarity | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter | 0 |

7.8. TIM15

mode: Clock Source

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.8.1. Parameter Settings:

Counter Settings:

| | |
|---|--------------|
| Prescaler (PSC - 16 bits value) | 79 * |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value) | 999 * |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |
| auto-reload preload | Disable |

Trigger Output (TRGO) Parameters:

| | |
|-----------------------------|--|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

Break And Dead Time management - BRK Configuration:

| | |
|---------------------------|---------|
| BRK State | Disable |
| BRK Polarity | High |
| BRK Sources Configuration | |
| - Digital Input | Disable |
| - COMP1 | Disable |
| - COMP2 | Disable |
| - DFSDM | Disable |

Break And Dead Time management - Output Configuration:

| | |
|--|---------|
| Automatic Output State | Disable |
| Off State Selection for Run Mode (OSSR) | Disable |
| Off State Selection for Idle Mode (OSSI) | Disable |
| Lock Configuration | Off |

PWM Generation Channel 1:

| | |
|-----------------------|------------|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |
| CH Idle State | Reset |

PWM Generation Channel 2:

| | |
|-----------------------|------------|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |
| CH Idle State | Reset |

7.9. USART2

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

| | |
|-------------|---------------------------|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

Advanced Parameters:

| | |
|----------------|----------------------|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

Advanced Features:

| | |
|-------------------------------|---------|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

7.10. USART3

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

| | |
|-------------|---------------------------|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

Advanced Parameters:

| | |
|----------------|----------------------|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

Advanced Features:

| | |
|-------------------------------|---------|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

*** User modified value**

8. System Configuration

8.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|--------|-----------------------|----------------|--------------------------------|-----------------------------|-------------|------------|
| ADC1 | PC0 | ADC1_IN1 | Analog mode for ADC conversion | No pull-up and no pull-down | n/a | PRX_LF |
| | PC1 | ADC1_IN2 | Analog mode for ADC conversion | No pull-up and no pull-down | n/a | PRX_RF |
| | PC2 | ADC1_IN3 | Analog mode for ADC conversion | No pull-up and no pull-down | n/a | PRX_LB |
| | PC3 | ADC1_IN4 | Analog mode for ADC conversion | No pull-up and no pull-down | n/a | PRX_RB |
| I2C1 | PB8 | I2C1_SCL | Alternate Function Open Drain | Pull-up | Very High * | |
| | PB9 | I2C1_SDA | Alternate Function Open Drain | Pull-up | Very High * | |
| RCC | PC14-OSC32_IN (PC14) | RCC_OSC32_IN | n/a | n/a | n/a | |
| | PC15-OSC32_OUT (PC15) | RCC_OSC32_OUT | n/a | n/a | n/a | |
| SYS | PA13 (JTMS-SWDIO) | SYS_JTMS-SWDIO | n/a | n/a | n/a | TMS |
| | PA14 (JTCK-SWCLK) | SYS_JTCK-SWCLK | n/a | n/a | n/a | TCK |
| TIM1 | PA10 | TIM1_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Medium * | DISP_BG |
| TIM5 | PA0 | TIM5_CH1 | Alternate Function Push Pull | Pull-up * | Low | ENC_L1 |
| | PA1 | TIM5_CH2 | Alternate Function Push Pull | Pull-up * | Low | ENC_L2 |
| TIM8 | PC6 | TIM8_CH1 | Alternate Function Push Pull | Pull-up * | Low | ENC_R1 |
| | PC7 | TIM8_CH2 | Alternate Function Push Pull | Pull-up * | Low | ENC_R2 |
| TIM15 | PB14 | TIM15_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | ML_PWM |
| | PB15 | TIM15_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | MR_PWM |
| USART2 | PA2 | USART2_TX | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | USART_TX |
| | PA3 | USART2_RX | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | USART_RX |
| USART3 | PC10 | USART3_TX | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | | | | | | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|-----------------------|---------------------|-------------|--|-----------------------------|-----------------------|----------------------|
| | PC11 | USART3_RX | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| Single Mapped Signals | PH0-OSC_IN (PH0) | RCC_OSC_IN | n/a | n/a | n/a | |
| | PH1-OSC_OUT (PH1) | RCC_OSC_OUT | n/a | n/a | n/a | |
| GPIO | PC13 | GPIO_EXTI13 | External Interrupt Mode with Falling edge trigger detection | No pull-up and no pull-down | n/a | B1 [Blue PushButton] |
| | PA5 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Very High * | LD2 [green Led] |
| | PB0 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Very High * | PRX_EN |
| | PB1 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Very High * | MR_DIR |
| | PB10 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Very High * | DISP_CE |
| | PB13 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Very High * | ML_DIR |
| | PC8 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Very High * | VL53_RST |
| | PA8 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Very High * | DISP_NRST |
| | PB3 (JTDO-TRACESWO) | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Very High * | DISP_CLK |
| | PB4 (NJTRST) | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Very High * | DISP_DC |
| | PB5 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Very High * | DISP_DIN |

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|--|--------|----------------------|-------------|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Prefetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 0 | 0 |
| ADC1 and ADC2 interrupts | true | 0 | 0 |
| PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| TIM1 break interrupt and TIM15 global interrupt | unused | | |
| TIM1 update interrupt and TIM16 global interrupt | unused | | |
| TIM1 trigger and commutation interrupts and TIM17 global interrupt | unused | | |
| TIM1 capture compare interrupt | unused | | |
| I2C1 event interrupt | unused | | |
| I2C1 error interrupt | unused | | |
| USART2 global interrupt | unused | | |
| USART3 global interrupt | unused | | |
| EXTI line[15:10] interrupts | unused | | |
| TIM8 break interrupt | unused | | |
| TIM8 update interrupt | unused | | |
| TIM8 trigger and commutation interrupts | unused | | |
| TIM8 capture compare interrupt | unused | | |
| TIM5 global interrupt | unused | | |
| FPU global interrupt | unused | | |

* User modified value

9. Software Pack Report