











**顶层文件：**

LIBRARY IEEE;

USE IEEE.STD\_LOGIC\_1164.ALL;

USE work.h\_adderp.all;

USE work.f\_adderp.all;

ENTITY adderVHDL IS

PORT(a0, b0, c0, a1, b1, a2, b2, a3, b3: IN STD\_LOGIC;

s0, s1, s2, s3, cout: OUT STD\_LOGIC);

END adderVHDL;

ARCHITECTURE example OF adderVHDL IS

SIGNAL ss1, ss2, ss3, ss4, cc1, cc2, cc3, cc4: STD\_LOGIC;

BEGIN

f1: f\_adder PORT MAP(a0, b0, c0, ss1, cc1);

f2: f\_adder PORT MAP(a1, b1, cc1, ss2, cc2);

f3: f\_adder PORT MAP(a2, b2, cc2, ss3, cc3);

f4: f\_adder PORT MAP(a3, b3, cc3, ss4, cc4);

s0 <= ss1;

s1 <= ss2;

s2 <= ss3;

s3 <= ss4;

cout <= cc4;

END example;

**h\_adder文件：**

LIBRARY IEEE;

USE IEEE.STD\_LOGIC\_1164.ALL;

ENTITY h\_adder IS

PORT(a, b: IN STD\_LOGIC;

s, c: OUT STD\_LOGIC);

END h\_adder;

ARCHITECTURE example OF h\_adder IS

BEGIN

s <= a XOR b;

c <= a AND b;

END example;

**h\_adderp包文件：**

LIBRARY IEEE;

USE IEEE.STD\_LOGIC\_1164.ALL;

PACKAGE h\_adderp IS

COMPONENT h\_adder IS

PORT(a, b: IN STD\_LOGIC;

s, c: OUT STD\_LOGIC);

END COMPONENT h\_adder;

END h\_adderp;

**f\_adder文件：**

LIBRARY IEEE;

USE IEEE.STD\_LOGIC\_1164.ALL;

USE work.h\_adderp.all;

ENTITY f\_adder IS

PORT(ai, bi, ci: IN STD\_LOGIC;

so, co: OUT STD\_LOGIC);

END f\_adder;

ARCHITECTURE example OF f\_adder IS

SIGNAL SZ1, CZ1, SZ2, CZ2: STD\_LOGIC;

BEGIN

h1: h\_adder PORT MAP(ai, bi, sz1, cz1);

h2: h\_adder PORT MAP(sz1, ci, sz2, cz2);

so <= sz2;

co <= cz1 OR cz2;

END example;

**f\_adderp包文件：**

LIBRARY IEEE;

USE IEEE.STD\_LOGIC\_1164.ALL;

USE work.h\_adderp.all;

PACKAGE f\_adderp IS

COMPONENT f\_adder IS

PORT(ai, bi, ci: IN STD\_LOGIC;

so, co: OUT STD\_LOGIC);

END COMPONENT f\_adder;

END f\_adderp;

