**16计数器**

library ieee;

use ieee.std\_logic\_1164.all;

entity counter is

port(clk, clr:in std\_logic;

q:buffer std\_logic\_vector(3 downto 0);

cout:out std\_logic);

end counter;

architecture one of counter is

begin

process(clk, clr)

begin

if clr = '0' then

q <= "0000";

elsif clk'event and clk = '1' then

if q(0) = '0' then q(0) <= '1';

else

q(0)<='0';

if q(1) = '0' then q(1)<='1';

else q(1)<='0';

if q(2)='0' then q(2)<='1';

else q(2)<='0';

if q(3)='0' then q(3)<='1';

else q(3)<='0';

end if;

end if;

end if;

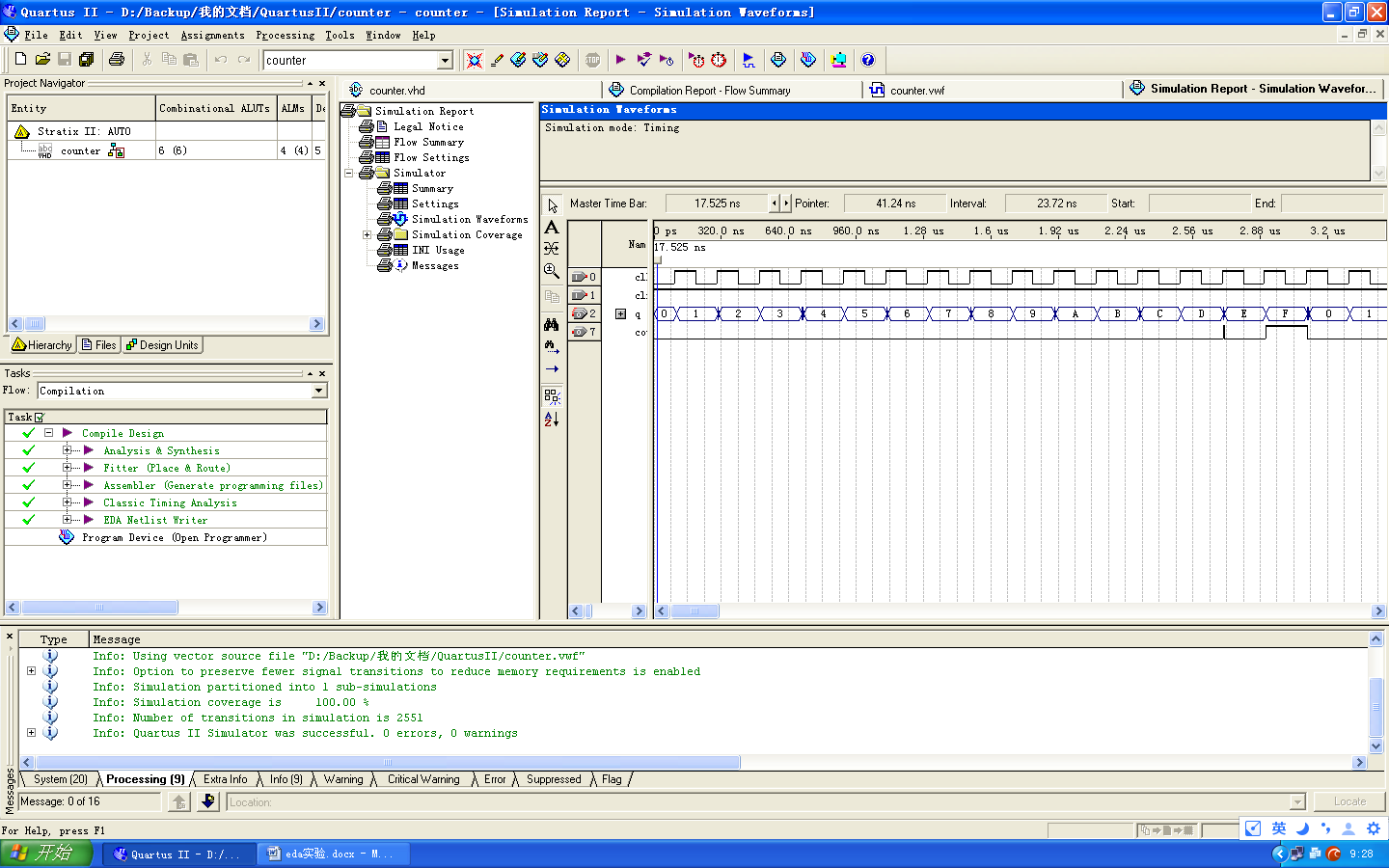
end if;

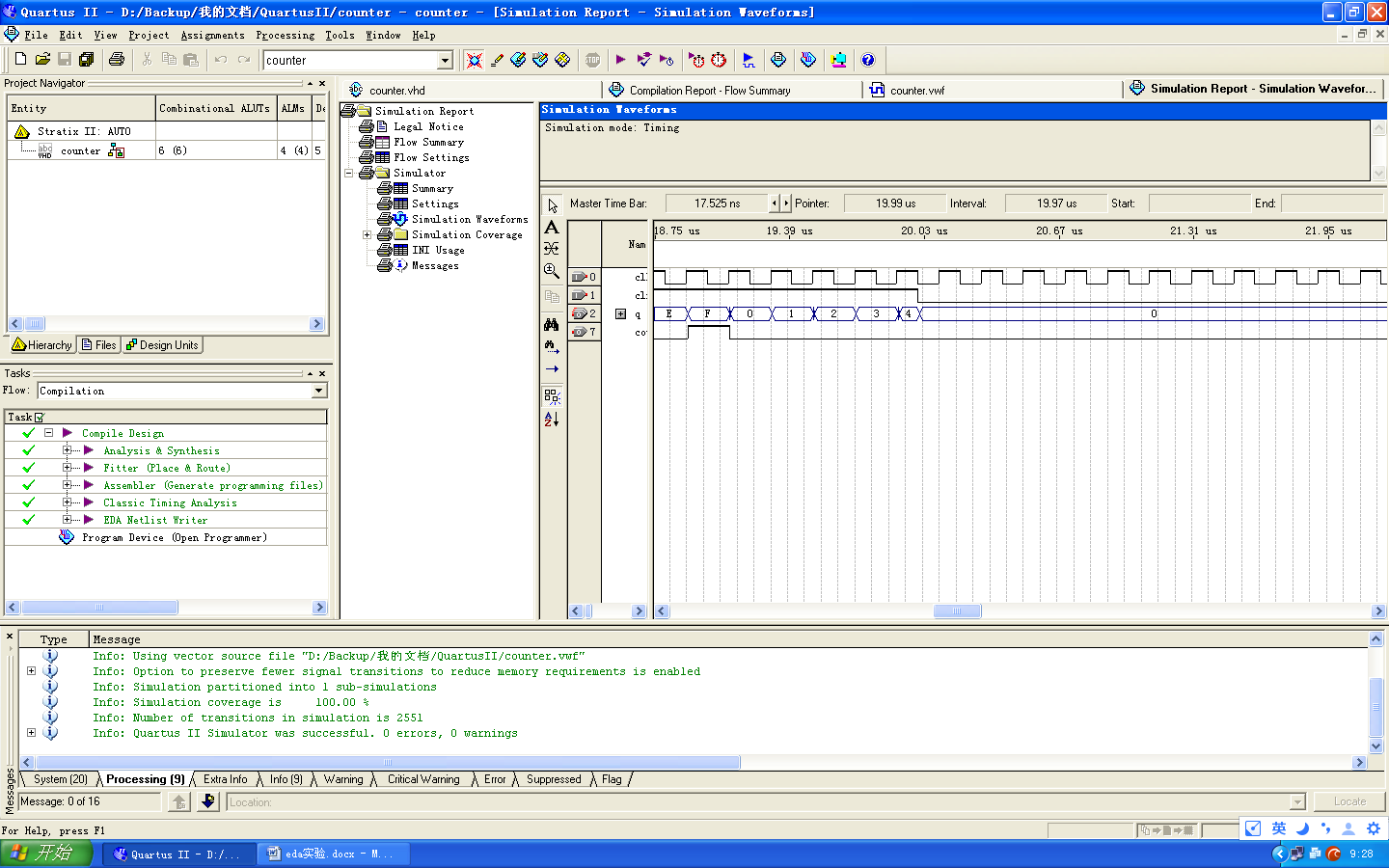
end if;

cout <= q(0) and q(1) and q(2) and q(3);

end process;

end one;





**10计数器**

library ieee;

use ieee.std\_logic\_1164.all;

entity counter is

port(clk, clr:in std\_logic;

q:buffer std\_logic\_vector(3 downto 0);

cout:out std\_logic);

end counter;

architecture one of counter is

begin

process(clk, clr)

begin

if clr = '0' then

q <= "0000";

elsif clk'event and clk = '1' then

if q = "1001" then q<="0000";

else

if q(0) = '0' then q(0) <= '1';

else

q(0)<='0';

if q(1) = '0' then q(1)<='1';

else q(1)<='0';

if q(2)='0' then q(2)<='1';

else q(2)<='0';

if q(3)='0' then q(3)<='1';

else q(3)<='0';

end if;

end if;

end if;

end if;

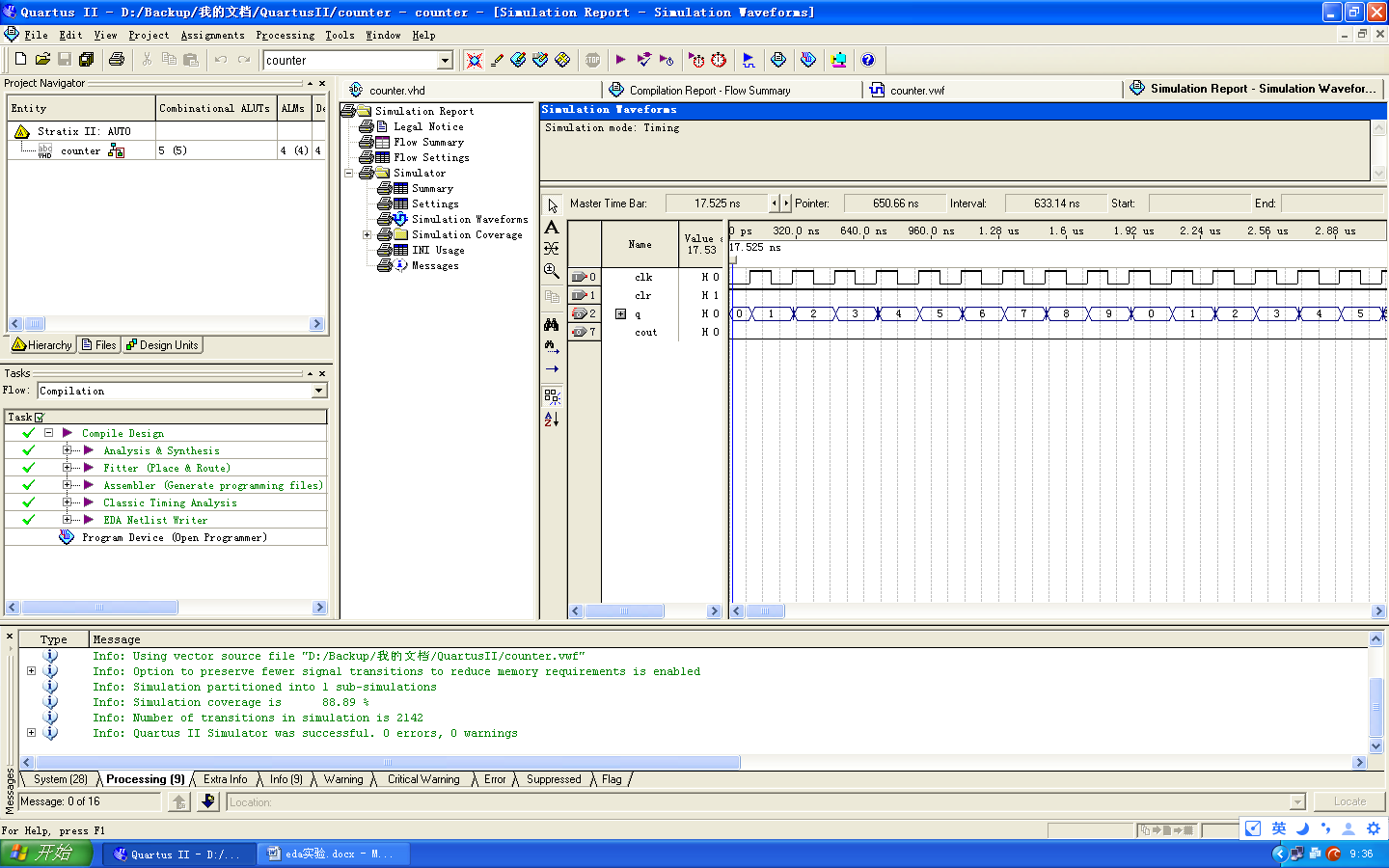
end if;

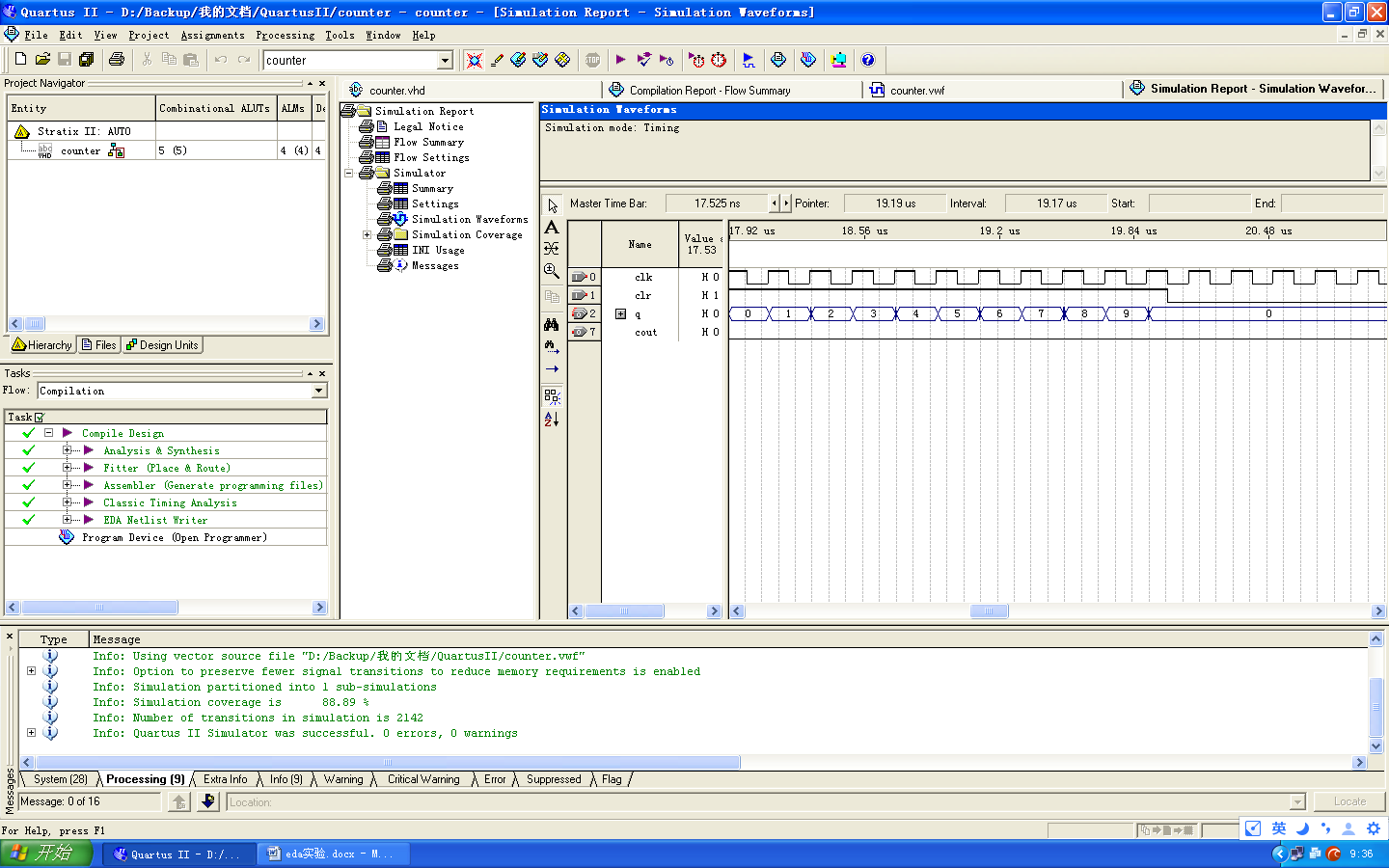
end if;

cout <= q(0) and q(1) and q(2) and q(3);

end process;

end one;





**47显示译码器**

library ieee;

use ieee.std\_logic\_1164.all;

entity decoder47 is

port(a:in std\_logic\_vector(3 downto 0);

q:out std\_logic\_vector(6 downto 0));

end decoder47;

architecture one of decoder47 is

begin

with a select

q <= "1111110" when "0000",

"0110000" when "0001",

"1101101" when "0010",

"1111001" when "0011",

"0110011" when "0100",

"1011011" when "0101",

"1011111" when "0110",

"1110000" when "0111",

"1111111" when "1000",

"1111011" when "1001",

"1000000" when others;

end one;

