**1092 DSD Machine Test**

Student ID :\_\_\_\_\_B07901068\_\_\_\_\_

Name:\_\_\_\_ 黃敬騰\_\_\_\_\_\_\_\_

**Final Outcome: (Write √ if you pass )**

1. RTL Simulation:

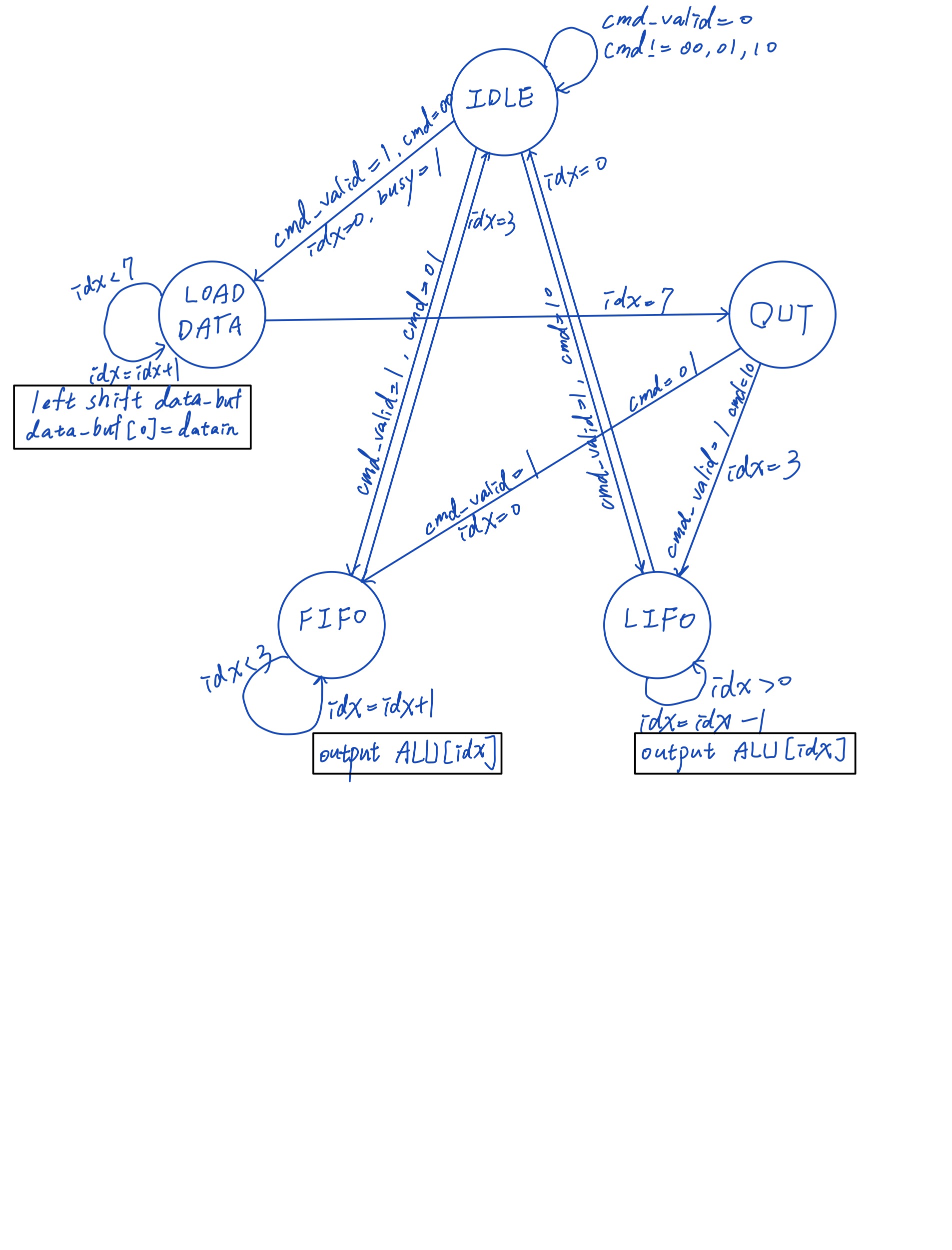
**√** ALU results are correct! (30%)

**√** DFC results of “ALU+FIFO instruction” are correct! (15%)

**√** DFC results of “ALU+LIFO instruction” are correct! (15%)

**√** Use your own ALU submodule in DFC design and results are all correct! (5%)

B. Illustrate Finite State Machine of your DFC Design (20%)



1. Gate-Level Simulation:

**√** DFC results of “ALU+FIFO instruction” are correct and no timing violation! (5%)

**√** DFC results of “ALU+LIFO instruction” are correct and no timing violation! (5%)

**√** Use your own ALU sub-module in DFC design and results are all correct and no timing violation! (5%)