Jing-Teng (Jeter) Hwang

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RESEARCH INTERESTS

Digital Circuit Design, Hardware Accelerators

EDUCATION

National Taiwan University (NTU) **Taipei, Taiwan**
B.S. in Electrical Engineering *Sept 2018 - Jun 2022*

- Cumulative GPA: 3.97 / 4.30; **Last-60 GPA: 4.13 / 4.30**
- Relevant Coursework: Integrated Circuit Design, Digital System Design, Electrical Engineering Lab (Digital Circuit), Integrated Circuits Design Lab, Computer Architecture (RISCV)

RESEARCH EXPERIENCE

NTU MicroSystem Research Lab, NTU **Taipei, Taiwan**
Undergraduate Research Assistant (with Prof. Tzi-Dar Chiueh) *Feb 2021 - Aug 2022*

Research topic: *Mixed-precision Quantized Neural Architecture Search (QNAS)* **[Paper]**

- Combined LSQ quantization scheme and Once-For-All network to search for mixed-precision networks.
- Best subnet achieved 72.31% accuracy on Imagenet with merely 6.17(G) bit operations.

Lab for Data Processing Systems, NTU **Taipei, Taiwan**
Undergraduate Research Assistant (with Prof. Yi-Chang Lu) *Sept 2020 - Present*

Research topic: *Accelerator for Multiple Sequence Alignment (MSA)*

- Designed and implemented the first MSA pipeline that embedded protein sequences with LSTM.
- The proposed algorithm outperformed most existing MSA pipelines in alignment accuracy.

PUBLICATION

- **Jing-Teng Hwang**, Yi-Chang Lu, "LE TRECO: an Lstm-based Embedding method for the TREe COnstruction step in Multiple Sequence Alignment," (Submitted to Bioinformatics) **[Paper]**

SELECTED TERM PROJECTS

FPGA-based Gobang AI [Demo] *Sept 2020*

- Designed an intelligent Gobang chess AI that can beat average players with the Min-Max Search algorithm.

ASIC for Sparse Matrix Vector Multiplication [PDF] *Apr 2021*

- Designed and taped out an ASIC for sparse matrix vector multiplication that achieved 70x speedup than software.

RISCV CPU [Slides] *May 2021*

- Implemented a RISCV CPU supporting branch prediction, cache prefetch and instruction compression.

Topic Transfer Chatbot [PDF] *Jun 2022*

- Designed a task-specific chatbot guiding conversation topics from one domain into another domain.

WORKING EXPERIENCE

Intel Microelectronics Asia LLC., Taiwan Branch **Taipei, Taiwan**
Platform Validation Engineer *Aug 2021 - Jul 2022*

- Maintained an internal project testing LTSSM state machine of PCIe connections.
- Led a web-based side project which aims to parse and graphicalize confidential testing logs.

KEY SKILLS

Programming Language Python, C++, Verilog, Javascript, Latex
Natural Language Taiwanese (native), Mandarin (native), English (fluent)