EE 435 Homework 4 Spring 2024

Jonathan Hess
GitHub Page

Problem 1 and 2

The model parameters μ, C OX, VTH and λ are widely used in analytical formulations of the performance of analog circuits. These parameters are used to characterize how MOS transistors operate in the square-law model of the transistor. When operating in the saturation region, the square-law model for the drain current of transistors can be expressed as $I_D =$

Though this square-law formulation is a simplification, it gives reasonable results that can be used for much of the design process. Better and more comprehensive models, such as the BSIM models, are then used in computer simulations to more accurately predict performance and for refining the design to meet target specifications. The BSIM models, however, are not analytically tractable and thus unsuitable for analytical formulations. Though intermediate models that are more accurate than the square-law models and less comprehensive than the BSIM models exist, there is little evidence of analytical tractability for models with complexity beyond that of the square-law model. Many analog circuits are quite sensitive to the parameter λ in the square-law model. Unfortunately, the parameter λ is quite sensitive to device dimensions and operating point. As such, a table or plot of λ parameters is useful when using the square- law model for predicting the performance of many analog circuits based upon the square- law model. Generate plots of λ for both n-channel and p-channel transistors in the 0.18μm CMOS for different lengths and for three different values of W and for three different values of VDS as shown below. Comment on how λ varies with device dimensions and operating points. When determining λ, assume that the devices are modeled by the BSIM model which is embedded in the PDK file used in SPECTRE. Extract λ at a given operating point by taking two measurements (simulation results) of the drain current at values of VDS slightly above and slightly below the target VDS value on a constant VGS locus as shown in the plot below. This is likely how you extracted the parameter λ in EE 330. The length should vary between LMIN and 20LMIN and the VDS values should be from slightly above VEB to 2.5V.

Problem 3

Consider the 5T op amp configured used as a transconductance amplifier in the circuit shown below. Assume the op amp is designed in a 0.18μm ON CMOS process with VDD =1.2V, VSS=-1.2V, L=2μm and V EB=100mV for all transistors, and the power in the op amp is 1mW. Assume λ=.01V

a)

What is W1?

To find all W we can look at constraints.
$W1 = W2$
$W3 = W4$
$P = 2.4V(Id) = 1mW$
$V_{EB} = 100mV = VGS - Vt$
$V_{SD3} + V_{DS1} + V_{DS5} = 2.4$
The max tail current is 416.6μA which means that current through M1 is 208.3μA. Using the current equation and K from the datasheet (K = 171.8μ)we get:
$I_d = \frac{W}{L}(K)(VGS - Vt)^2(1 + V_{DS}\lambda) = 208.3\mu A = (.01) * 171.8\mu * \frac{W}{L}(1 + V_{DS}(.01))$
$I_d = \frac{W}{L}(K)(VGS - Vt)^2 = 208.3\mu A = (.01) * 171.8\mu * \frac{W}{L}$

We get that:
$w = 121.265 * L = 242.53\mu m$

b)

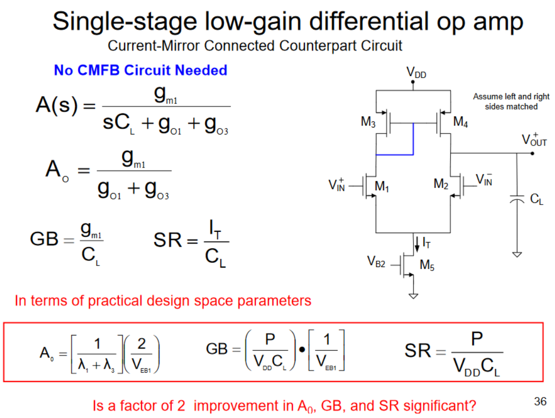
What is the quiescent voltage at the source of M1 ?

The voltage drop across M3 is id*Gm3 The voltage on source

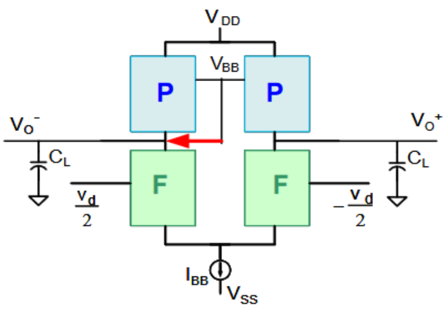
c)

Obtain an expression for the small signal voltage gain of the OTA circuit in terms of the small-signal parameters g m1, R1 , and C1.

These expressions are available in the lecture 5 slides

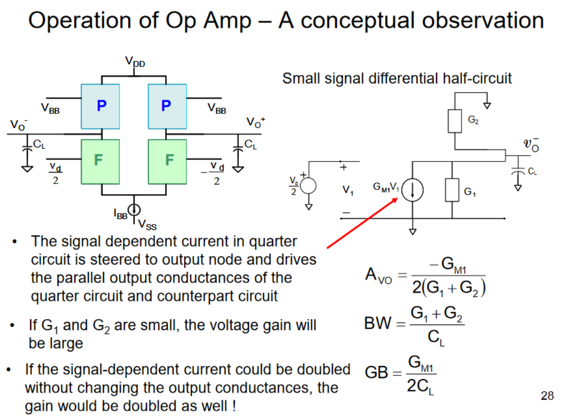


These were found by splitting the circuit into quarters and mirroring the left and right sides.



By doing this we can analyze the F and P circuits individually.

For the P circuit we have a single transistor connected to itself. Because of the current mirror the second P (on the right side) is also virtually connected to itself. This means that it acts as a resistor with no external biasing.



d)

Numerically determine and plot the small signal frequency dependent voltage gain if R1 =50K and C1 =40pF

e)

Determine the 3dB bandwidth

f)

How does the 3dB bandwidth change if the power in increased by 20% by changing VB2?

http://class.ece.iastate.edu/ee435/miscHandouts/TSMC
http://class.ece.iastate.edu/ee330/lectures/EE