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Design and Analysis of Two-Stage CMOS Operational Amplifier for Fluorescence Signal Processing

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***Abstract*—Transimpedance amplifier is an important part of the signal processing circuit in the fluorescent optical fiber temperature sensor to amplify the current signal and convert it into a voltage one. The two-stage CMOS operational amplifier, which can be designed to achieve high gain, high CMRR and low input offset voltage, can be used in transimpedance amplifier circuits. Based on 0.18μm CMOS process, a two-stage differential operational amplifier is designed in this paper. The simulation results show that the gain of the reaches 85.5dB, the CMRR and the negative PSRR are both around 90dB. The Miller compensation circuit in the circuit increases the gain bandwidth of the two-stage CMOS operational amplifier and makes the phase margin reach 80°. This paper introduces the circuit principle of CMOS two-stage operational amplifier in detail, and according to the simulation result, this operational amplifier meets the index requirement.**

Keywords-fluorescence detection; two-stage operational amplifier; Miller compensation; fully differential structure;

I. INTRODUCTION

In the fields of industrial production, chemical reaction, and medical treatment, real-time online temperature monitoring is required. Fluorescent optical fiber temperature sensing is one of the commonly used technologies for real-time temperature monitoring [1]. In the fluorescent optical fiber temperature sensor, the photodiode can detect the weak fluorescent signal and convert the fluorescent signal into a current signal. In order to further amplify the fluorescent signal, a transimpedance amplifier is needed. The transimpedance amplifier uses the "virtual ground" of the inverting input terminal of the operational amplifier and the extremely high input impedance characteristics, which greatly inhibits the shunting effect of the photodiode. The photocurrent completely flows through the feedback resistor connected across the inverting input terminal and the input terminal of the operational amplifier, and a corresponding voltage signal is generated at the output terminal of the operational amplifier [2]. Because the two-stage CMOS operational amplifier has higher gain and high CMRR and low input offset voltage, it can be used in transimpedance circuits.

As a widely used circuit module, operational amplifiers generally require the main characteristics of high input impedance, high magnification, and low output impedance [3]. Because it can realize various operations on analog signals, it is often used in many applications, and its performance indicators also directly affect the overall performance of electronic devices [4]. In this paper, two-stage operational amplifier can achieve higher gain and output swing at the same time. The principle is to process the gain and swing in two-stages, that is, use the first-stage amplifier to obtain high gain at the expense of swing; the second-stage obtains large output swing amplitude, to compensate the swing amplitude sacrificed by the first stage, in addition to further increase the operational amplifier gain, thereby overcoming the contradiction between gain and swing amplitude.

II. CIRCUIT DESIGN AND THEORY

The two-stage operational amplifier system originally designed is shown in Fig.1. It contains five modules, namely differential input, high gain stage, output buffer stage, bias circuit and compensation circuit.

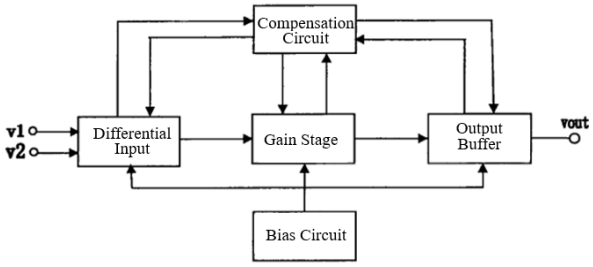

Figure 1. Block diagram of operational amplifier

In practice, most of the various performance indicators of the operational amplifier will restrain each other, causing the design to become a multi-dimensional optimization problem. Although it is impossible to design a very ideal operational amplifier, we can design it with one or two outstanding parameters, although other parameters may require sacrifices or compromises. The following will further analyze the principle and design process of the secondary operational amplifier.

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A. Specific Circuit Sqtructure

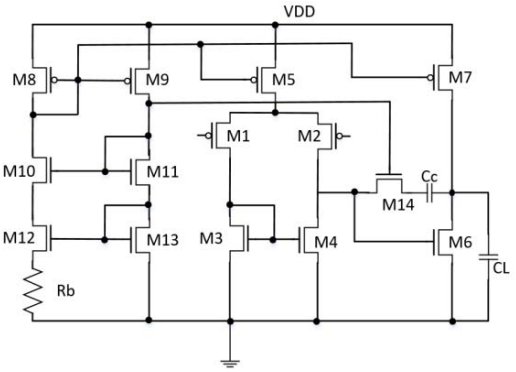

Figure 2. The Two-Stage CMOS operational amplifier circuit

The performance requirements of the two-stage operational amplifier in this article are shown in Table I, and the circuit will be designed based on this table below.

Choose the circuit structure shown in Fig.2 based on the performance indicator of the designed operational amplifier. The operational amplifier is composed of two amplifier stages. The first stage is a differential amplifier with input pairs M1 and M2, and current mirrors M3 and M4 as loads. The tail current source M5 provides operating current; the second stage is a common source amplifier. M6 is used as input tube, M7 is used as load tube; the current source composed of M8-M13 and a resistor Rb provides bias voltage for the two-stage amplifier, and also provides bias voltage for M14 for frequency compensation [5]; M14 and capacitor Cc form frequency compensation, they is connected between the input and output of the common source stage.

B. Theoretical Analysis

The operational amplifier design process is actually the process of converting the performance index requirements into the specific topology and device parameters of the operational amplifier. Of course, this process needs to be combined with the process model that finally realizes the operational amplifier layout. Therefore, the design of the operational amplifier can be divided into the following two steps:

- Select the operational amplifier structure according to the main performance indicators, and draw the circuit diagrams of all the tube connections.
- On the basis of clarifying the relevant process parameters, manually calculate the width-to-length ratio of each tube in the operational amplifier, and then select the appropriate software for simulation results.

The following is the process of theoretical analysis of the secondary operational amplifier.

a) Gain Margin

The total gain of the second stage operational amplifier:

$$A_V = A_{V1}A_{V2} = \frac{g_{m1}g_{m6}}{(g_{o2}+g_{o4})(g_{o6}+g_{o7})} \tag{1}$$

b) Frequency Characteristics

Common source transfer function:

$$H(s) = \frac{1 - g_{m6}\left(R_{on14} + \frac{1}{sC_C}\right)}{g_{m6}R_{o1} + 1 + \left(\frac{1}{R_{o2}} + sC_L\right)\left(R_{o1} + R_{on14} + \frac{1}{sC_C}\right)} \tag{2}$$

In equation (2), Ron14 is the resistance of the M14 tube, Ro1 is the output resistance of the first stage, Ro2 is the output resistance of the second stage.

The zero pole is obtained through the equation (2), is

$$\omega_Z = \frac{1}{\left(\frac{1}{g_{m6}} - R_{on14}\right)C_C} \tag{3}$$

Main pole and the second pole are respectively

$$\omega_{p1} = \frac{1}{R_{o1}(1 + g_{m6}R_{o2})C_C} \tag{4}$$

$$\omega_{p2} = \frac{g_{m6}}{C_L} \tag{5}$$

Unity-gain frequency can be obtained by equations (1) and (4), available as follow:

$$GBW = A_V\omega_{p1} \approx \frac{g_{m1}}{C_C} \tag{6}$$

c) Bias Circuit

According to the current and voltage formula, taking $\left(\frac{I}{W}\right)_{12} = 4\left(\frac{I}{W}\right)_{13}$, we can get

$$R_b = \frac{1}{g_{m13}} \tag{7}$$

d) CMRR

$$CMRR = \frac{2g_{m1}g_{m3}}{(g_{o2}+g_{o4})g_{o5}} \tag{8}$$

e) Negative Power Supply Rejection Ratio(NPSRR)

$$NPSRR = \frac{2g_{m1}g_{m6}}{(g_{o2}+g_{o4})g_{o6}} \tag{9}$$

III. Simulation Results and Analysis

After completing the basic design, the simulation verification is carried out through the Cadence. The following are the simulation results and analysis of the second stage operational amplifier.

a) Frequency Response Rnalysis

As shown in Fig.3, the unity gain bandwidth of the operational amplifier can be obtained as 45.7MHz, the phase margin is 80.4°, and the open-loop gain at low frequency is 85.5dB.

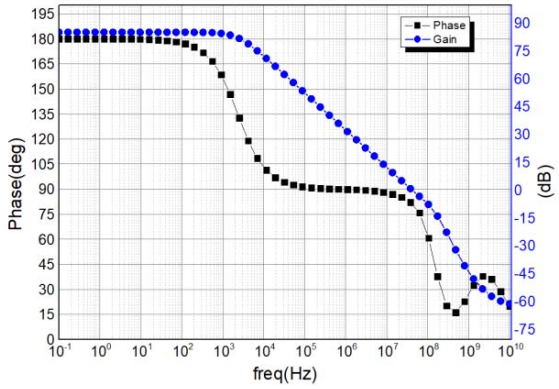

Figure 3. The AC characteristic curve

b) Input Offset Voltage

Input the reverse terminal of the operational amplifier with a DC level of 2.5V, and scan the DC voltage difference between the non-inverting terminal and the reverse terminal [6]. As shown in Fig.4, when the differential mode voltage at the non-inverting input terminal and the inverting input terminal is about 79.8uV, the output DC level is closest to 2.5V, that is, the resulting input offset voltage is 79.8uV.

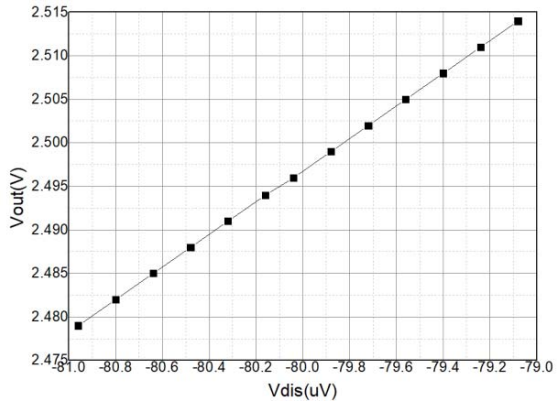

Figure 4. The input Offset voltage simulation waveform

c) CMRR

The quotient of the differential mode magnification and the common mode magnification is CMRR, which is generally expressed in decibels, namely CMRR= 20log(Av/Acm) [7]. The simulation result is shown in Fig.5. The curve is 1/CMRR, so the low-frequency common-mode rejection ratio of the operational amplifier can be obtained as 92dB.

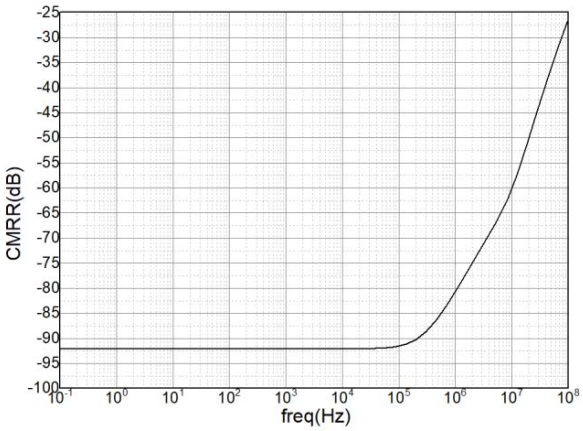

Figure 5. Measured the common mode gain

d) NPSRR

NPSRR is a measure of the ability of a circuit to suppress power supply noise. That is, the quotient of the differential mode magnification and the negative power magnification is NPSRR, which is generally expressed in decibels, namely NPSRR=20log(Av/Agnd). The simulation results are shown in Fig.6. The curve is 1/NPSRR, so the NPSRR of the operational amplifier can be obtained as 89dB.

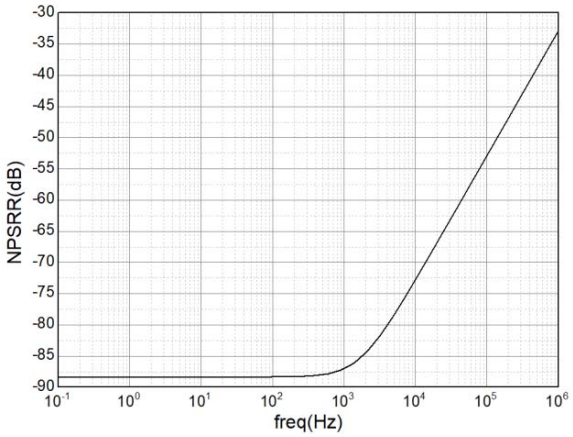

Figure 6. Measured the negative power rejection ratio

The comparison between design requirements and simulation results is shown in Table Ⅰ.

TABLE I. SIMULATION RESULTS

Performance parameter	*Performance requirements*	*Simulation results*
Power consumption	⩽2mW	2mW
Gain margin	⩾80dB	85.5dB
Phase margin	⩾60°	80.4°
CMRR	⩾60dB	92dB
Offset voltage	⩽0.5mV	79.8uV
Unity-gain frequency	⩾40MHz	45.7MHz
NPSRR	⩾80dB	89dB

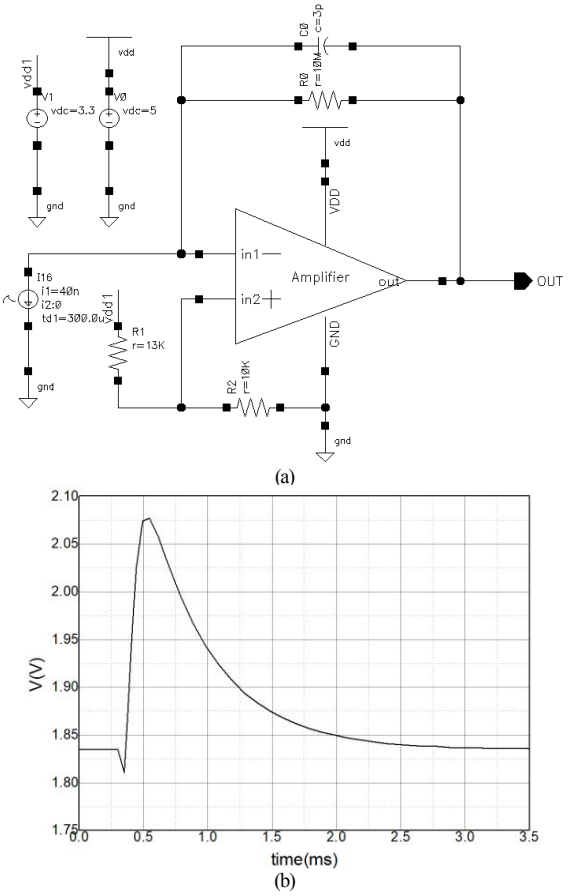

Figure 7. Transimpedance amplifier using two-stage CMOS operational amplifier. (a)is the circuit diagram, (b) is the output waveform diagram

The transimpedance circuit using a two-level CMOS operational amplifier is shown in Fig. 7(a). Set up an imitating exponential decay current source in the circuit, its maximum value is 40nA, the simulation result obtained is shown as in Fig. 7(b). It can be seen from the simulation curve that the output voltage amplitude of the transimpedance circuit can reach 250mV, which meets the design requirements.

IV. CONCLUSION

A two-stage CMOS operational amplifier is designed. The amplifier has large gain and good frequency response due to pole-zero cancellation to eliminate the positive zero of Moller amplifier, and excellent common-mode behavior. The simulation results show that the two-stage CMOS operational amplifier meets the design requirements. The open-loop gain is 85.5dB, the CMRR and the NPSRR are both around 90dB, and the input offset voltage is 79.8uV. The two-stage CMOS operational amplifier is used in the transimpedance circuit, and the simulation results obtained meet the requirements.

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