EE 435 Lab 3 Spring 2024

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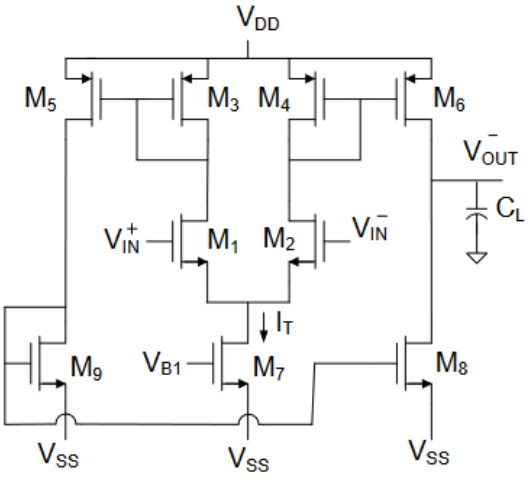
GitHub Page

Current-Mirror Operational Amplifier Design

The current mirror op amp is shown below. This can be used as a standard operational amplifier in a feedback configuration though when it was introduced the primary focus was on using it in open-loop applications as an Operational Transconductance Amplifier (OTA).

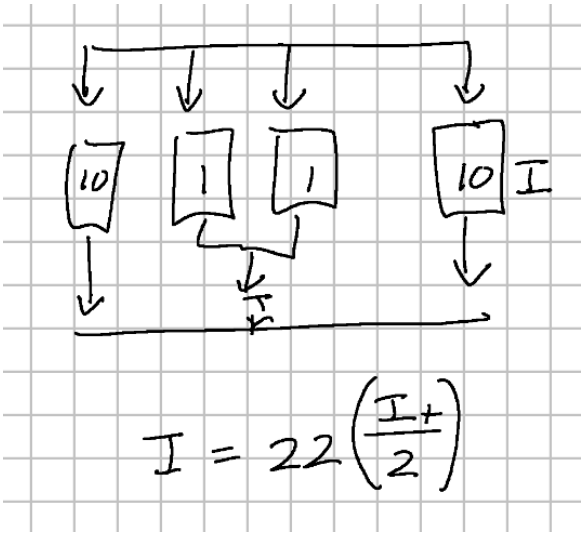


Part 1

Design this op amp in a 0.18μm process with supply voltages of VDD=1.5V and VSS =-1.5V. In this design, the lengths of all devices should be 5xL min , the mirror gains M 35 and M46 should be 10, the mirror gain M98 should be 1, the power dissipation should be 1mW, and V EB should be 100mV for all devices.

The first step taken wss to figure how the constraints affected the design.

Using the power constraint ($P = 1mW$) we can constrain the current because the $P = IV$. Voltage is $VDD - VSS = 3V$, this means current equals 333.33μA. Because of the current mirrors and symmetry we can find the tail current. The paths are laid out like so.



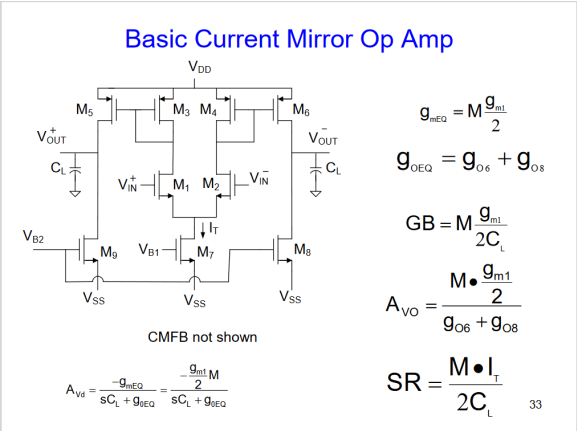
The tail current is $\frac{(333.33\mu A)}{11} = 30.30\mu A$ and because the bias current has been constrained as well we can solve for the W/L ratio.

Using the DC operating point we can find the VTH and other process parameters.
$M3 = M4 = (1/10) * M5 = (1/10) * M6$
$M1 = M2$
$M7 =$ fixed due to power
$M9 = M8$

Part 2

Analytically determine the differential voltage gain, the BW, the GB, and the SR of this amplifier. Assume CL =20pF

The gain, bandwidth, gain bandwidth, and slew rate can be determined by the following equations given in the lecture slides.



Where M is the value of the current mirror (10) C_L is the load capacitor, and gm1 is the gain of the m1/m2 mosfet.

This means that using our values provided so far:

$A = \frac{10*gm_1}{g_6+g_8}$

$BW = \frac{GB}{A}$

$GB = 10 * \frac{gm_1}{2*20pF}$

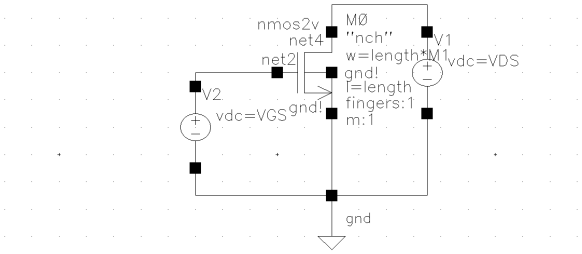
$SR = \frac{10*30.30\mu A}{2*20pF}$

We set the width to length ratio for M1 to 100 and

Part 3

Analytically determine the output signal swing for a common-mode input of -200mV

First step was to determine the width to length values. Lambda is the Channel length modulation parameter. This was done with a simple test bench containing one transistor.

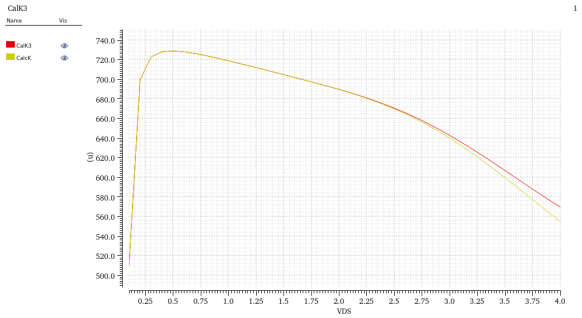


The equations used to create find these values are as follows:

Name	Type	Details	Plot	Save	Spec
Filter	Filter	Filter			Filter
	signal	/net2	☑	☑	
	expr	VT("/net2")	☑	☐	
ro	expr	OP("/M0" "rout")	☑	☐	
	signal	/net4	☑	☑	
	signal (I)	/M0/D	☑	☑	
	expr	OP("/M0" "gm")	☑	☐	
vth	expr	OP("/M0" "vth")	☑	☐	
id	expr	OP("/M0" "id")	☑	☐	
ids	expr	OP("/M0" "ids")	☑	☐	
Lambda	expr	(1 / (ro * ids))	☑	☐	
VDS	expr	VAR("VDS")	☑	☐	
VGS	expr	VAR("VGS")	☑	☐	
M1	expr	VAR("M1")	☑	☐	
NonK	expr	(M1 * ((VGS - vth)**2) * (1 + (Lambda * VDS)))	☑	☐	
CalcK	expr	(ids / NonK)	☑	☐	
CalK2	expr	(ids / (M1 * ((VGS - vth)**2)))	☑	☐	
Lambda2	expr	waveVsWave(?x getData("m0:ids" ?result "dc") ?y v("/net2" ?result "dc"))	☑	☐	
PCLM	expr	OP("/M0" "plcm")	☑	☐	
/M0	oppoint	/M0	☐	☑	
Lambda3	expr	(1 / OP("/M0" "vearly"))	☑	☐	
CalK3	expr		☑	☐	

What is concering is that despite having a constant VGS and accounting for VDS changes with lambda

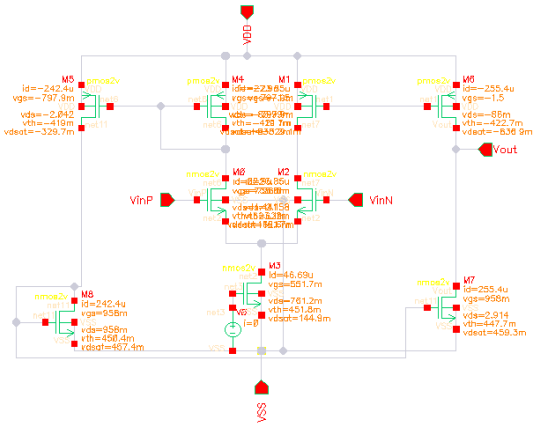
we still see this curve in the constant K value.

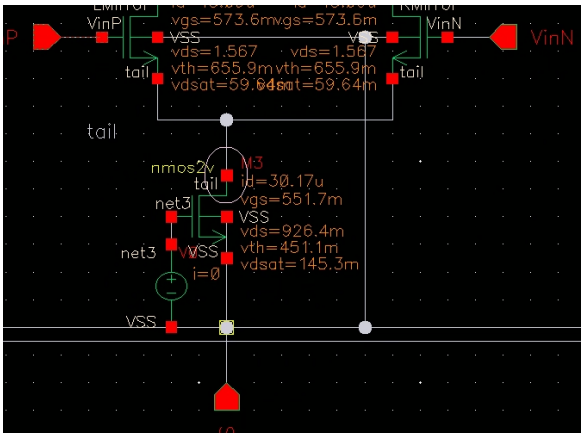


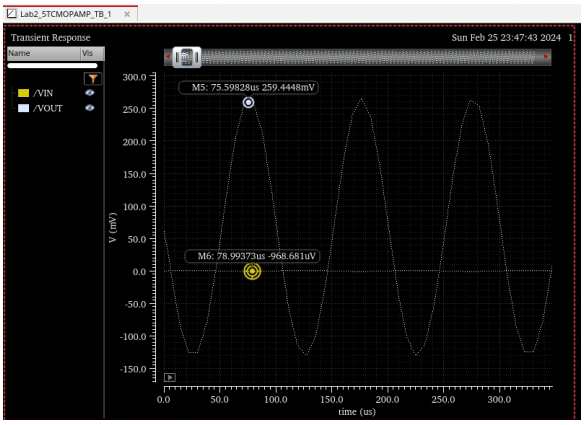
Part 4

Compare the results obtained in part 2 and part 3 with computer simulations.

Because of the model we used in the lab the simple saturation model for the transistor was not accurate. We had to edit our width to length to 8.







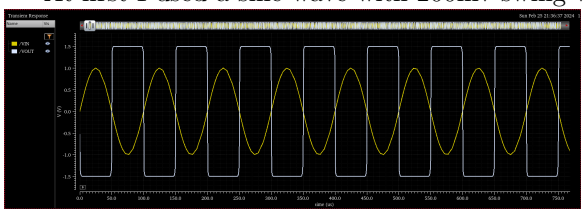
Part 5

What is the 3dB bandwidth when feedback is applied to form a unity- gain buffer?

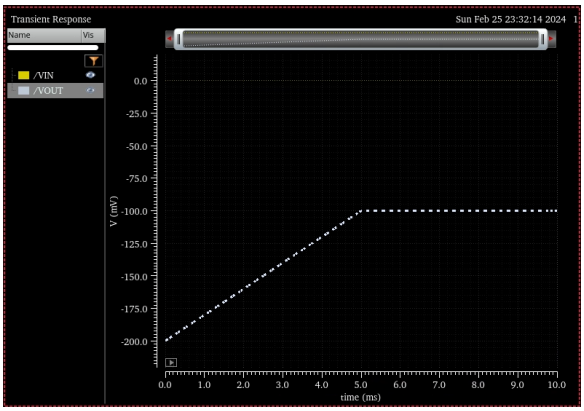
Part 6

What is the response of the unity-gain feedback amplifier to a 100mV step input with a common-mode input of -200mV?

At first I used a sine wave with 200mv swing without unity gain.



After fixing the testbench and using a input of -200mV the graph had a unity gain



Part 7

Determine the poles and zeros using a Spice analysis for both the open-loop and closed-loop amplifier. The feedback should provide a dc gain of +1. Plot the two dominant open-loop and closed-loop poles