EE 435 Lab 2 Spring 2024

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GitHub Page

Operational Amplifier Design

The operational amplifier is one of the most widely used analog circuits with virtually all analog and mixed-signal circuit designers being expected to be knowledgeable about both the design and operation of the operational amplifier. Although the concept of the operational amplifier is very fundamental and although there have been a very large number of operational amplifiers designed by a large number of engineers, the design of operational amplifiers continually presents challenges even to experienced designers. In this experiment, emphasis will be placed on the design of the most basic operational amplifier, a single-stage amplifier with differential inputs and a single-ended output using a tail-current bias. This basic structure can be systematically derived from either an n-channel or a p-channel quarter circuit. The structure of this amplifier, based upon the n-channel quarter circuit is shown in Fig. 1 where the transistor M9 has been used to generate the tail-current bias.

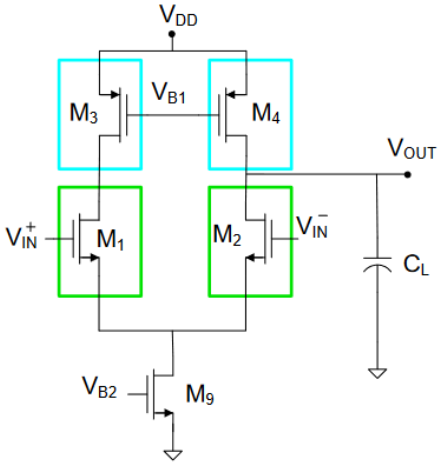

Fig. 1. Basic Operational Amplifier

Although this circuit will work fine for the appropriate value of bias voltage VB1, a common-mode feedback circuit (CMFB) is generally required to generate this bias voltage and there is modest circuit overhead associated with the CMFB biasing circuit. These will be discussed later in the course. Since only a single-ended output is being used on this circuit, the voltage on the drain node of M1 is not critical and it can be shown that this node can be used to bias M3 and M4 without requiring a CMFB. The modified version of this amplifier is shown in Fig. 2 where the gates of M3 and M4 are connected so as to form a current mirror of the current in M3 to that in M4

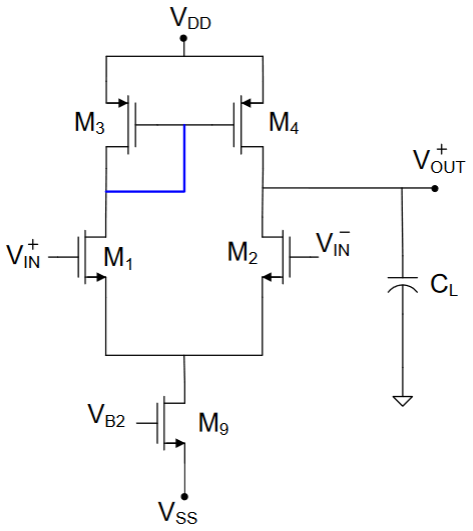

Fig. 2 Basic Operational Amplifier with Current-Mirror Biasing

Fig. 2 where the gates of M3 and M4 are connected so as to form a current mirror of the current in M3 to that in M4. .VDD M1 M2 VB2 M3 M4 VIN VIN CL M9 VOUT VSS Fig. 2 Basic Operational Amplifier with Current-Mirror Biasing Our goal in this experiment will be to design an operational amplifier based upon this architecture and to compare the theoretical values for some of the key performance parameters of this structure with that obtained in a theoretical analysis. In this design, it will be assumed that the TSMC 0.18μ CMOS process is to be used, the supply voltages VDD and VSS are fixed at +1V and -1V respectively, the bias voltage VB2 is fixed at -0.3V, and the capacitor CL is given. It will be assumed that the quiescent input voltages are both 0V and the desired quiescent output voltage is also 0V though the amplifier can be operated over some range of common-mode input and quiescent output values. Consistent with the concept of symmetric circuits, it will be assumed that the circuit will be designed under the assumption that matching between the left-half and the right- half circuits is to be maintained.

Part 1

Determine the number of degrees of freedom in this design and list the design variables.

There are three degrees of freedom. We know with the traditional 4 transistor op amp we have four degrees. Now we after removing the need to bias the transistors 3 and 4 with a common mode feedback circuit, we also remove one parameter (and freedom) from the design.

Part 2

Design an operational amplifier using the architecture of Fig. 2 that can drive a capacitive load of 10pF using an analytical formulation for the amplifier. This design should result in determining all of the natural design parameters for this circuit. The amplifier should have a GB of at least 10MHz , a dc voltage gain of at least 100 when driving this load, and a p-p output swing of 0.5V for some common-mode input levels and some quiescent output level.

Using the following equations given in the lecture slides we can set our constraints.

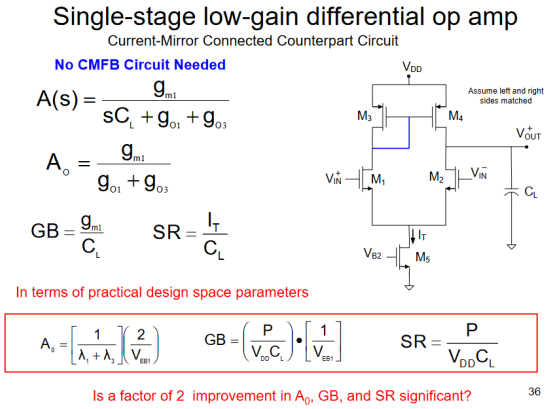

Figure 1: EE435 Lecture 5 Slide 36[?]

The first step was setting the gain to 100. This requires finding the λ_1 and λ_2 (the channel-length modulation parameter). It is defined as the following.

To find the value the following testbench was created.

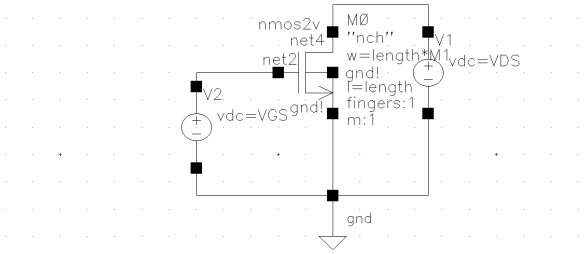

Figure 2: EE435 Lecture 5 Slide 36[?]

Name	Type	Details	Plot	Save	Spec
Filter	Filter	Filter			Filter
	signal	/net2	☑	☑	
	expr	VT("/net2")	☑	☐	
ro	expr	OP("/M0" "rout")	☑	☐	
	signal	/net4	☑	☑	
	signal (I)	/M0/D	☑	☑	
	expr	OP("/M0" "gm")	☑	☐	
vth	expr	OP("/M0" "vth")	☑	☐	
id	expr	OP("/M0" "id")	☑	☐	
ids	expr	OP("/M0" "ids")	☑	☐	
Lambda	expr	(1 / (ro * ids))	☑	☐	
VDS	expr	VAR("VDS")	☑	☐	
VGS	expr	VAR("VGS")	☑	☐	
M1	expr	VAR("M1")	☑	☐	
NonK	expr	(M1 * ((VGS - vth)**2) * (1 + (Lambda * VDS)))	☑	☐	
CalcK	expr	(ids / NonK)	☑	☐	
CalK2	expr	(ids / (M1 * ((VGS - vth)**2)))	☑	☐	
Lambda2	expr	waveVsWave(?x getData("m0:ids" ?result "dc") ?y v("/net2" ?result "dc"))	☑	☐	
PCLM	expr	OP("/M0" "plcm")	☑	☐	
/M0	oppoint	/M0	☐	☑	
Lambda3	expr	(1 / OP("/M0" "vearly"))	☑	☐	
CalK3	expr		☑	☐	

Figure 3: EE435 Lecture 5 Slide 36[?]

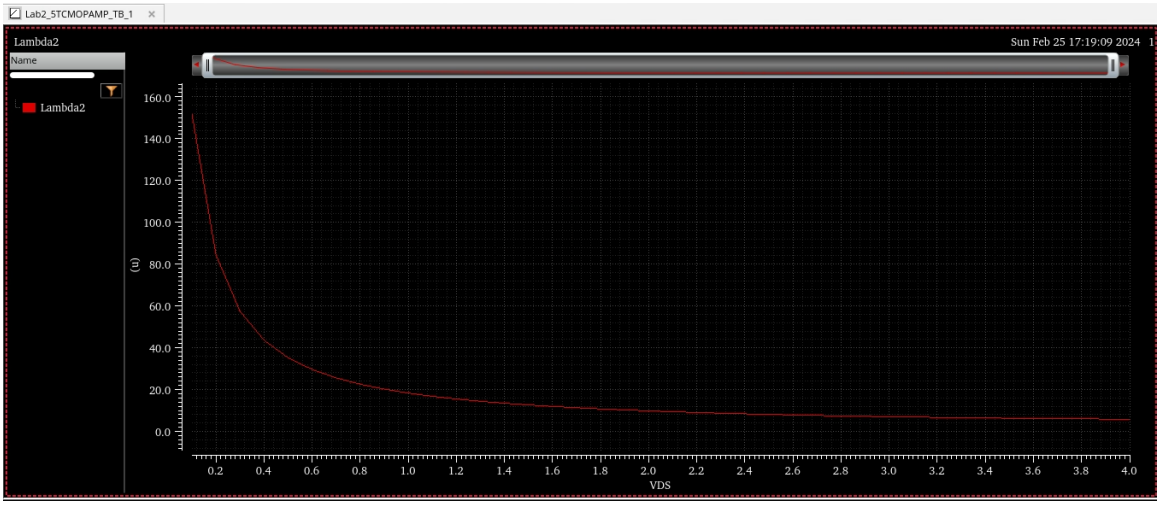

Figure 4: EE435 Lecture 5 Slide 36[?]

Part 3

Simulate the amplifier you designed in Part 2 in Specrtre using the TSMC 0.18μ CMOS process. Compare the dc gain, the GB, the output signal swing, and the SR with what you obtained by the analytical formulation.

Part 4

Make minor changes, if necessary, in the design so that the simulated performance meets the design requirements. Verify by computer simulations that the performance requirements have been met.

Part 5

Layout the circuit that you have designed and compare the post-layout extracted performance with that of your circuit schematic. Resolve the reasons for any discrepancies between the original schematic simulation and that of the extracted circuit.