CS2100: Computer Organisation
Lab #7: Multiply-by-5 Circuit
(Week 10: 18 – 22 October 2021)

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Remember to bring this along to your lab!

Name: Toh Jia-Yih Ronald Student No.: A0199937B

Lab Group: 2

Objectives:

In this experiment, you will create a multiply-by-5 circuit using a parallel adder.

IC chips:

1. One **74LS83 chip** (4-bit adder)
2. One **74LS20 chip** (DUAL 4-input NAND gates)

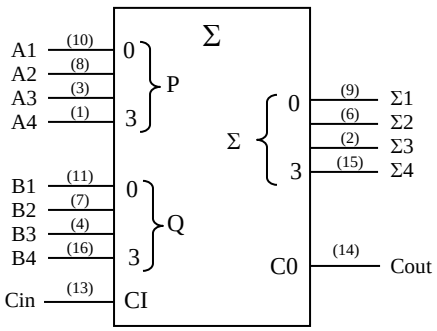


Figure 1a. Logic symbol† of 74LS83

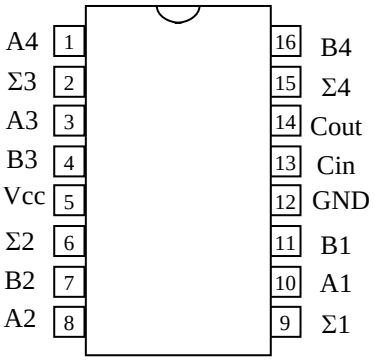


Figure 1b. Pin configuration of 74LS83

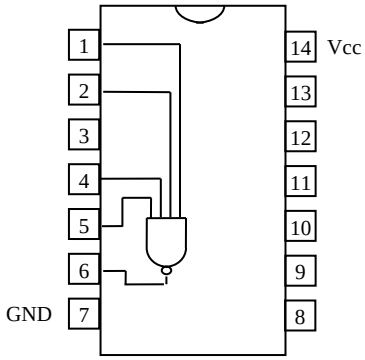


Figure 2. 74LS20 (partial; only one gate is shown)

† This symbol is in accordance with ANSI/IEEE St 91-1984 and IEC Publication 617-12.

Procedure:

1. You are to design a multiply-by-5 circuit given a 3-bit binary unsigned value *ABC* as its input. The circuit generates a 5-bit binary number $S_4\ S_3\ S_2\ S_1\ S_0$, and an output *V*.

   Since the circuit may not accommodate certain input value owing to the limited number of output bits, such an input value is deemed invalid, and the corresponding output will be don't-care values. The output *V* is used to indicate whether the input value is valid or not: 1 if the input value is valid, or 0 otherwise.

   Fill in the truth table below. [7 marks]

Inputs			Outputs					
A	***B***	***C***	S_4	S_3	S_2	S_1	S_0	***V***
0	0	0	0	0	0	0	0	1
0	0	1	0	0	1	0	1	1
0	1	0	0	1	0	1	0	1
0	1	1	0	1	1	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	1	0	1
1	1	1	x	x	x	x	x	0

2. Complete the K-maps for S_4 , S_3 , S_2 , S_1 and S_0 below (you should not leave any cell blank), and write out the simplified SOP (sum-of-products) expression for each of them. [5 marks]

S_4

A \ BC	00	01	11	10
0	0	0	0	0
1	1	1	x	1

$S_4 =$ A

S_3

A \ BC	00	01	11	10
0	0	0	1	1
1	0	1	x	1

$S_3 =$ B + A · C

S_2

A \ BC	00	01	11	10
0	0	1	1	0
1	1	0	x	1

$S_2 =$ A' · C + A · C'

S_1

A \ BC	00	01	11	10
0	0	0	1	1
1	0	0	x	1

$S_1 =$ B

S_0

A \ BC	00	01	11	10
0	0	1	1	0
1	0	1	x	0

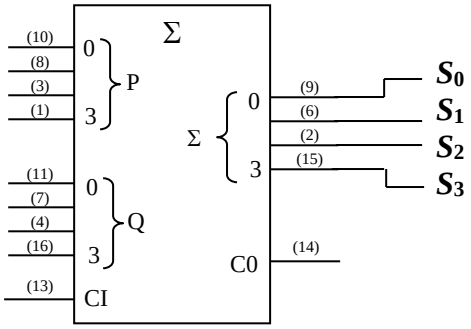
$S_0 =$ C

3. Now, implement the multiply-by-5 circuit using a 4-bit adder (74LS83 chip). The 4-bit adder is used to generate the 5-bit output $S_4S_3S_2S_1S_0$. You are not allowed to use any logic gate to generate the 5-bit output.

   In the following diagram, the outputs S_3, S_2, S_1, and S_0 have been filled for you. You are not allowed to change them. You are to complete the output S_4 and the inputs to the adder.

   For the output *V*, you are to use a NAND gate to implement it. The 74LS20 chip is meant for this purpose

   Draw the logic diagram for this circuit using the block diagram of 74LS83 (given in Figure 1a) and a NAND gate. [7 marks]



4. Show your circuit to your lab TA. [6 marks]

Marking Scheme: Report (19 marks), Circuit (6 marks); Total: 25 marks.
Your graded report will be returned to you at the next lab.