Remember to bring this along to your lab!

CS2100 Computer Organisation
Lab #8: Decoder
(Week 11: 25 – 29 October 2021)

[This document is available on LumiNUS and module website https://www.comp.nus.edu.sg/~cs2100]

Name: _____ Student No: _____

Lab Group: _____

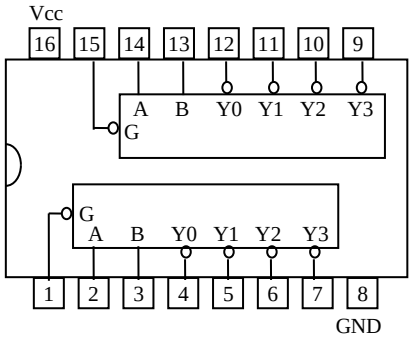
Objectives:

In this experiment, you will use the decoder to implement some logic functions.

IC chips:

1. One **74LS139** chip (DUAL 2×4 decoder with negated output and zero-enable).
2. One **74LS20** chip (DUAL 4-input NAND gates).

The decoder chip you will use in this lab is the 74LS139, which contains two sets of 2×4 decoder with *negated outputs* and *zero-enable*. The pin configuration and the function table are given below.

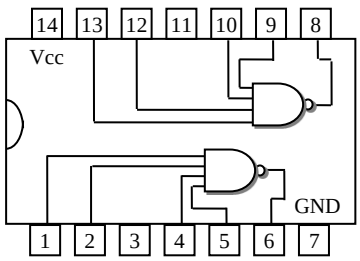


Function Table of 74LS139

INPUTS			OUTPUTS			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

1 = High, 0 = Low, X = don't care

The 74LS20 chip contains two 4-input NAND gates. The pin configurations are shown below.



74LS20

Propagation delay:

Assume that the propagation delay for every NAND gate in 74LS20 is 15 ns (nano-seconds), and the propagation delay for each decoder in 74LS139 is 35 ns.

Procedure:

1. Given a 3-variable function ***S(P,Q,R) = (P + Q + R)·(P + Q')·(P' + R)***, write this function in the **product-of-maxterms** form, using the Π*M* notation. [2 marks]

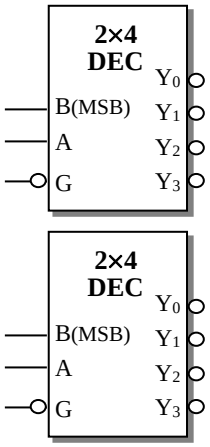
   $S(P,Q,R) = \Pi\ M\ ($ _____ $)$

2. Complete the truth table for *S* below. [2 marks]

P	***Q***	***R***	***S***
0	0	0	**0**
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

3. With the truth table above, implement function *S* using the 2×4 decoders in the 74LS139 chip, and NAND gates in the 74LS20 chip. Connect the inputs *P*, *Q*, and *R* to SW7, SW6 and SW5 on your logic trainer respectively.

   Complete the following logic diagram. [5 marks]



4. Show your implementation implementation of the above circuit to your lab TA before dismantling the circuit and moving on to another circuit in step 7. [5 marks]

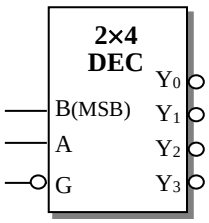
5. What is the propagation delay of your circuit above? _____ ns. [1 mark]

6. Given a 4-variable function $F(W,X,Y,Z) = \Pi M(3, 7)$, write out the simplified SOP expression for *F* below. [2 marks]

   Simplified SOP expression: $F =$ _____

7. Implement *F* using only **ONE** 2×4 decoder, without any additional logic gate. Connect *W*, *X*, *Y* and *Z* to SW7, SW6, SW5 and SW4 respectively. (You may find that you do not need to use all 4 inputs.) You circuit is considered wrong if it uses any additional logic gate, even though it produces the correct output.

   Complete the logic diagram below. [3 marks]

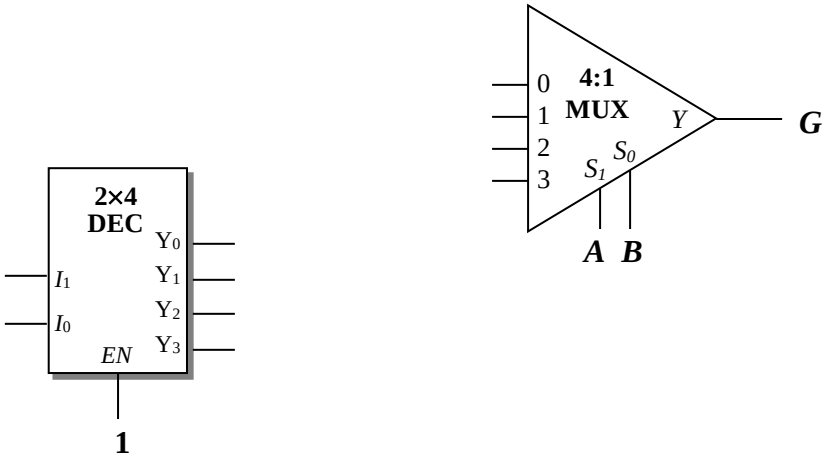


8. Show your implementation of the above circuit to your lab TA. [2 marks]

9. Using one 4:1 multiplexer and one 2×4 decoder with 1-enable as shown below, show how you might implement function $G(A,B,C,D) = \Sigma m(0, 6, 9, 15)$ without using any additional logic gate. Complete the diagram below. [3 marks]

   Note that the selector lines for the 4:1 multiplexer have been fixed to *AB*, and you must not change it.

   You do not need to implement this since you are not given any multiplexer in this lab.



Marking Scheme: Report (18 marks), Circuit (7 marks); Total: 25 marks.
Your graded report will be returned to you at the next lab.