Analysis of a Snubber for the T-Type NPC Converter

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***Abstract*—The study of a totally passive snubber applied to the T-type NPC converter is presented in this paper. The snubber circuit aids all commutations in all the switches. The voltage across the switches is clamped in a value close to half of the total input voltage. The description of the operation is presented in this paper.**

***Keywords*—Undeland Snubber, NPC T-type, soft commutation, soft switching**

I. Introduction

During the commutations of the converter, the presence of both voltage and current simultaneously may cause the called commutation losses. Being the commutations hard, the losses in a switch become directly proportional to the commutation frequency, thus limiting, for instance, the frequency increase and the possibility of reduction of the output filter volume. The hard switching also can impair the efficiency of a certain structure, as well as increase the necessary heatsink volume of the semiconductors. This work will present a passive snubber circuit without direct regeneration of energy, applicable to the T-type Three-Level Neutral-Point Clamped Inverter also known by the acronym T-type NPC [1], [2], [3], [4]. The presented snubber is derived from the Undeland Snubber [5], usually employed in half-bridge inverters, full bridge and conventional NPC inverters, including the contribution published by Peres [6], de Novaes [7] and Lima [8].

II. Description of the Operation Principles

The T-type NPC converter is a three-level topology featured by having a bidiretional switch clamping the load to the middle point of the input voltage link, as covered in [9] and [10]. It is shown in the Fig. 1.

At the conventional NPC converter the active switches are subject to half of the DC link voltage when bloquing [11]. Different from the conventional NPC, in the T-type NPC the half-bridge switches bloquing voltage is the entire DC link voltage, while the bloquing voltage of the neutral-point switches is half of the DC link voltage. Unlike the conventional NPC, the T-type NPC is usually employed for low voltage applications [12], [13], [14] although it is not limited to it. The topology presents high efficiency for applications with switching frequency under 20kHz, due to the low conduction losses. Therefore, the T-type deliver the result of having low conduction losses as the conventional two-level (2N) converter with the advantage of the low switching losses as an NPC converter [15], [16].

In applications such as photovoltaic energy processing the efficiency is an important issue. Medium switching frequencies (something between 10 and 20 kHz) are used to obtain smaller and cheaper passive components. Furthermore, the switching frequency might be elevated to a magnitude above 20kHz in residential applications in order to avoid audible noise. The increase of the frequency implies the reduction of the efficiency, which is bad in applications such as photovoltaic, where energy generation is expensive. The T-type topology already have a better efficiency in medium switching frequencies than the conventional NPC, therefore, the application of the snubber circuit here present can remove energy from the commutation, and this energy can be regenerate to the DC link by an auxiliary circuit which can lead the total efficiency to a higher level depending on the parameters of the project.

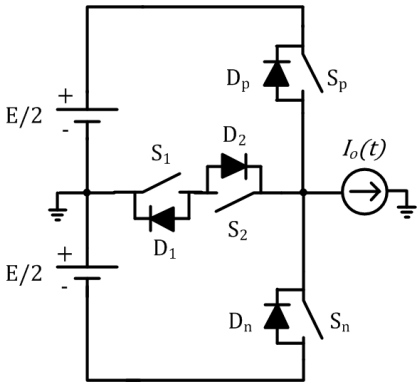

Fig. 1. T-type NPC converter topology

This paper presents the work of analysis for the application of a snubber circuit to the t-type NPC converter topology.

A. Single Snubber Operation

This section presents the converter operation for positive load voltage and positive load current, denominated as the first region of operation. The commutation sequency is shown on the Table I. For the analysis, the load is represented as an ideal current source.

TABLE I. Commutation Sequence

Device Switching Status				Output Voltage
S_p	S_2	S_n	S_1	
on	off	on	off	$E/2$
off	on	off	on	0
off	on	on	off	$-E/2$

The Fig. 3 shows the operating regions defined according to the polarity of voltage and current in the load.

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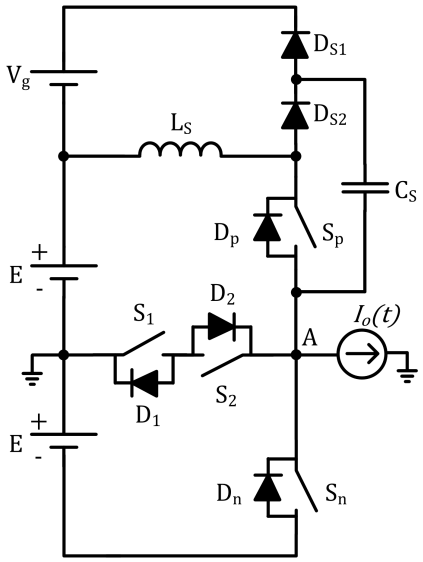

Fig. 2. Undeland snubber applied to the T-type NPC converter-1

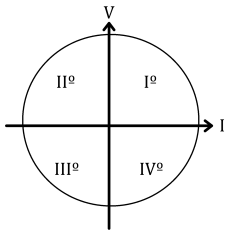

Fig. 3. Operating regions

The Fig. 4 presents the operating stages for the operation in the first region.

Stage 1(t_0, t_1)

In the first stage the S_p switch conducts the load current. All the remain switchs conduct no currents. The S_1 switch is commanded to close, while the S_2 and S_n switches are opened. The voltage across the C_s capacitor is zero. The voltage in the "A" node is equal to $E/2$. Energy is transferred to the load by the input source.

Stage 2(t_1, t_2)

The second stage starts when S_p is gated-off and S_2 is gated-on. The "A" node is connected to the middle point of the input voltage link, since S_1 and S_2 are gated-on. This propiciate the begining of a ressonant stage between L_s and C_s. The current through C_S starts to increase, being formed by two components, the load current I_o and one component due to the ressonance with L_s. The ressonant current circulates through S_2 and D_1. The voltage across the capacitor increases with limited slope which leads to the controlled rise of the voltage across the S_p switch, thus configuring a soft commutation. This stage ends when V_{Cs} reaches $E/2 + V_g$.

Stage 3(t_2, t_3)

When the voltage across the capacitor reaches $E/2 + V_g$, the D_{S_1} diode starts to conduct, current of the inductor L_S

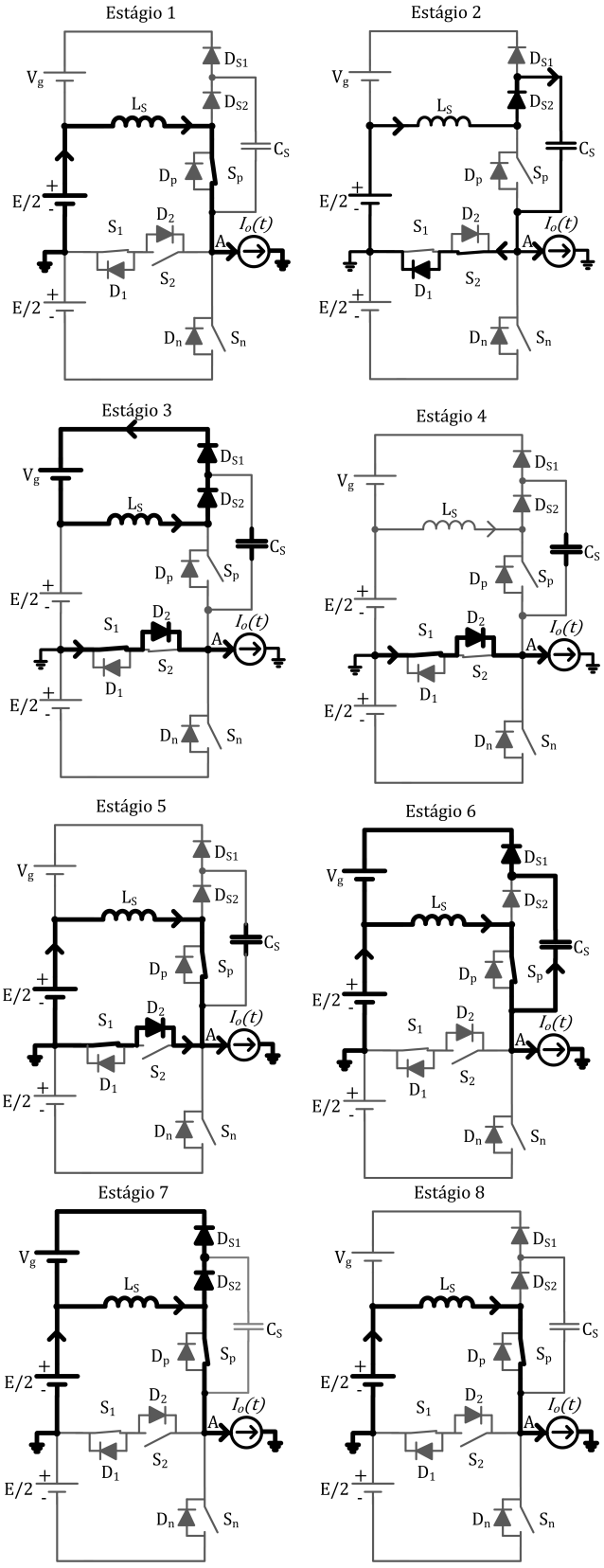

Fig. 4. Operating Stages- 1 to 8. The snubber capacitor when represented in bold means it is charged

starts to behave with a controlled slope, equal to $-V_g/L_s$, delivering energy to V_g. The capacitor remain charged, with voltage equal to $E/2 + V_g$. The load current now flows by S_1 and D_2 at the central branch. The voltage across the S_p switch is $E/2 + V_g$. and the stage ends when the inductor current reaches zero and the voltage across S_p passes to be $E/2$.

Stage 4 (t_3, t_4)

The fourth stage beggins when the inductor current reaches zero. The voltage at the "A" node is zero. This stage lasts until the time in which the S_p switch is gated-on once more.

Stage 5 (t_4, t_5)

The fifth stage is started when the S_p switch is gated-on and S_2 is gated-off. Thus the voltage across L_s becomes $E/2$ and the current circulating on it has the slope equal to $\frac{E/2}{L_S}$. The load current I_o starts to reduce its magnitude at D_2 with the same slope. The current that starts to circulate through S_p is the same of the inductor so the commutation is soft. The stage finish when the load current I_o circulates totally through S_p.

Stage 6(t_5, t_6)

Beggins when the current through D_2 goes to zero and the negative pole of the capacitor is connected to the "A" node and disconnected of the middle point. The voltage at the point "A" starts to increase until it reaches $E/2+V_g$ and, since there is voltage at the capacitor, the D_{S_1} diode conducts. It beggins a ressonant stage between L_S and C_S thus C_S returns energy to the input source. This stage ends when the voltage across C_S becomes zero.

Stage 7 (t_6, t_7)

The stage 7 starts when the capacitor voltage reaches zero. The D_{S_2} diode starts to conduct and the energy present in the inductor due to the last stage is returned to the V_g source.

Stage 8 (t_7, t_0)

The stage 8 starts when the current though the inductor is only the load current I_o. The voltage in the "A" node becomes $E/2$. This stage lasts until the beggining of the stage 1 in a new commutation cycle.

The Fig. 5 presents the waveform fot both current and voltage in the main semiconductors.

B. Commutation Analysis

This section analyses the commutation in all the switches fot the operation in the positive output voltage and current as shown in the Fig. 5.

1) S_p: At the instant t_1 occurs the bloquing of the S_p switch. The voltage across the capacitor C_S increases with controlled slope, as well as the voltage across S_p, thus performing a soft commutation.

At the instant t_4 the switch is gated-on, the current starts to circulate in S_p and is the same that goes through the inductor L_S meaning its rise is controlled, performing a zero voltage swithing.

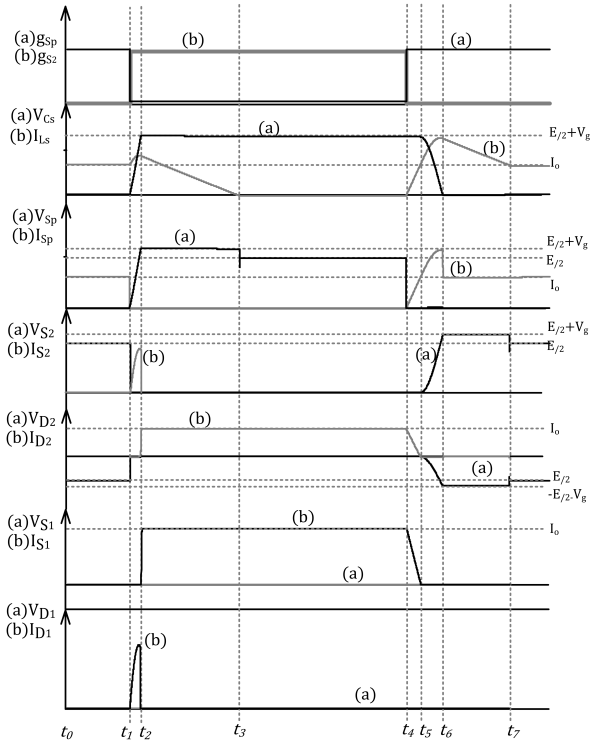

Fig. 5. Main waveforms-positive voltage and current at the load

2) S_2: At the instant t_1 the S_2 switch is gated-on and it starts to conduct a ressonant current coming from the ressonance between L_S and C_S. This current has a slope controlled, whitch leads to a zero voltage commutation.

At t_2 occurs the bloquing of S_2 and at this moment the voltage across the switch is already zero, performing a zero current switching.

3) D_2: At the instant t_2 the diode D_2 starts conducting I_o with zero voltage across it, since S_2 is already gated-on, leading to a zero voltage switching.

At the instant t_4 it begins the bloquing of the diode D_2 with the current decreasing until zero at the instant t_5 when the voltage across D_2 starts to rise controlled by the capacitor C_S, performing a zero current commutation.

4) S_1: At the insatnt t_2 the S_1 switch starts to conduct the load current I_o but the voltage across the switch is zero, since it remains gated-on all the first region of operation featuring a zero voltage commutation.

At the instant t_4 it begins the bloquing of S_1 which occurs with zero current since S_1 is gated-on.

5) D_1: At the insatnt t_1 the D_1 diode starts to conduct a sinusoidal current as well as S_2, and its voltage is zero, leading to a commutation with zero voltage.

The same occurs at t_2, when the current reaches zero in D_1 with zero voltage across the diode performing a zero current commutation.

C. Other Regions of Operation - Problems with commutation

In the second region of operation all the commutations are soft, as well as in the first region. Within the third region of operation, although, two problems occur: at the S_n switch the gate-on commutation is not soft. Furthermore, in the fourth region of operation both the gate-on and gate-off commutations of the S_1 switch are not soft. Once there are problems with the commutations with the operation of one snubber applied to the T-type converter, the work was lead to the analisys of two snubber circuits, one applied at the upper switch and a second one in the lower switch. The analisys is presented in the following section.

D. Double Snubber Operation

The Fig. 6 shows the circuit of T-type converter with two snubber circuits, one intended to aid the commutations of the upper switch and the second to aid the lower switch. Both aids the commutation of the central switches.

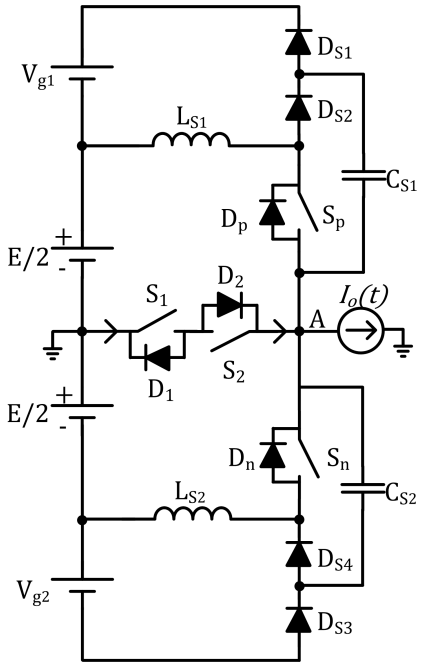

Fig. 6. The Undeland snubber applied to the T-type NPC converter - 2

The stages of operation are similar to the single snubber, in which the upper snubber aids the commutations in the first region of operation while the lower snubber aids the commutations in the fourth region, eliminating the problem existing in the operations of single snubber in the fourth region.

Nevertheless, this two snubber topology does not eliminates all the problems existent.

As shown in the Fig. 7 there is still a current peak on S_1 provenient from the undesirable discharge of the upper snubber capacitor. This peak is just limited by the impedance of the neutral-point switches, once is the path of the discharge. The similar occurs on the first region, at the S_2 switch. Both of these problems occurs because, in a given region, the capacitor of the snubber in opposition with the one which is operating ends up charging itself and the snubber circuit being passive cannot control this situation.

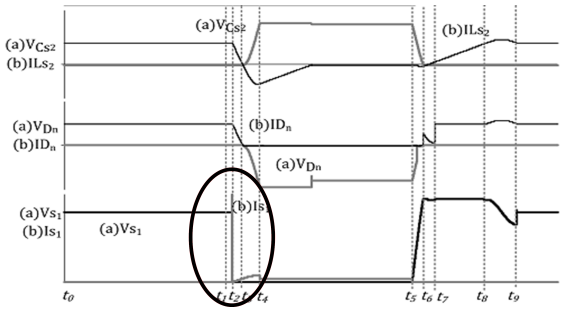

Fig. 7. Fourth region of operation - 2 snubbers

III. Snubber with Auxiliary Switch

In order to try to avoid the problem of the capacitors discharge, achieve soft commutation in all the switches and do not add extra operationg stages, a new snubber topology is proposed. The Fig. 8 shows the snubber with auxiliary switch, one for each the upper and the lower snubber circuit. At the first and second regions of operation the upper auxiliary switch remain gated-on allowing the normal operations of the upper snubber while the lower auxiliary is gated-off to avoid the interferencce of the lower snubber that is not required. The operation is opposite for the third and fourth regions.

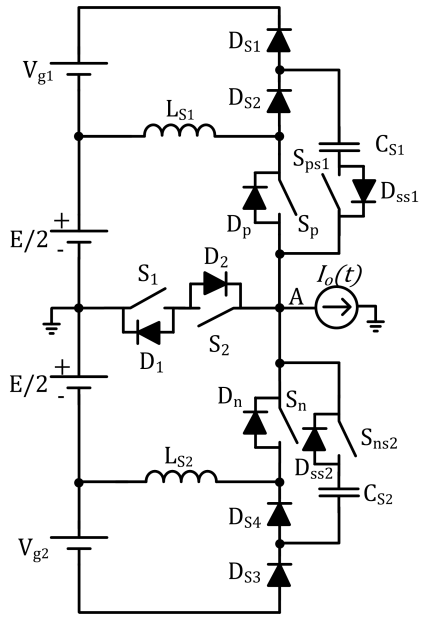

Fig. 8. Undeland snubber applied to the T-type NPC converter with auxiliary switch

The Fig. 9 shows the main waveforms to the operation of the snubber with the two auxiliary switches at the third region of operation.

The figure demonstrates that all the commutation are soft. The same occurs at all the regions of operation, since only the upper snubber works for the first and second regions, being disconnected on the third and fourth stages. Then the lower snubber operates on the third and fourth regions, being disconnected on the first and second regions of operation.

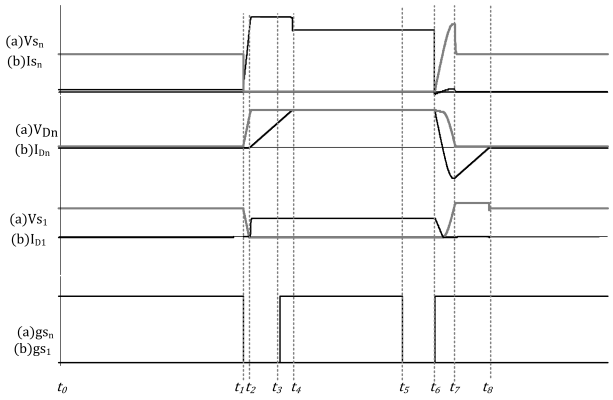

Fig. 9. Main waveforms of the T-type NPC converter with 2 auxiliary switches at third region

A. Simplified Parameter Design

The calculation of the snubber inductor L_s is obtained using the Stage 5 described in Section I. The fifth stage is started when the S_p switch is gated-on and S_2 is gated-off. Thus the voltage across L_s becomes $E/2$ and the current circulating on it has the slope equal to $\frac{E/2}{L_S}$. The load current will increase until it becomes I_o. The stage ends when the load current I_o circulates totally through S_p. The fundamental equation of the voltage across the inductor is described as:

$$V_{Ls} = Ls\frac{diL}{dt} \tag{1}$$

The current diL within the interval dt is equal to I_o. The time interval dt must be chosen according to the fall time (t_{fv}) of the voltage across the semiconductor being commutated. The procedure is to let the current reach the final value of I_o an amount of time after t_{fv} has been passed, so the voltage is already close to zero. This way the commutation losses will be close to zero. For example, for $t_{fv} = 150s$ the time dt was used 10 times greater then t_{fv}. This way one can obtain the equation that describes the value of L_s, where is used $k = 10$:

$$Ls = kV_{Ls}\frac{t_fv}{I_o} \tag{2}$$

For the simulated circuit the parameters are $I_o = 20A$, $t_fv = 150ns$ and $V_{Ls} = \frac{E}{2} = 200V$, so the inductor L_s obtained is:

$$Ls = kV_{Ls}\frac{t_fv}{I_o} = 15\mu H \tag{3}$$

The calculation of the snubber capacitor C_s is obtained using the Stage 2 of the operations description in Section I. The second stage starts when S_p is gated-off and S_2 is gated-on. The "A" node is connected to the middle point of the input voltage link, since S_1 and S_2 are gated-on. This propiciate the begining of a ressonant stage between L_s and C_s. The current through C_S starts to increase, being formed by two components, the load current I_o and one component due to the ressonance with L_s. The ressonant current circulate through S_2 and D_1. The voltage across the capacitor increases with limited slope which leads to the controlled rise of the voltage across the S_p switch, thus configuring a soft commutation. This stage ends when V_{Cs} reaches $E/2 + V_g$. The fundamental equation of the current across the capacitor is described as:

$$I_{Cs} = Cs\frac{dVc_s}{dt} \tag{4}$$

The voltage dVc_s at the end of the interval dt is equal to $E/2 + V_g$. The time interval dt must be chosen according to the fall time (t_f) of the current across the semiconductor being commutated, aiming to let the voltage reach the final value of $E/2 + V_g$ a certain amount of time after t_f has been passed, so the current is already close to zero, so will be the commutation losses close to zero. For example, for $t_f = 150s$ the time dt was used 3 times greater then t_f. If the ressonant current is not considered, using only the I_o component one can easily obtain the equation witch describe the value of C_s, where $k = 3$ was used, and the value of the capacitor obtained was:

$$Cs = kI_{Cs}\frac{t_f}{E/2 + V_g} = 40nF \tag{5}$$

The voltage source V_g used must be a value that do not causes overvoltage to the switch S_p, just the necessary tho clamp the voltage across it, being between 5% and 10% of the half of the link voltage. For the simulations the value used was $V_g = 35V$.

This values presented in this section were used in all the simulation work witch generated the waveforms presented in the work.

IV. Conclusion

The topology with two auxiliary switches avoids the undesirable discharge of the snubber capacitor in the region where it is not required. The current which circulates through the auxiliary switches comes from the ressonance between L_s and C_s, equal to the one which circulates in the other snubber components. The disadvantage of this snubber is that it adds two switches without regenarating the energy of the commutations, even though the energy can be regenerated to the input DC link with a simple DC-DC converter. The snubber circuit is suitable for medium power converters using the T-type converter in which the amount of energy removed from the commutations with medium switching frequency is more significant. Future works include the evaluation of experimental results, the detailed analysis of the behaviour of the auxiliary switch in combination with the snubber capacitor and the quantitative analysis, where all the equations that describe the circuit are obtained. The snubber can be applied also for the full-bridge configuration of the T-Type NPC converter, as well for the 3-phase configuration.

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