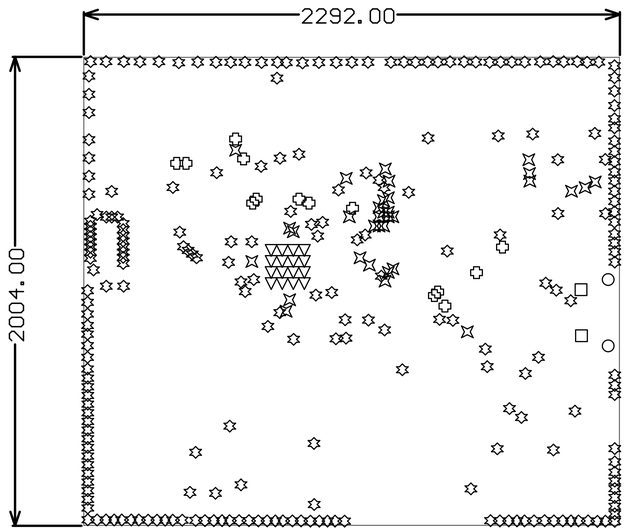
Symbol	Count	Hole Size	Plated	Hole Type	Hole Length	Routed Path Length
○	2	32.48mil (0.825mm)	PTH	Slot	59.06mil (1.500mm)	26.57mil (0.675mm)
□	2	35.43mil (0.900mm)	PTH	Slot	39.37mil (1.000mm)	3.94mil (0.100mm)
✣	14	7.00mil (0.178mm)	PTH	Round	-	-
▽	16	12.99mil (0.330mm)	PTH	Round	-	-
✖	33	6.00mil (0.152mm)	PTH	Round	-	-
✡	238	8.00mil (0.203mm)	PTH	Round	-	-
	305 Total					

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack
1	Top Overlay					
2	Top Solder	Solder Resist	0.40mil	3.5		
3	Top	Copper	1.40mil			
4	Core 1	FR-4	5.00mil	4.2		
5	Layer 2	Copper	0.70mil			
6	Core 2	FR-4	10.00mil	4.2		
7	Layer 3	Copper	0.70mil			
8	Core 3	FR-4	5.00mil	4.2		
9	Bottom	Copper	1.40mil			
10	Bottom Solder	Solder Resist	0.40mil	3.5		
11	Bottom Overlay					



NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: COPPER CLAD PLASTIC SHEET PER IPC-4101
   ROHS COMPLIANT TG 140 FR-4
   TYPE GFN FINISHED COPPER WEIGHT TO BE: 1 OZ.
   OVERALL BOARD THICKNESS TO BE .025 +/-.005.
2. UNLESS OTHERWISE SPECIFIED ALL HOLE DIMENSIONS APPLY AFTER PLATING.
3. ALL HOLES SHALL BE LOCATED WITHIN 0.003 DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.003. ADD TEARDROPS AS REQUIRED SO THAT ALL HOLES SURROUNDED BY LAND SHALL HAVE A MINIMUM ANNULAR RING OF 0.002.
4. CONDUCTOR WIDTHS AND SPACING SHALL BE WITHIN +/- 20% OF ARTWORK ORIGINALS.
5. APPLY SOLDERMASK (LIQUID PHOTO IMAGEABLE) OVER BARE COPPER, SOLDERMASK TO BE PER IPC-SM-840, CLASS T, COLOR: TRANSPARENT GREEN. ALL EXPOSED CONDUCTIVE SURFACES TO BE IMMERSION GOLD OVER ELECTROLESS NICKEL (ENIG) PER IPC-4552.
6. WARP OR TWIST OF BOARD SHALL NOT EXCEED 0.75%.
7. APPLY SILKSCREEN, AS REQUIRED, USING WHITE EPOXY INK.
8. REMOVE ALL BURRS AND BREAK SHARP EDGES 0.001 MAX.
9. FABRICATE IN ACCORDANCE WITH IPC-6012, TYPE 2, CLASS 2.
10. DIMENSIONS AND TOLERANCES PER ANSI Y14.5.
11. SURFACE MOUNT PAD SOLDER PLATING MUST BE FLAT TO A MAXIMUM OF 0.001 ABOVE BOARD SURFACE.
12. ALL COPPER SET BACK MUST BE MAINTAINED WITHIN ARTWORK ORIGINALS FROM ANY EDGE OF P.C. BOARD (i.e O.D., I.D, NON-PLATED THROUGH HOLES, NON-PLATED RADIUS, GROOVES AND SLOTS).
13. ALL VIAS TO BE TENTED UNLESS EXPLICITLY CLEARED IN GERBERS
14. DO NOT CHANGE GERBERS WITHOUT WRITTEN APPROVAL

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ENGINEER: S. Dandona	TITLE: Dev. Board Fab Drawing	
PCB DESIGNER: S. Dandona		
DATE: 6/13/2016	PART NO.: JDB-001	REV: 1
FILE NAME: JDB-001.PcbDoc	DWG NO:	SCALE: