Mid Sem. Monsoon2022: VLSI Digital (EC2.201)

Max. Time: 90 Mins [4:30 to 6:00 PM] Date: 22/09/2022

Note(s): No query is allowed during exam.
Write your assumptions (if any) for each question.

Q 1. [5 Marks] [CO-1]

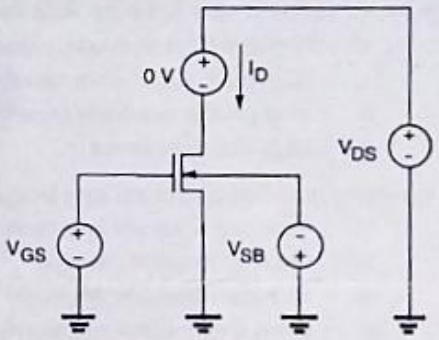
Consider two NMOS transistors working in saturation with same V_{GS} and V_{DS}

a) If two devices are matched except maximum possible mismatch in their (W/L) ratios of 3%. What is the maximum resulting mismatch in the drain currents

b) If two devices are matched except maximum possible mismatch in their V_t values of 10mV. What is the maximum possible mismatch in the drain currents. Assume nominal value of V_t is 0.6V

Q 2. [5 Marks] [CO-1]

A set of I-V characteristics of an nMOS transistor at room temperature are shown in below (in Table) for different biasing conditions. Fig. shows measurement setup. Using the data, find the threshold voltage V_{T0}



V_{GS}	V_{DS}	V_{SB}	I_D (μA)
4V	4V	0.0V	256
5V	5V	0.0V	441
4V	4V	2.6V	144
5V	5V	2.6V	256

MOS Capacitance

Q 3. Answer the following questions [9 Marks] [CO-1]

(a) Draw a MOSFET Capacitance model (DC model) depicting distinct components of capacitance.

(b) The capacitances in MOSFET occurs due to _____

i. Interconnects
ii. Difference in Doping concentration
iii. Difference in dopant materials
iv. All of the mentioned

(c) The parasitic capacitances found in MOSFET are _____

i. Oxide related capacitances
ii. Inter electrode capacitance

iii. Electrolytic capacitance
iv. All of the mentioned

(d) In Cut-off region (assume MOS is in accumulation), the capacitance Cgs will be equal to _

i. $2C_{GDO}$
ii. $C_{GSO}.W$
iii. C_{GB}
iv. All of the mentioned

(e) In cut-off region (assume MOS is in accumulation), the value of gate to substrate capacitance is equal to _____

i. Cox .(W- L)
ii. $C_{GBO}.L + Cox\ W/L$
iii. $C_{GBO}.L + Cox^* W^*L$
iv. 0

(f) In linear mode operation, the parasitic capacitances that exists are _____

i. Nonzero Gate to source capacitance
ii. Nonzero Gate to drain capacitance
iii. Zero gate to substrate capacitance
iv. All of the mentioned

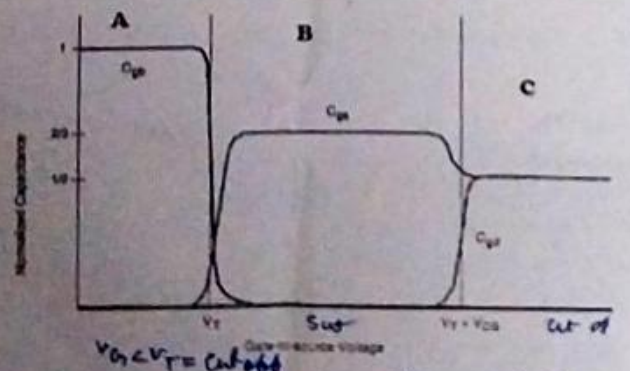
(g) In saturation mode operation, gate to drain capacitance (channel) is zero due to_____

i. Gate and drain are interconnected
ii. Channel length is reduced
iii. Inversion layer doesn't exist
iv. Drain is connected to ground

(h) When MOSFET is operating in saturation region, the gate to source capacitance (channel) is?

i. $1/2^*Cox^*W^*L$
ii. $2/3^*Cox^*W^*L$
iii. Cox^*W^*L
iv. $1/3^*Cox^*W^*L$

(i) In the below graph, the regions marked as A, B, C are?



$V_{GS} < V_T$ = Cutoff

i. A : Saturation, B : Linear, C : Cut-off

$V_{GS} < V_T + V_{DS}$

$V_{DS} < V_{GS} - V_T$ - Lin

$V_{DS} > V_{GS} - V_T$ - Sat

ii. A : Cut-off, B : Linear, C : Saturation

iii. A : Linear, B : Saturation, C : Cut-off

iv. None of the mentioned

Hint: Analyse the graph from the gate to source voltage on x axis and regions can be determined.

Noise Margin

Q 4. [10 Marks] [CO-1, CO-2]

Consider a resistive-load inverter with V_{DD}=5V, transconductance (k_n') = 20 μA/V², V_{TO}= 0.8 V, R_L= 200 KΩ, and W/L=2. Calculate the critical voltages (V_{OL}, V_{OH}, V_{IL}, V_{IH}) and on the VTC and find the noise margin of the circuit.

Are your calculated noise margins good? Please comment on the quality of the inverter design, and how can you improve it?

Power dissipation and propagation delays

Q 5. [10 Marks] [CO-2]

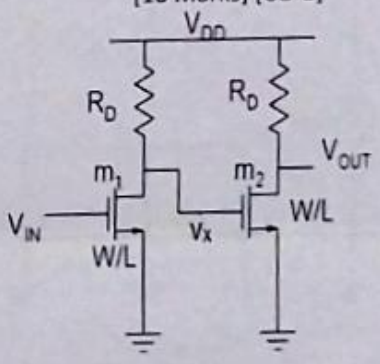
Consider a resistive-load inverter design, driving a similar inverter (as shown in Fig.). Now answer the following-

(a) What is the net capacitance at node V_X.

(b) Let's say the input (V_{IN}) is abruptly switching from V_{DD} to 0. What is the state/region of each MOS (m_1 and m_2) before and after the switching.

(c) Develop a simple expression for the calculation of low-to-high propagation delay (τ_{plh}).

(d) Discuss the parameters impacting the τ_{plh}. From the developed expression, how can you improve the operating speed of this resistive-load inverter? Discuss the trade-off. Also discuss the assumption considered.



Q 6. [6 Marks] [CO-1, CO-2]

How much is the dynamic power dissipated ($P_{dynamic}$) in 2-input resistive-load NAND gate for the following cases? Develop only equations.

(a) When input 'B'=1, and input 'A' switches with clock frequency.

(b) When input 'A'=1, and input 'B' switches with clock frequency.