Final Project

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EDA Tools used

- NG-SPICE
- Magic
- Verilog

NG SPICE

- After building basic gates using using *22nm* technology
  - NAND gate
  - OR Gate
  - AND Gate
  - NOT Gate
- Half adder was realized using 5 nand gates
- Full adder was realized 2 half adders and an or gate
- Four bit adder was realized using full adders
- And finally four bit multiplier using four bit adders
- Now we have calculate the delays by varying inputs using a python script and after calculating all the delays we observed the worst case was 15.6598 *ns*.
- Similarly we have calculated Leakage current by giving input as 0 and then calculating the current at the output and the observed values are in the text file.

Magic

The corresponding layouts were realized using *getcell* command and are in the corresponding *.mag* files

Verilog

- Verification of functionality of the multiplier was done using structural implementation.
- Different modules were built and then used these modules to build 4-bit Multipler