Analog IC Design: Course Project

A low-power low-noise CMOS amplifier for neural recording applications

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2021112022

There is a need among scientists and clinicians for low-noise low-power bio-signal amplifiers capable of amplifying signals in the millihertz-to-kilohertz range while rejecting large dc offsets generated at the electrode–tissue interface. The advent of fully implantable multielectrode arrays has created the need for fully integrated micropower amplifiers.

1. Design Specifications

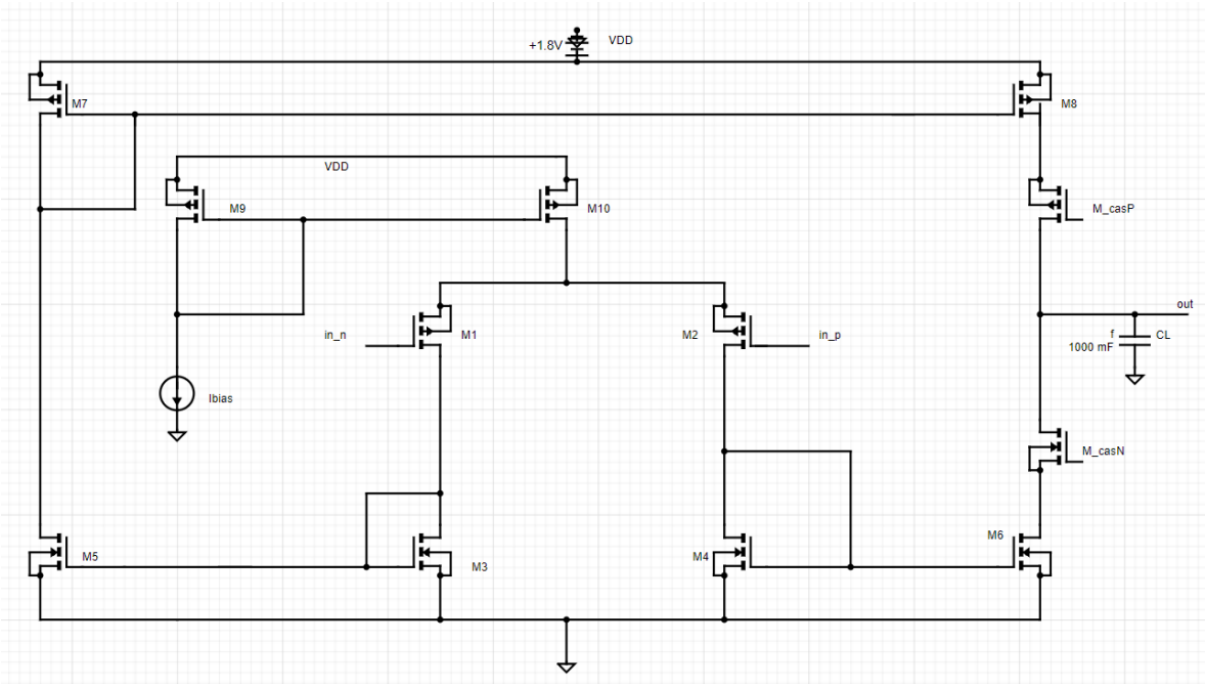
We are given to design the low noise low power neural amplifier (Fig. 1 in the paper) using the OTA topology (Fig. 4 in the paper) given in the following research paper: R. R. Harrison and C. Charles, *A low-power low-noise CMOS amplifier for neural recording applications*.

The specifications of the design are as follows:

- DC gain $\geq$ 60dB
- -3dB bandwidth $\geq$ 10kHz
- Input referred noise $\leq 2\mu V_{rms}$.
- CMRR $\geq$ 100dB
- Noise Efficiency Factor(NEF) ≤ 4
- DC power consumption $\leq$ 30 µA.
- Supply Voltage $\leq$ 1.8 V

2. Hand Calculations

a) OTA schematic using circuit-diagram.org is as follows including labelled transistors, resistors, and capacitors.



b) The step-by-step design procedure and calculations are as follows.

Given

$I_{DC} \leq 30\mu A$

$V_{DD} = -V_{SS} = 1.8\,V$

Firstly we calculate the gain expression for this OTA.

The output resistance Rout is given by

$$g_{mn} r_o^2 \,\|\, g_{mp} r_o^2 \qquad \because g_{mn} = g_{mp}$$

$$\approx \frac{g_{mn} r_o^2}{2}$$

Now we find the incremental current expression

Referring to the circuit schematic above we have, the incremental current as follows considering V_- at ↓ and V_+ at ↑

for M_1 : $g_{m1} V_{in} \downarrow$ $\quad M_5 : (g_{m1} v_{in}) \left(\frac{g_{m5}}{g_{m3}}\right) \downarrow$

M_2 : $g_{m1} v_{in} \uparrow$ $\quad M_6 : (g_{m1} v_{in}) \left(\frac{g_{m6}}{g_{m4}}\right) \uparrow$

M_3 : $g_{m1} v_{in} \downarrow$ $\quad M_8 : (g_{m1} v_{in}) \left(\frac{g_{m5}}{g_{m3}}\right)\left(\frac{g_{m8}}{g_{m4}}\right) \downarrow$

M_4 : $g_{m1} v_{in} \uparrow$ $\quad (\because g_{m3} = g_{m4})$

So the incremental current $= g_{m1} v_{in} \left[\frac{g_{m8}}{g_{m4}} + \frac{g_{m6}}{g_{m4}}\right]$

So the differential gain is

$$A = g_{m1}\left(\frac{g_{m8}}{g_{m4}} + \frac{g_{m6}}{g_{m4}}\right)\left(\frac{g_{mn} r_o^2}{2}\right)$$

As $g_{m4} \cdot g_{m1} \geq 10^{-11}$

$$g_{m1} \geq \frac{10^{-11}}{42 \times 10^{-6}}$$

$$g_{m1} \geq 0.25\,\mu$$

Given that input reffered noise $\leq 2\,\mu V_{rms}$

Firstly the $\overline{v_{n,out}^2} = 4KTU\,(g_{m1} + g_{m2} + g_{m3} + g_{m4} + g_{m5} + g_{m6} + g_{m7} + g_{m8})$

as $\overline{v_{n,in}^2} = \frac{\overline{v_{n,out}^2}}{A^2}$

$$= \frac{8KTU}{g_{m1}}\left[1 + \frac{2g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}}\right]$$

as $\gamma = \frac{U}{2}$; we have.

$$\sqrt{\frac{16KT}{3g_{m1}}\left[1 + \frac{2g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}}\right]} \leq 2\,\mu V_{rms}$$

Now from NEF :

$$\overline{V_{in,rms}^2} \cdot \frac{2(2\pi f)}{\pi (2 \times 10^{-3})(4 \times 4.4 \times 10^{-21}) \times 10^4} \leq 16$$

$$V_{in,rms} \leq 2.1\,\mu$$

$$\frac{16\,KT}{3\,g_{m1}}\left[1 + \frac{3g_{m3}}{g_{m1}}\right] \leq 4 \times 10^{-12}$$

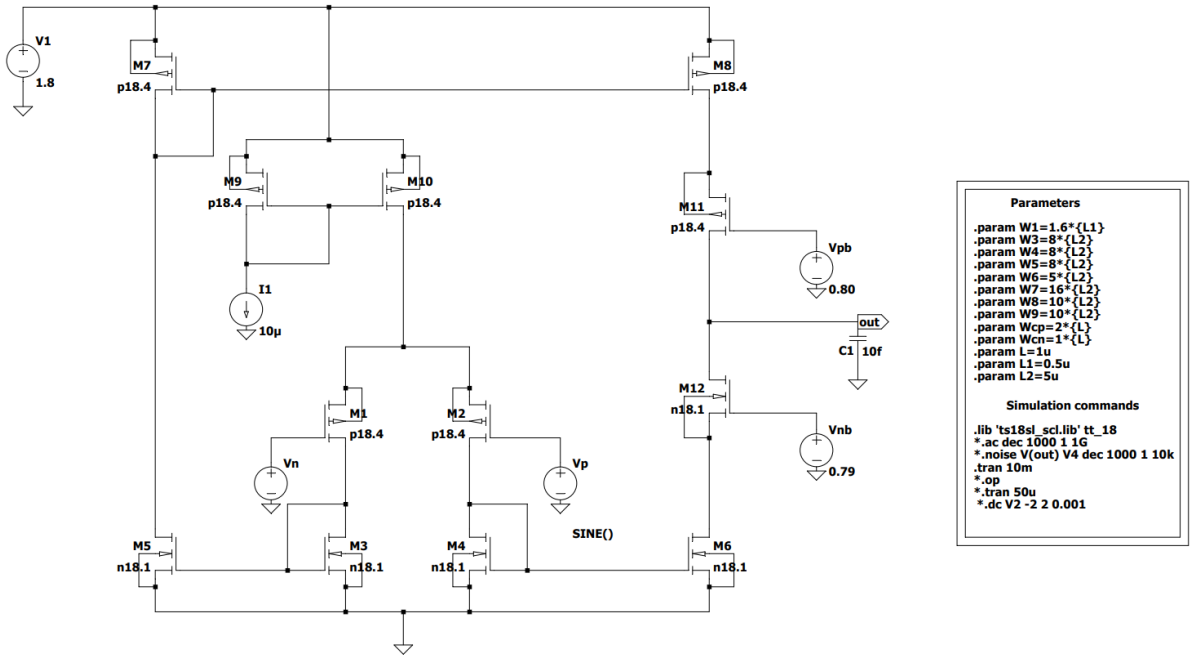
$$1 + \frac{3g_{m3}}{g_{m1}} \leq 7.66 \times 10^{3}$$

$$3g_{m3} \leq 320 \times 10^{-3}.$$

$$g_{m3} \leq 100\,m$$

3. OTA Simulations

a. Circuit Schematic

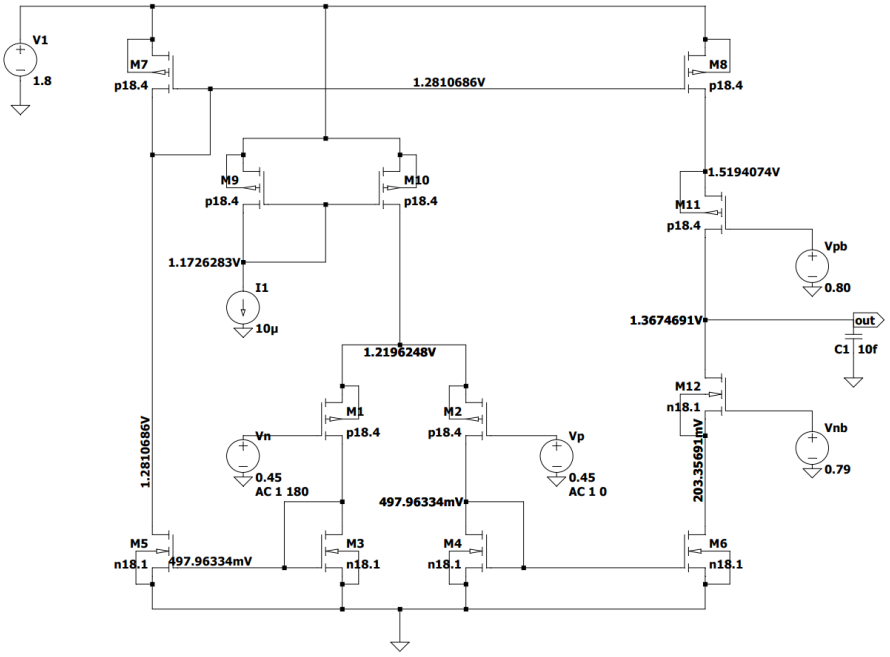


b. Design Parameters

Current I_bias	10µ
Load Capacitance	10fF
M1, M2	0.8µ/0.5µ
M3, M4, M5	40µ/5µ
M6	32µ/5µ
M7	80µ/5µ
M8	50µ/5µ
M9, M10	50µ/5µ
Mcasep	2µ/1µ
Mcasen	1µ/1µ

c. Operating Point

The Operating Point analysis of the OTA is as follows, where the DC voltage have been annotated at each node as instructed. We observe that all the transistors are biased to be in saturation.



The obtained values for Operating Point analysis are as follows.

```
        --- Operating Point ---

V(n008):        1.21962         voltage
V(n011):        0.45            voltage
V(n013):        0.497963        voltage
V(n009):        0.203357        voltage
V(n014):        0.497963        voltage
V(n001):        1.8             voltage
V(n002):        1.28107         voltage
V(n003):        1.51941         voltage
V(n006):        1.17263         voltage
V(out):         1.36747         voltage
V(n010):        0.79            voltage
V(n007):        0.8             voltage
V(n012):        0.45            voltage
```

Name:	m12	m4	m5	m6	m3
Model:	n18.1	n18.1	n18.1	n18.1	n18.1
Id:	3.13e-06	5.00e-06	5.02e-06	3.13e-06	5.00e-06
Vgs:	5.87e-01	4.98e-01	4.98e-01	4.98e-01	4.98e-01
Vds:	1.16e+00	4.98e-01	1.28e+00	2.03e-01	4.98e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	3.99e-01	3.70e-01	3.70e-01	3.70e-01	3.70e-01
Vdsat:	1.90e-01	1.18e-01	1.18e-01	1.18e-01	1.18e-01
Gm:	3.21e-05	9.45e-05	9.51e-05	5.87e-05	9.45e-05
Gds:	6.90e-08	5.81e-08	2.32e-08	5.10e-07	5.81e-08
Gmb	6.06e-06	1.74e-05	1.75e-05	1.08e-05	1.74e-05
Cbd:	2.44e-15	4.86e-13	3.99e-13	3.39e-13	4.86e-13
Cbs:	3.50e-15	5.98e-13	5.98e-13	3.74e-13	5.98e-13
Cgsov:	2.20e-16	8.80e-15	8.80e-15	5.50e-15	8.80e-15
Cgdov:	2.20e-16	8.80e-15	8.80e-15	5.50e-15	8.80e-15
Cgbov:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
dQgdVgb:	6.46e-15	1.09e-12	1.09e-12	7.15e-13	1.09e-12
dQgdVdb:	-2.21e-16	-1.10e-14	-8.88e-15	-4.88e-14	-1.10e-14
dQgdVsb:	-5.32e-15	-8.73e-13	-8.72e-13	-5.43e-13	-8.73e-13
dQddVgb:	-2.73e-15	-4.66e-13	-4.64e-13	-3.13e-13	-4.66e-13
dQddVdb:	2.66e-15	4.97e-13	4.08e-13	3.74e-13	4.97e-13
dQddVsb:	3.04e-15	5.53e-13	5.52e-13	3.44e-13	5.53e-13
dQbdVgb:	-1.00e-15	-1.61e-13	-1.62e-13	-8.93e-14	-1.61e-13
dQbdVdb:	-2.44e-15	-4.87e-13	-3.99e-13	-3.54e-13	-4.87e-13
dQbdVsb:	-4.49e-15	-8.39e-13	-8.38e-13	-5.23e-13	-8.39e-13

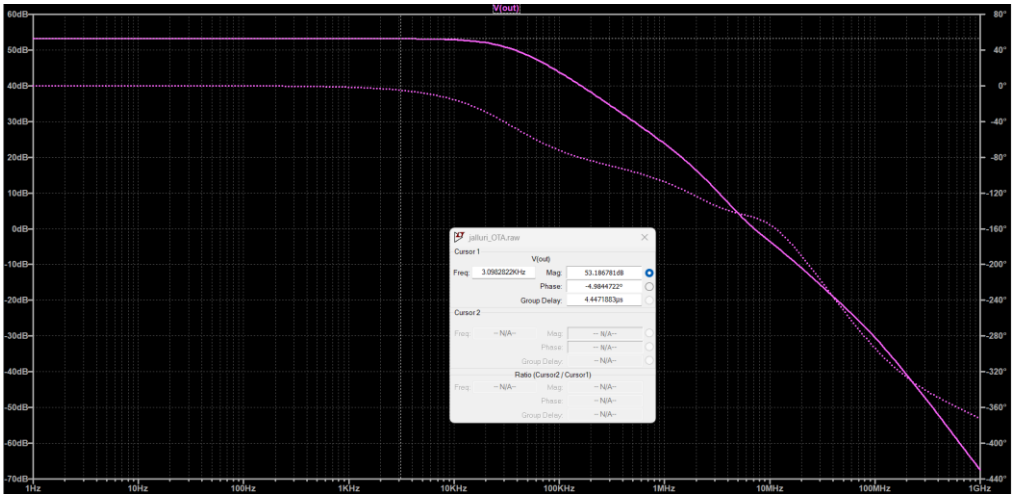
Name:	m11	m2	m7	m9	m10
Model:	p18.4	p18.4	p18.4	p18.4	p18.4
Id:	3.13e-06	5.00e-06	5.02e-06	1.00e-05	1.00e-05
Vgs:	-5.67e-01	-4.80e-02	0.00e+00	0.00e+00	-4.70e-02
Vds:	1.52e-01	7.22e-01	5.19e-01	6.27e-01	5.80e-01
Vbs:	1.52e-01	7.22e-01	5.19e-01	6.27e-01	5.80e-01
Vth:	-4.12e-01	-4.18e-01	-4.05e-01	-4.05e-01	-4.05e-01
Vdsat:	-2.66e-01	-2.99e-01	-1.20e-01	-2.00e-01	-2.00e-01
Gm:	1.39e-05	2.58e-05	6.78e-05	8.33e-05	8.32e-05
Gds:	1.23e-05	4.21e-07	5.44e-08	9.85e-08	1.12e-07
Gmb	4.41e-06	7.53e-06	2.08e-05	2.57e-05	2.57e-05
Cbd:	6.05e-15	1.49e-15	1.01e-12	6.29e-13	6.29e-13
Cbs:	5.70e-15	1.21e-15	8.37e-13	5.09e-13	5.15e-13
Cgsov:	5.20e-16	2.08e-16	2.08e-14	1.30e-14	1.30e-14
Cgdov:	5.20e-16	2.08e-16	2.08e-14	1.30e-14	1.30e-14
Cgbov:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
dQgdVgb:	1.60e-14	3.11e-15	2.25e-12	1.51e-12	1.51e-12
dQgdVdb:	-4.11e-15	-2.09e-16	-2.35e-14	-1.48e-14	-1.54e-14
dQgdVsb:	-1.08e-14	-2.59e-15	-1.81e-12	-1.28e-12	-1.28e-12
dQddVgb:	-7.45e-15	-1.29e-15	-9.01e-13	-6.30e-13	-6.31e-13
dQddVdb:	9.65e-15	1.70e-15	1.03e-12	6.44e-13	6.44e-13
dQddVsb:	5.97e-15	1.41e-15	1.17e-12	8.14e-13	8.15e-13
dQbdVgb:	-1.10e-15	-5.30e-16	-4.44e-13	-2.53e-13	-2.53e-13
dQbdVdb:	-8.62e-15	-1.50e-15	-1.01e-12	-6.30e-13	-6.30e-13
dQbdVsb:	-7.40e-15	-1.65e-15	-1.38e-12	-8.70e-13	-8.76e-13

Name:	m8	m1
Model:	p18.4	p18.4
Id:	3.13e-06	5.00e-06
Vgs:	-2.38e-01	-4.80e-02
Vds:	2.81e-01	7.22e-01
Vbs:	2.81e-01	7.22e-01
Vth:	-4.05e-01	-4.18e-01
Vdsat:	-1.20e-01	-2.99e-01
Gm:	4.22e-05	2.58e-05
Gds:	1.44e-07	4.21e-07
Gmb	1.30e-05	7.53e-06
Cbd:	6.29e-13	1.49e-15
Cbs:	5.63e-13	1.21e-15
Cgsov:	1.30e-14	2.08e-16
Cgdov:	1.30e-14	2.08e-16
Cgbov:	0.00e+00	0.00e+00
dQgdVgb:	1.42e-12	3.11e-15
dQgdVdb:	-2.87e-14	-2.09e-16
dQgdVsb:	-1.13e-12	-2.59e-15
dQddVgb:	-5.73e-13	-1.29e-15
dQddVdb:	6.54e-13	1.70e-15
dQddVsb:	7.30e-13	1.41e-15
dQbdVgb:	-2.71e-13	-5.30e-16
dQbdVdb:	-6.37e-13	-1.50e-15
dQbdVsb:	-9.05e-13	-1.65e-15

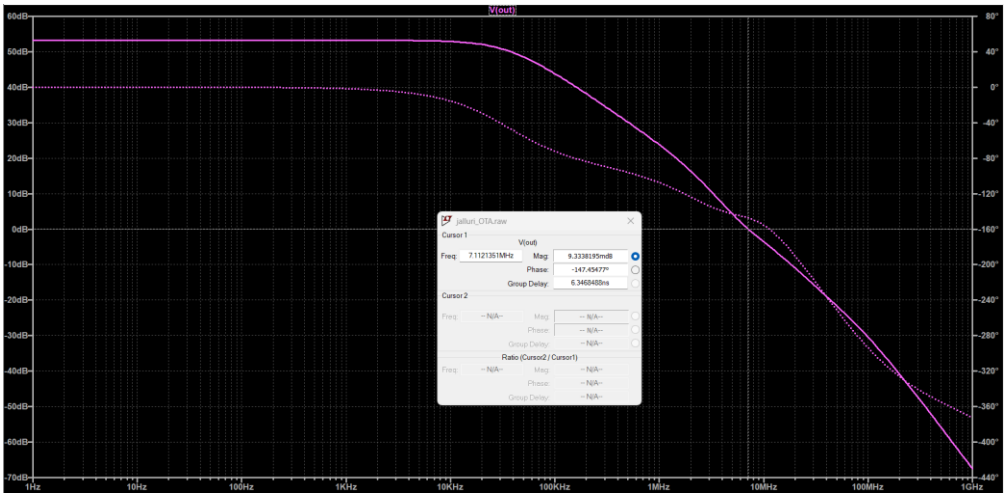
From the operating points obtained, it can be seen that all MOSFETs are in saturation mode. The current is mirrored as per the requirements. Hence, the devices are biased properly.

d. Stability Analysis

- The DC gain is observed to be 53.18dB



- The Unity gain frequency is observed to be 7.11MHz



- The phase margin is observed to be almost 37 degrees from the above graph.

e. Slew Rate

After giving a positive step from 0 to 1.8V with a rise time of 100 ps in unity gain feedback mode.

The slew rate = 522.05388ns/1.8 = 0.29MV/s = 0.29V//µs.

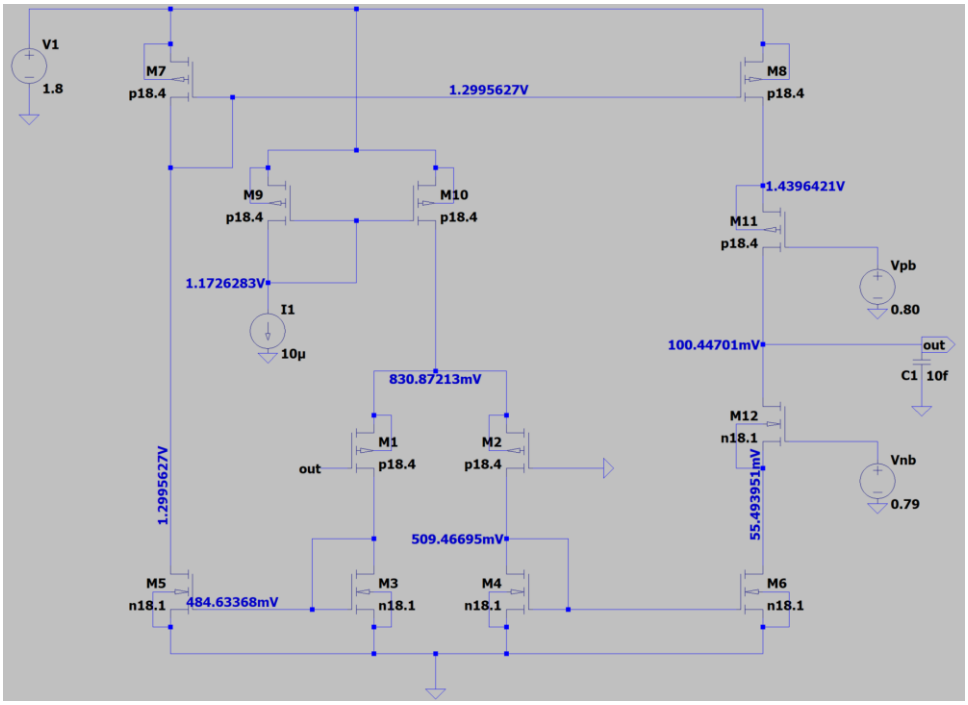
f. Settling Time

The settling time for 2% accuracy is when we apply the same step input as above and finding the settling time which is at V=1.764V

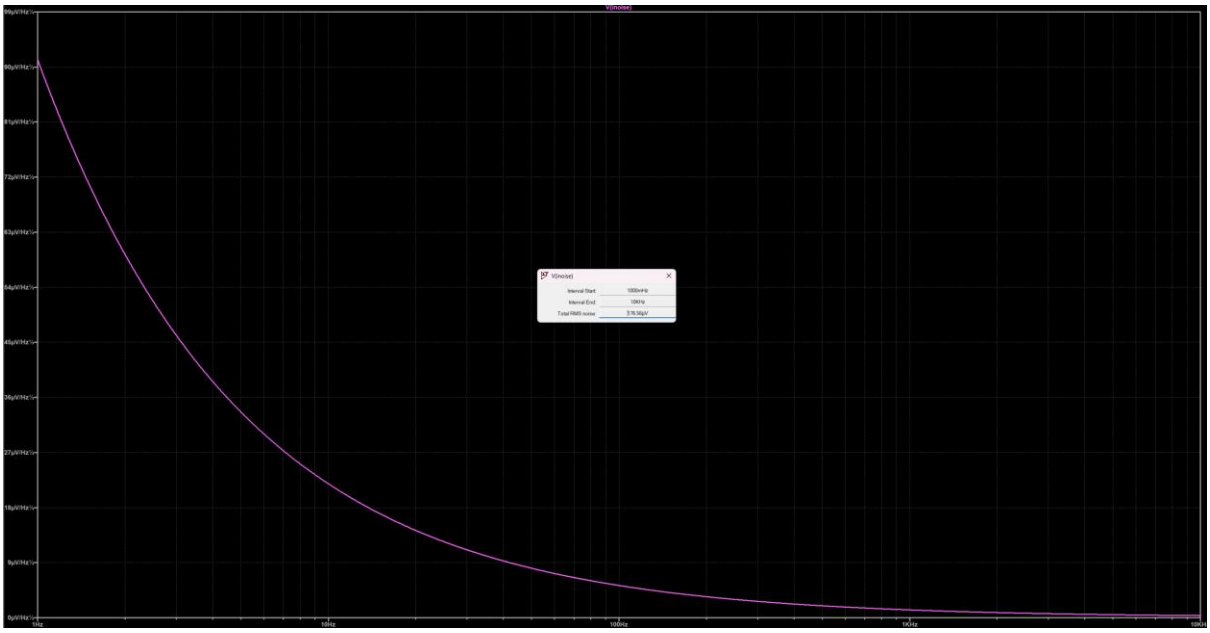
From the following plot we observe that the settling time is 194.19692ns.

g. Systematic Offset

The systematic offset obtained after following given steps is 100.44mV

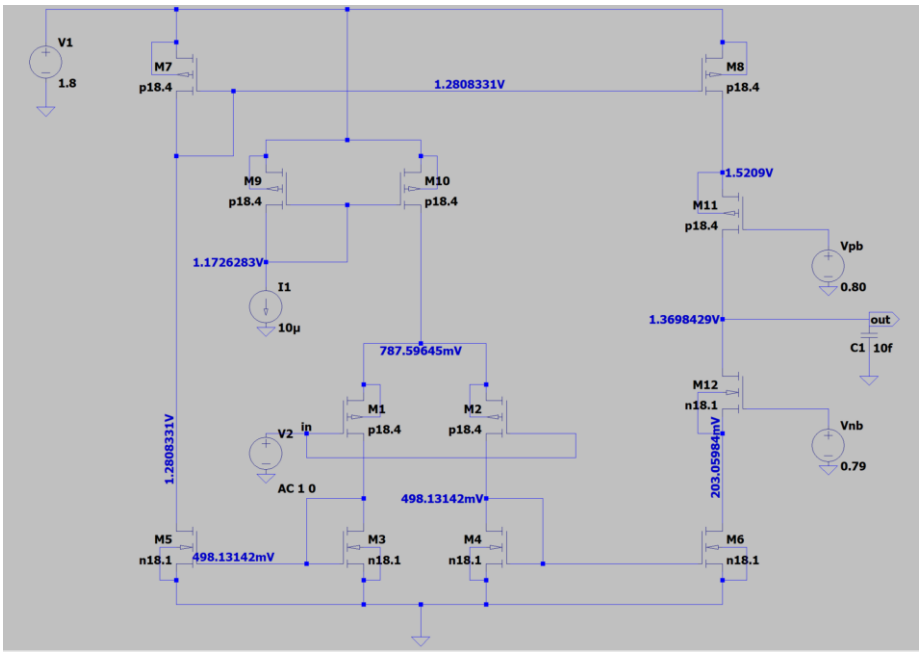


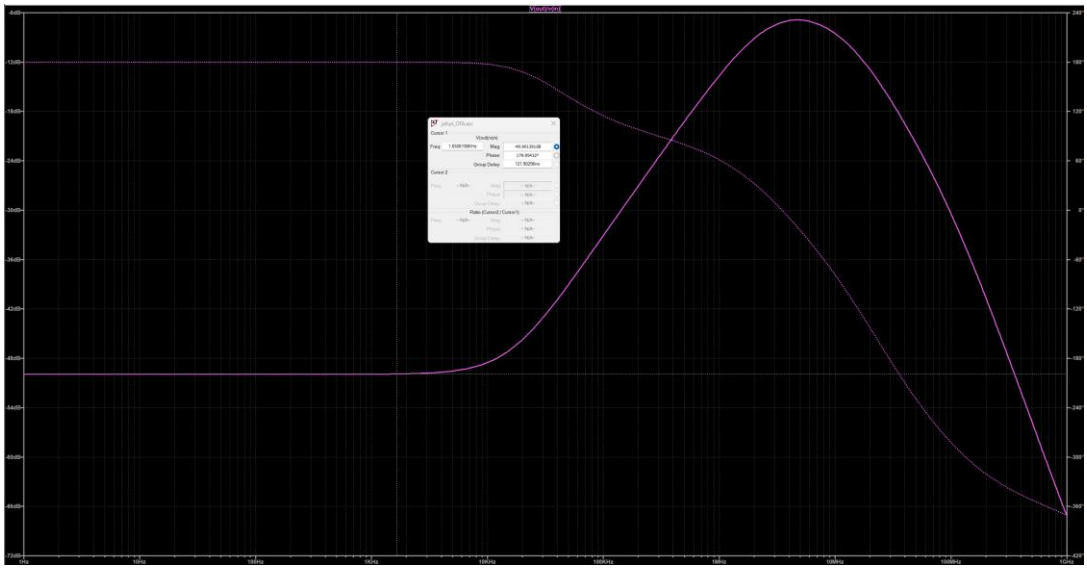
h. Noise



i. CMRR

The modified circuit for finding CMRR is as follows





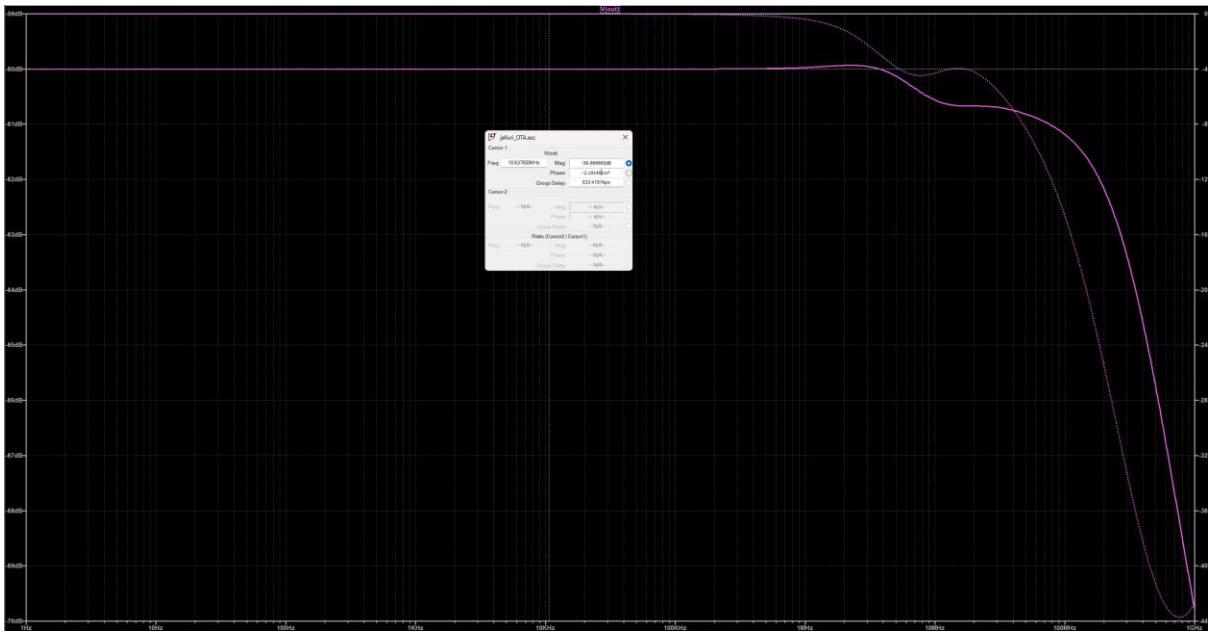
From the above obtained plot, we have

Common mode gain (Ac) = -49.9dB

Differential mode gain (Ad) = 53.18dB

Now, the Common Mode Rejection Ratio (CMRR) = Ad(dB)-Ac(dB) = 103.08dB

j. PSRR



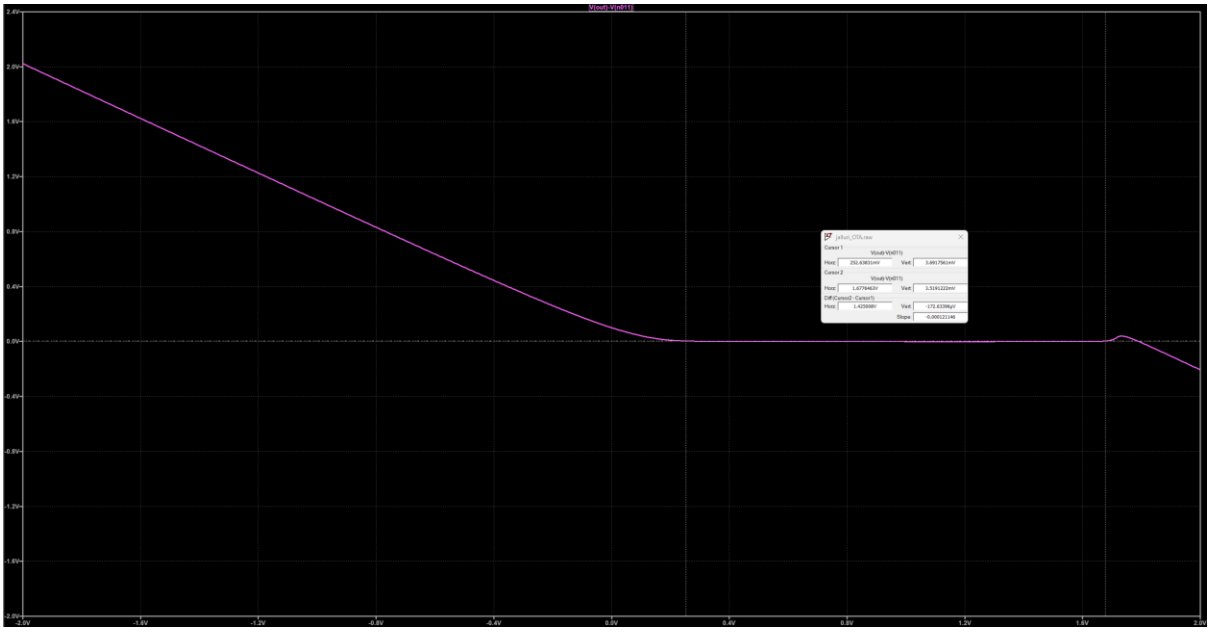
The obtained PSRR from the above figure is hence 53.18dB-(-59.99dB) = 113.18dB

k. ICMR

From the below graph the ICMR obtained after following the given steps is

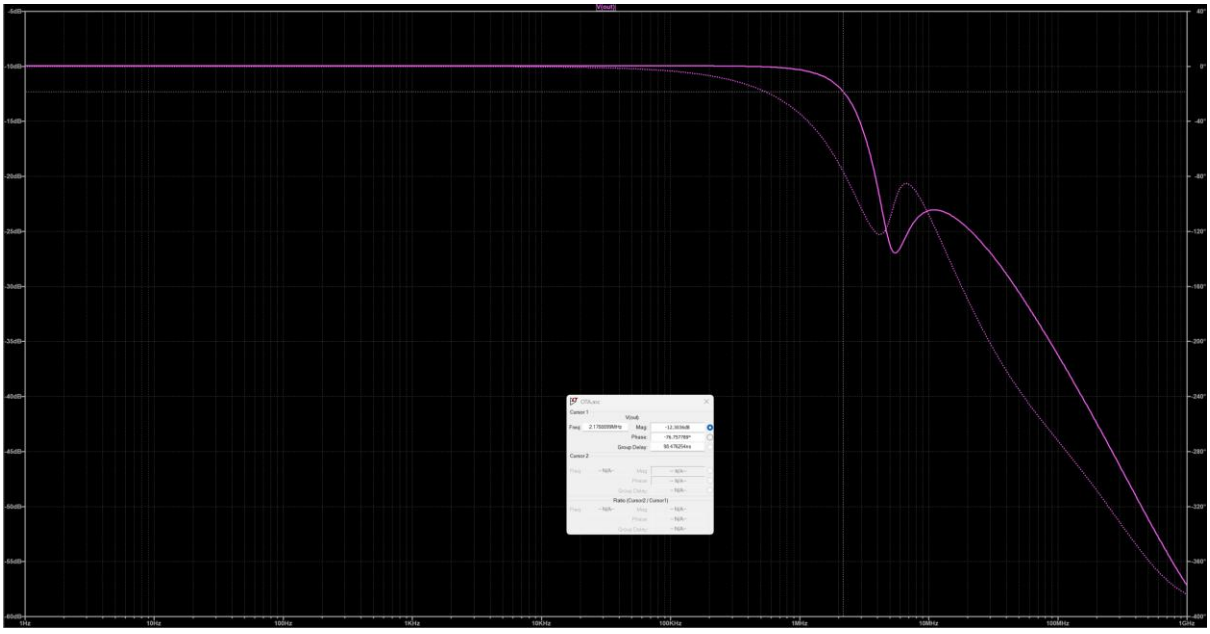
$$0.252\text{mV} < \text{ICMR} < 1.67\text{V}$$

So it has a range around 1.42V.



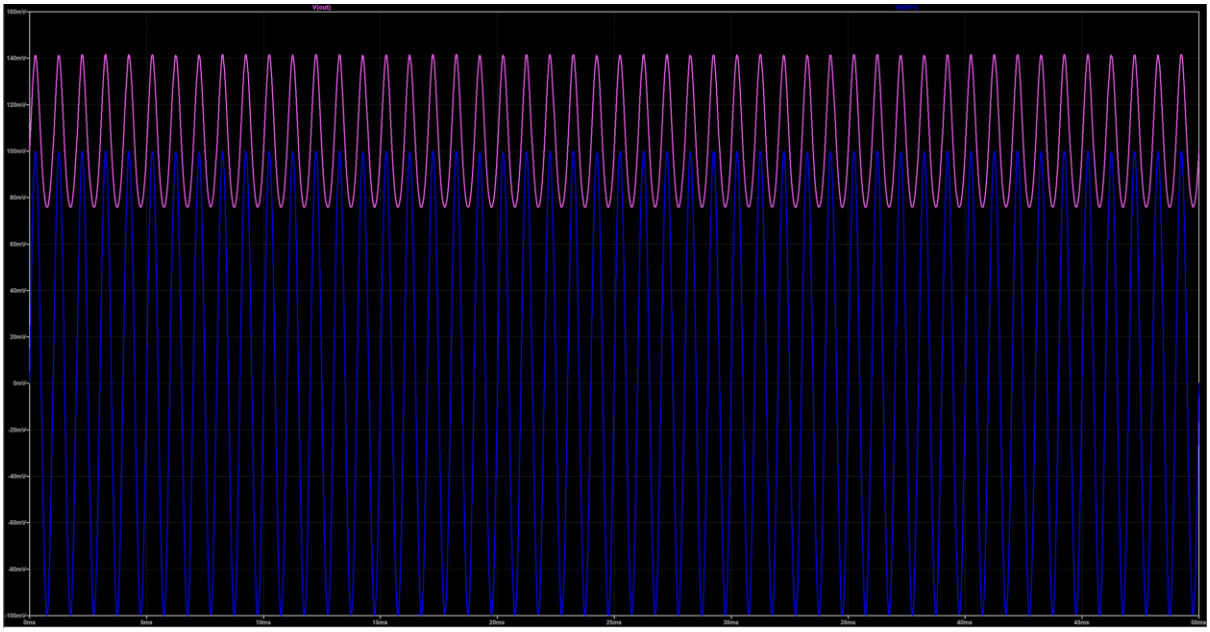
l. Closed Loop Gain

The -3dB bandwidth was observed around 2.1Mhz for the closed loop gain.



m. Closed Loop Transient Analysis

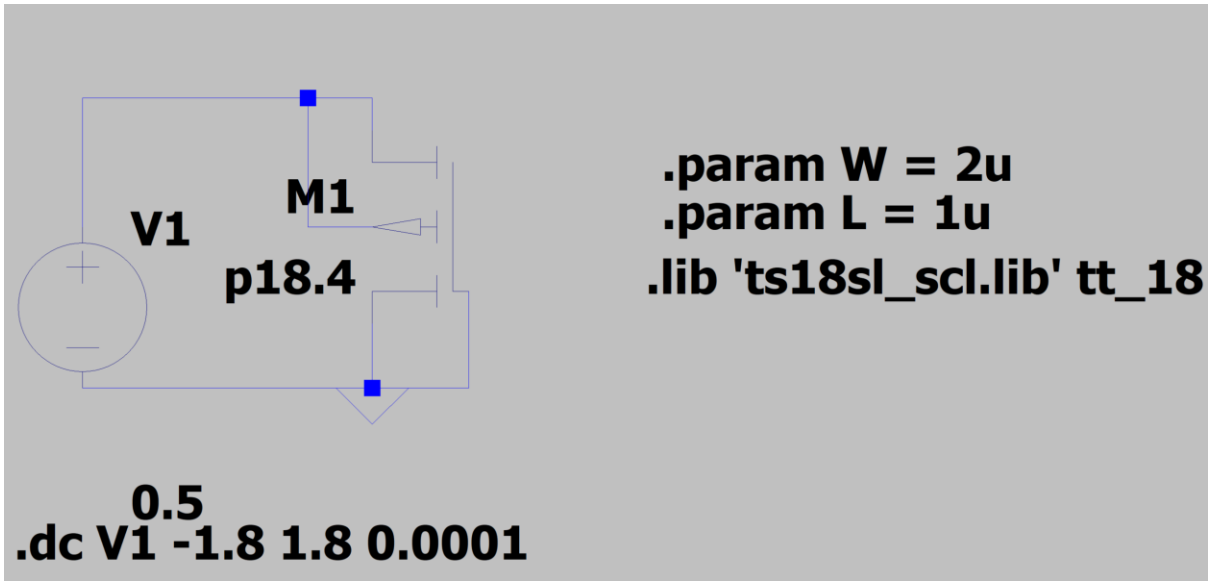
The closed loop transient analysis for input of around 100mV is as follows

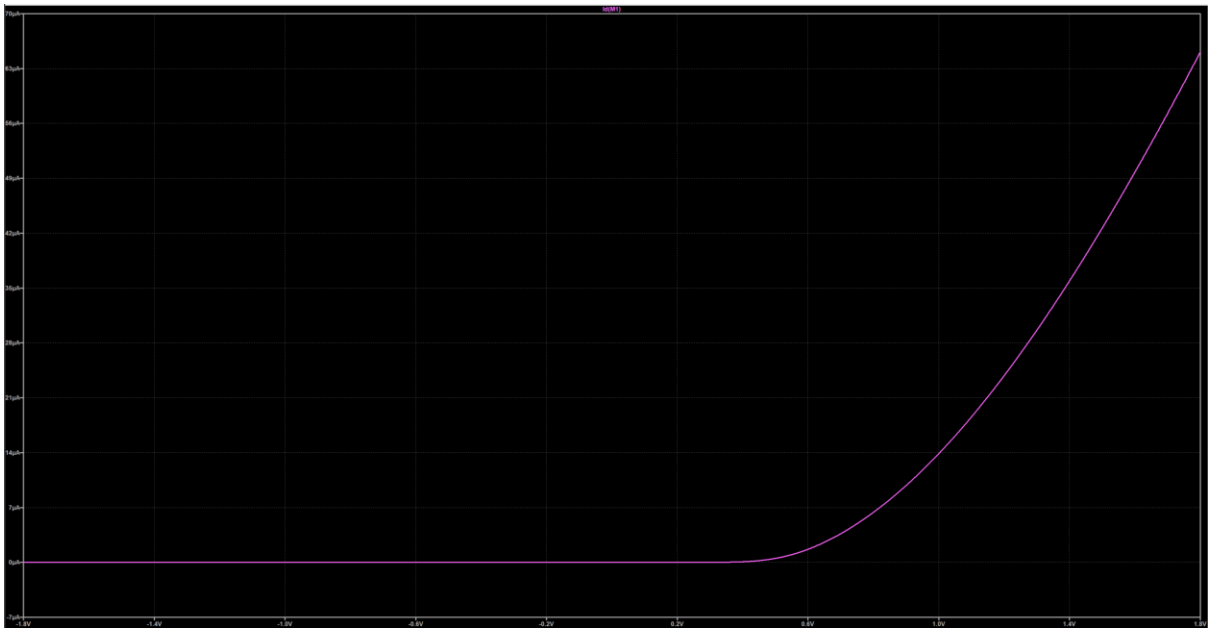


n. Power Consumption

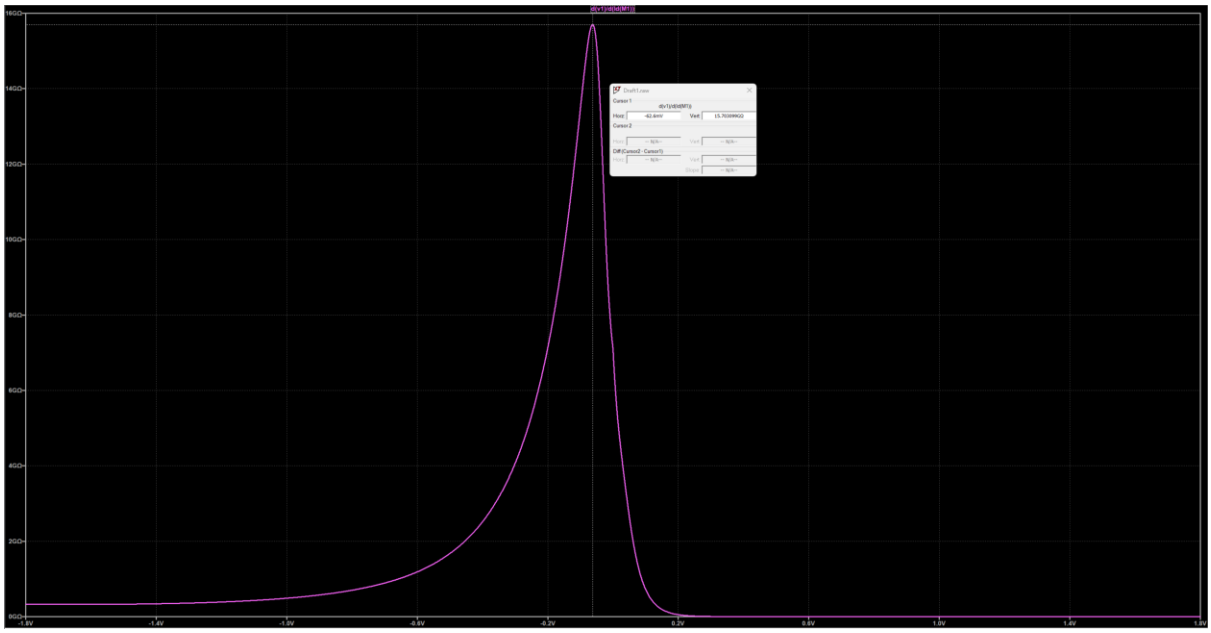
Total Current drawn from the source is 10+10+5+4 = 29µA, so the total DC power consumed is 1.8(VDD) times 29µA(I drawn), which is 52.2µW.

Pseudo Resistor is shown as follows



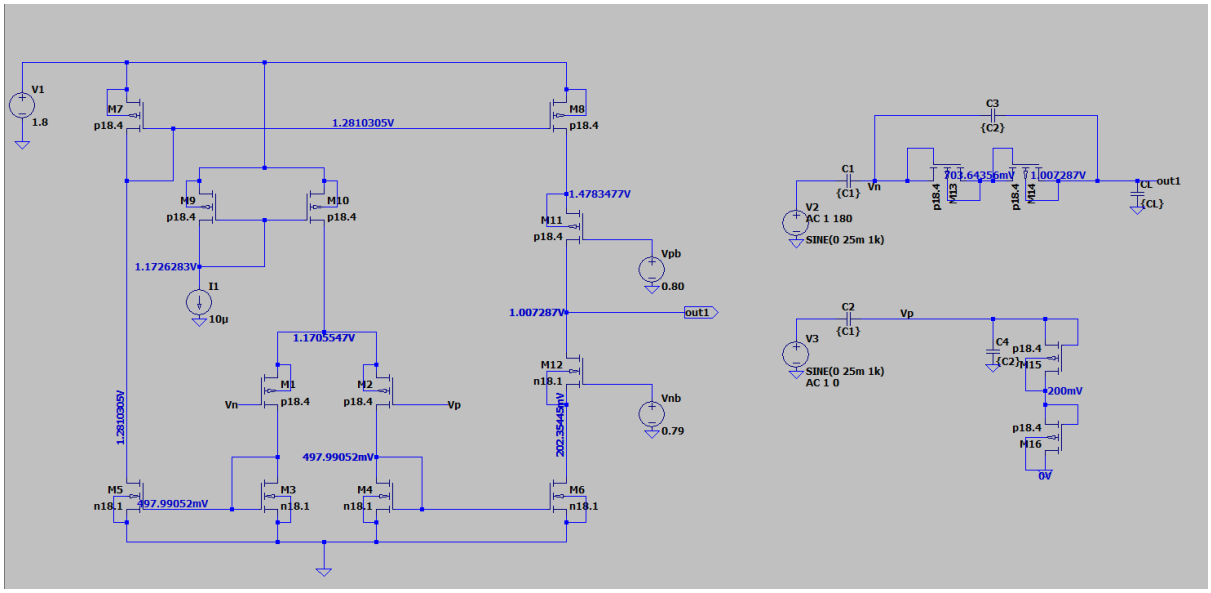


Above is the obtained I-V diagram for the pseudo-resistor. And the obtained incremental resistance vs incremental voltage is plotted below, from where we observe that the maximum incremental resistance is 15.7GΩ.



Neural Amplifier

The values of C1, C2 and the sizing of the pseudo resistor is taken from the reference paper which gives C1 as 0.2nF, C2 as 200fF and W/L to be 4u/4u. The values can also be calculated from the input and output resistances with the frequency to be less than the bandwidth at both input and output nodes. The final circuit is as follows.


V1
1.8
M7
p18.4
1.2810305V
M8
p18.4
M9
p18.4
M10
p18.4
1.1726283V
I1
10µ
1.4783477V
M11
p18.4
Vpb
0.80
1.007287V
out1
1.1705547V
M1
p18.4
Vn
M2
p18.4
Vp
M12
n18.1
Vnb
0.79
202.35445mV
497.99052mV
M5
n18.1
497.99052mV
M3
n18.1
M4
n18.1
M6
n18.1
C3
{C2}
C1
{C1}
Vn
V2
AC 1 180
SINE(0 25m 1k)
703.64356mV
1.007287V
CL
out1
{CL}
C2
{C1}
Vp
V3
SINE(0 25m 1k)
AC 1 0
C4
{C2}
p18.4
n15
200mV
p18.4
M16
0V

AC Response