RECONFIGURABLE 10T SRAM 2*2 ARRAY WITH EFFICIENT COMPUTE IN MEMORY (CIM)

MINI PROJECT SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF **BACHELOR OF ENGINEERING** IN **ELECTRONICS AND COMMUNICATION ENGINEERING** OF THE ANNA UNIVERSITY

ENGINEERING PROJECTS IN COMMUNITY SERVICE

DEC 2025

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ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

We oblige ourselves to the Almighty who has given us all the strengths and knowledge to complete this project work.

We wish to thank **Dr. K. MANONMANI, M.E., Ph.D.,** Principal, Government College of Technology, Coimbatore, for providing us the necessary facilities for completing this project work.

We express our heartiest thanks to **Dr. M. SANTHI, M.E., Ph.D.,** Professor and Head of the Department**,** Department of Electronics and Communication Engineering, Government College of Technology, Coimbatore, for providing us the valuable suggestions that were helpful in this project work.

We wish to enunciate our deep sense of gratitude and loyalty to our guide, **Dr. P. DEEPA**, **M.E., Ph.D.,** Associate Professor, Department of Electronics and Communication Engineering, Government College of Technology, Coimbatore for being the beacon of guidance in our project work and motivating us in every possible manner, which led to the successful completion of this project work.

We express our heartiest thanks to **Dr. S. MATHIVANNAN**, **M.E., Ph.D.,** Assistant Professor and Faculty Advisor, Department of Electronics and Communication, Government College of Technology, Coimbatore, for providing us the valuable suggestions.

We wish to express our thanks to our committee members, **Dr. G. SUCHITRA, M.E., Ph.D.,** Associate Professor Department of Electronics and Communication Engineering, Government College of Technology, Coimbatore and **Dr. G. THIRUGNANAM, M.E., Ph.D., Professor (CAS)**, Department of Electronics and Communication Engineering, Government College of Technology, Coimbatore for their ideas in improving this project work. Finally, we are grateful to our family members and our beloved friends for letting us know that they are always there to help us in hours of need.

ABSTRACT

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The increasing computational demands of modern data-centric applications—including artificial intelligence, machine learning, and edge computing—have underscored the limitations of conventional memory architectures, particularly the pronounced latency and energy inefficiency arising from frequent data movement between memory and processing units. In this context, compute-in-memory (CIM) architectures have gained prominence by enabling logic operations directly within memory arrays, effectively reducing the von Neumann bottleneck. This project presents the design, implementation, and detailed characterization of a 10-transistor (10T) SRAM cell specifically engineered for CIM applications, utilizing Cadence Virtuoso for schematic simulations.

The proposed 10T SRAM-CIM cell is developed to support integrated computation alongside standard data storage, leveraging its advanced structure to facilitate robust logic and arithmetic operations directly within the memory array. The work emphasizes minimizing data movement, thereby enhancing energy efficiency and computational throughput. A comprehensive analysis of both static and dynamic performance characteristics is undertaken, including metrics such as access time, static noise margin (SNM), and write trip point. These parameters are critical for evaluating the operational reliability, speed, and resilience of the SRAM cell, especially under varying load and environmental conditions essential for practical deployment.

Simulation results from Cadence Virtuoso validate the robustness of the proposed architecture, confirming its capability to deliver efficient in-memory computation without compromising data integrity or speed. The implementation demonstrates significant improvements in both latency and power consumption as compared to conventional memory designs. Ultimately, this project contributes to the evolving field of CIM technologies by providing a scalable, high-performance memory solution suitable for next-generation intelligent systems, establishing a foundation for further research in energy-efficient and high-speed architectures

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SRAM	-	STATIC RANDOM ACCESS MEMORY
CIM	-	COMPUTING-IN-MEMORY
MAC	-	MULTIPLY AND ACCUMULATE
NMOS	-	N-TYPE METAL OXIDE SEMICONDUCTOR
PMOS	-	P-TYPE METAL OXIDE SEMICONDUCTOR
RBL/RBLB	-	READ BIT LINE/READ BIT LINE BAR
BL/BLB	-	BIT LINE / BIT LINE BAR
WL/WWL	-	WORD LINE / WRITE WORD LINE
RWL	-	READ WORD LINE
CEN	-	COMPUTE ENABLE
SA	-	SENSE AMPLIFIER
SNM	-	STATIC NOISE MARGIN
RSNM	-	READ STATIC NOISE MARGIN
WSNM	-	WRITE STATIC NOISE MARGIN
VDD	-	SUPPLY VOLTAGE

INTRODUCTION

CHAPTER 1
INTRODUCTION

The exponential growth of artificial intelligence, machine learning, and edge computing applications has intensified the need for memory architectures that deliver both high performance and energy efficiency. Conventional von Neumann architectures face a fundamental bottleneck caused by the physical separation of computation and memory units, resulting in significant data transfer overhead, latency, and power dissipation. Compute-in-Memory (CIM) architectures address these challenges by performing computation directly within the memory array, thereby reducing data movement and enabling parallel processing.

Among the various CIM implementations, SRAM-based compute-in-memory arrays stand out for their compatibility with standard CMOS technology, high operational speed, and low-voltage functionality. By integrating additional peripheral circuits—such as mixed-signal or digital adder trees and specialized compute word lines—SRAM-based CIM systems can efficiently execute fundamental logic and multiply-accumulate (MAC) operations directly within the memory, an architectural enhancement that markedly improves computational throughput while minimizing system-level energy consumption.

This mini project focuses on the design, simulation, and performance analysis of a 10T SRAM-based compute-in-memory architecture. The study includes detailed evaluations of static noise margin (SNM), read access time, and functional integration in a CMOS environment, with the proposed design being implemented and validated using Cadence Virtuoso, following methodologies inspired by recent advancements and state-of-the-art research in CIM-SRAM technology.

1.1 OBJECTIVE

To design a 10T Compute-in-memory (CIM) based 2×2 SRAM array with reconfigurable architecture, focusing on enhanced read reliability and power efficiency for AI, ML, and edge computing applications.

1.2 MOTIVATION OF THE PROJECT

Modern AI and ML applications require executing millions of Multiply-Accumulate (MAC) operations, especially in neural network inference and edge-processing tasks. In conventional von Neumann systems, these operations cause significant power consumption because data has to travel back and forth between the memory and the processor. This constant data movement, known as the memory wall, limits both performance and energy efficiency.Compute-in-Memory (CIM) offers a promising solution by enabling computations to be performed directly within the memory array itself, thereby reducing data transfer overhead. Among various memory technologies, SRAM-based CIM stands out due to its high speed, stability, and compatibility with CMOS processes. A 10T SRAM cell further improves read stability, isolates internal nodes, and supports reliable computation without disturbing stored data.This motivated the development of a reconfigurable 10T SRAM 2×2 array, where both normal write operations and CIM operations can occur efficiently—even in parallel. Such a design directly addresses the challenges of power consumption and computation delay in traditional architectures. By enabling in-memory MAC operations with reduced energy and improved reliability, this architecture is highly suitable for low-power AI, ML, and edge computing applications that require fast and energy-efficient processing close to the sensor or device.

1.3 LITERATURE SURVEY

This study reviews 10T SRAM and Compute-in-Memory architectures emphasizing low power, stability, and performance improvements for modern embedded systems.

JOURNAL NAMES	AUTHORS	TITLE OF PAPER	CONCEPT	ADVANTAGES	DIS ADVANTAGES
IEEE Journal of Solid-State Circuits [17]	Shanshan Xie, Siddhartha Raman Sundara Raman, Can Ni, Meizhi Wang, Mengtian Yang, and Jaydeep P. Kulkarni	A Reconfigurable 10T SRAM and Scalable Compute Within Memory	The paper proposes Ising-CIM, a compute-in-memory (CIM) architecture that performs analog design using computations within memory arrays to solve combinatorial optimization problems (COPs) efficiently.	Eliminates off-chip data movement → low power and high speed. - Area-efficient (6×–17× smaller spin area than prior Ising accelerators).	Analog computations are susceptible to process, voltage, and temperature (PVT) variations. - Requires careful calibration of reference voltages (VREF).
IEEE Journal paper of Micromachine (2023) [1]	C. Liu, H. Liu, J. Yang	A Novel Low-Power and Soft Error Recovery 10T SRAM Cell	Proposes PP10T cell with built – in error recovery and low leakage	High soft-error tolerance, low power , improved, read stability.	Larger area due to extra transistors and feedback path , slightly lower write speed
IEEE Journal paper of Sensors (2021) [6]	M. -H. Sheu et al.	A 0.3-V PNN-Based 10T SRAM with Pulse Control.	Uses pulse-controlled bitlines and near-threshold assist techniques for reliable 10T SRAM operation at	Reliable read/write at 0.3 V, very low static power, compatible with ultra-low-power systems.	Requires complex pulse timing circuitry; not ideal for high-speed memory systems.

			ultra-low voltage		
Integration, The VLSI Journal (2018) [7]	M. Limachia, R. Thakker, N. Kothari	Near-Threshold 10T Differential SRAM for FinFET Technology	FinFET-compatible differential 10T SRAM for high stability in near-threshold operation.	Focus on balancing leakage and speed. High read/write noise margins, excellent process variation tolerance, scalable to FinFET nodes.	Slightly higher leakage at nominal voltages; area penalty vs. 6T cells.
World Scientific Journal (2021) [8]	R. Manoj Kumar	Bit-Interleaved Low-Power 10T SRAM with Improved Read Stability	Bit-interleaving reduces coupling noise; stacked devices and isolated read ports enhance RSNM.	Improved read reliability and leakage control; simple structure; lower dynamic power.	Slight delay in write operation; increased design complexity at large scales.
IEEE Journal Paper of Sensors (2022) [15]	M.B.G. Sulaiman et al.	SRAM-Based CIM Architecture Design for Event Detection	Proposes SRAM-CIM for energy-efficient real-time event detection in IoT sensor nodes.	Reduces off-chip data transfer; high energy efficiency and latency improvement.	Limited to small data sets; scaling to high-bitwidth operations is challenging.

Analog Integrated Circuits and Signal Processing (Springer, 2024) [16]	J.A. Díaz-Madrid et al.	Energy-Efficient SRAM with Mixed-Signal In-Memory Convolution Architecture	Implements current-mode mixed-signal CIM for convolutional operations in image processing.	High throughput, real-time processing, energy-efficient mixed-signal computing.	Sensitive to analog mismatch and noise; higher design complexity.
Journal of Systems Architecture (2021) [14]	S. Mittal, G. Verma, B.K. Kaushik	Review on SRAM-Based Computing-in-Memory: Circuits and Application	Review of SRAM-CIM circuit-level and system-level implement comparison of digital vs. analog approaches.	Comprehensive summary of CIM circuit architectures; useful for design trade-off analysis	No experimental results; lacks specific focus on 10T layouts.

1.4 INFERENCE

Several significant conclusions can be drawn from the analysis of the proposed CIM SRAM design when compared to the base paper. The results indicate remarkable improvements in key performance parameters, particularly in access time and noise margin metrics.

- Drastic improvement in read access time:
  The proposed design achieves an exceptionally low read access time of 42 ps, compared to 1.33 ns in the base paper—demonstrating over a 30× speed enhancement. This ultra-fast read capability is vital for high-performance memory architectures and compute-in-memory (CIM) operations where rapid data retrieval is crucial.

- Slight trade-off in write access time, yet robust performance:
  While the write access time of 5 ns is marginally higher than the base paper's 3.6 ns, it remains within a practical range. The increase is compensated by the significantly improved noise margins, ensuring stable and dependable memory operation even under varying process and voltage conditions.

- Enhanced noise margins ensuring stability:
  The substantial improvement in read, write, and hold Static Noise Margins (SNM) highlights the robustness of the proposed design. This ensures higher resilience against disturbances, improving overall reliability for in-memory computing and AI accelerator systems.

The proposed CIM SRAM design thus establishes itself as a highly stable, fast, and energy-efficient memory solution suitable for next-generation compute-in-memory and AI hardware accelerators. The combined gains in access time and noise margin underline its potential to enable faster, more reliable, and error-resilient on-chip computation, marking a notable advancement over conventional SRAM architectures.

1.5 REPORT ORGANISATION

The remainder of this report is structured into five chapters, each focusing on a significant aspect of the project workflow.

CHAPTER 1: INTRODUCTION

This chapter introduces the motivation, objectives, and detailed literacy survey of our project.

CHAPTER 2: PROPOSED RECONFIGURABLE 10T COMPUTE-IN-MEMORY SRAM ARCHITECTURE

In this chapter reviews conventional 6T SRAM designs, explaining their operational principles and key limitations-including read disturbance, poor noise margins and lack of compute functionality-when applied to CIM tasks. It also discusses the base paper's 10T SRAM architecture, highlighting both its improvements over 6T and its remaining challenges in stability, power, and read performance.

CHAPTER 3: RESULTS AND DISCUSSIONS

It presents the simulation methodology, toolchain, and system specifications used for validating the detailed simulation results for both the single cell and 2*2 array, highlighting the read, write, hold, and compute functionality as well as comparative performance metrics.

CHAPTER 4: CONCLUSION AND FUTURE SCOPE

The final chapter presents the overall conclusions drawn from the simulation results and highlights the future scope of the proposed CIM-based 10T SRAM design, It outlines the key contributions and potential enhancements for advanced memory centric computing applications

PROPOSED RECONFIGURABLE 10T SRAM-CIM ARCHITECTURE

CHAPTER 2
PROPOSED RECONFIGURABLE 10T COMPUTE-IN-MEMORY SRAM ARCHITECTURE

2.1 6T SRAM DESIGN

The 6T SRAM cell, as shown in Figure 2.1[8], consists of two cross-coupled inverters forming a bistable latch and two access transistors used for read and write operations. This structure offers compact area, low power consumption, and high-speed performance, making it widely adopted in standard memory architectures. However, the 6T cell is not suitable for Compute-in-Memory (CIM) applications because the read and write operations share the same bit lines, which can cause read disturbance and may lead to data corruption during computation. Furthermore, the 6T SRAM lacks dedicated read or compute ports, preventing the execution of analog-domain operations such as charge sharing or current accumulation. Therefore, although efficient for storage, the 6T SRAM cannot directly support CIM functionality.

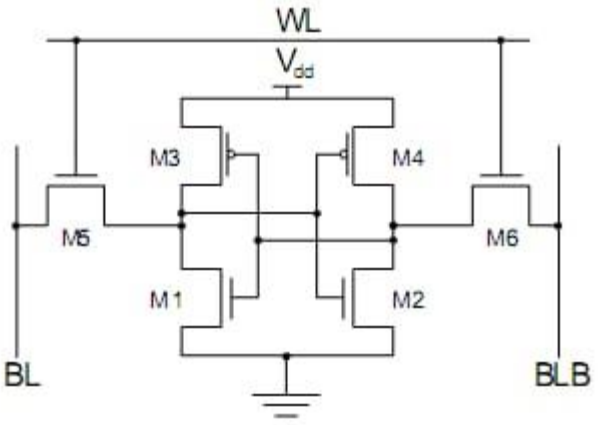

FIGURE 2.1 NORMAL 6T SRAM

2.2 PROBLEMS IN CONVENTIONAL 6T SRAM

The problems in conventional SRAM is discussed below from the upcoming sections.

2.2.1 SHARED READ AND WRITE BITLINES

- In a 6T SRAM cell, the same pair of bitlines is used for both read and write operations.
- This shared path can cause read disturbance, where the voltage division on the bitlines during a read operation may unintentionally flip the stored data.
- Hence, data integrity is not guaranteed when both operations occur under low-voltage or compute conditions.

2.2.2 LIMITED READ STABILITY

- During a read operation, one of the internal storage nodes is directly connected to the bitlines through the access transistor.
- This connection reduces the Read Static Noise Margin (Read SNM) and makes the cell highly sensitive to supply voltage fluctuations and process variations.
- As a result, the 6T SRAM cell becomes less reliable for stable data retention during read operations.

2.2.3 ABSENCE OF DEDICATED COMPUTE PATH

- The 6T SRAM architecture is optimized purely for storage and lacks any dedicated circuitry for computation.
- Because there are no separate transistors or ports for analog-domain operations, the cell cannot perform charge-sharing or multiply-accumulate (MAC) functions required for CIM applications.

2.2.4 READ-WRITE TRADE-OFF

- In the 6T SRAM design, the transistor sizing strongly affects both read and write operations.
- Enhancing the write ability by increasing the access transistor size often reduces the read stability, and improving the read margin can make the cell harder to write.
- This read–write trade-off limits performance optimization and design flexibility.

2.2.5 INCOMPATIBILITY WITH COMPUTE-IN-MEMORY(CIM) OPERATIONS

- Since the 6T SRAM shares the same bitlines for both storage and access, it cannot isolate internal nodes during computation.
- This prevents stable analog accumulation and parallel in-memory processing.

Therefore, modified SRAM structures such as 8T or 10T SRAM cells are preferred for CIM-based architectures, as they provide separate read and compute ports for improved stability and functionality.

2.3 EXISTING 10T SRAM-BASED CIM DESIGN

The 10T SRAM cell, shown in Figure 2.2, is adopted from the base paper used in this work [17].

This design adds four additional transistors to the conventional 6T cell to provide a decoupled read path, improving read stability and reducing the possibility of read disturbance. The separate read port allows data to be accessed without directly affecting the internal storage nodes, making it partially suitable for CIM operations such as charge sharing and logic computation.

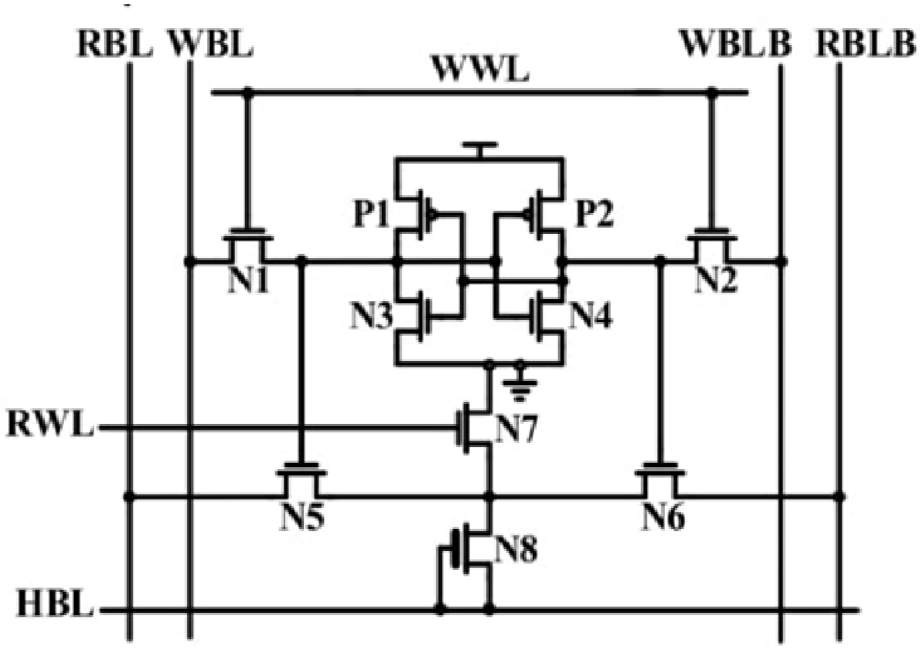

FIGURE 2.2 EXISTING 10T SRAM CIM

However, the base paper design exhibits several performance limitations,

Which are discussed below.

2.3.1 LOW READ STATIC NOISE MARGIN (READ SNM)

- The diode-connected configuration used in the read access path weakens the voltage levels at the storage nodes during read operation.
- This results in a low Read SNM, reducing the stability of the cell and increasing the possibility of read disturbance, especially at lower supply voltages.

2.3.2 LOW HOLD STATIC NOISE MARGIN (HOLD SNM)

- The internal node voltage in the base design is sensitive to leakage and process variations due to the stacked transistor arrangement.
- This leads to a low Hold SNM, which affects the cell's ability to retain data reliably during standby or hold conditions.

2.3.3 INCREASED POWER CONSUMPTION

- The diode-connected read access transistors cause continuous current flow during read operation, leading to higher static power dissipation.
- This increases the overall energy consumption of the memory array, making it less efficient for low-power applications.

2.3.4 INCREASED READ ACCESS TIME

- The read discharge path contains multiple series-connected transistors, which increases the effective resistance of the read path.
- As a result, the bitline discharge becomes slower, causing a higher read access time and reduced read speed compared to conventional designs.

2.4 PROPOSED 10T SRAM-BASED CIM DESIGN

The proposed 10T SRAM design, as shown in Figure 2.3, improves upon the existing CIM-enabled cell by incorporating high-threshold NMOS transistors for in-

memory logical AND operations, which reduces leakage and enhances computation reliability.The design also features fully decoupled read and write paths, minimizing read disturbance and improving data stability. These enhancements lead to higher Read and Hold SNM, lower power consumption, and faster read access, making the proposed 10T SRAM cell more efficient and well-suited for CIM applications.

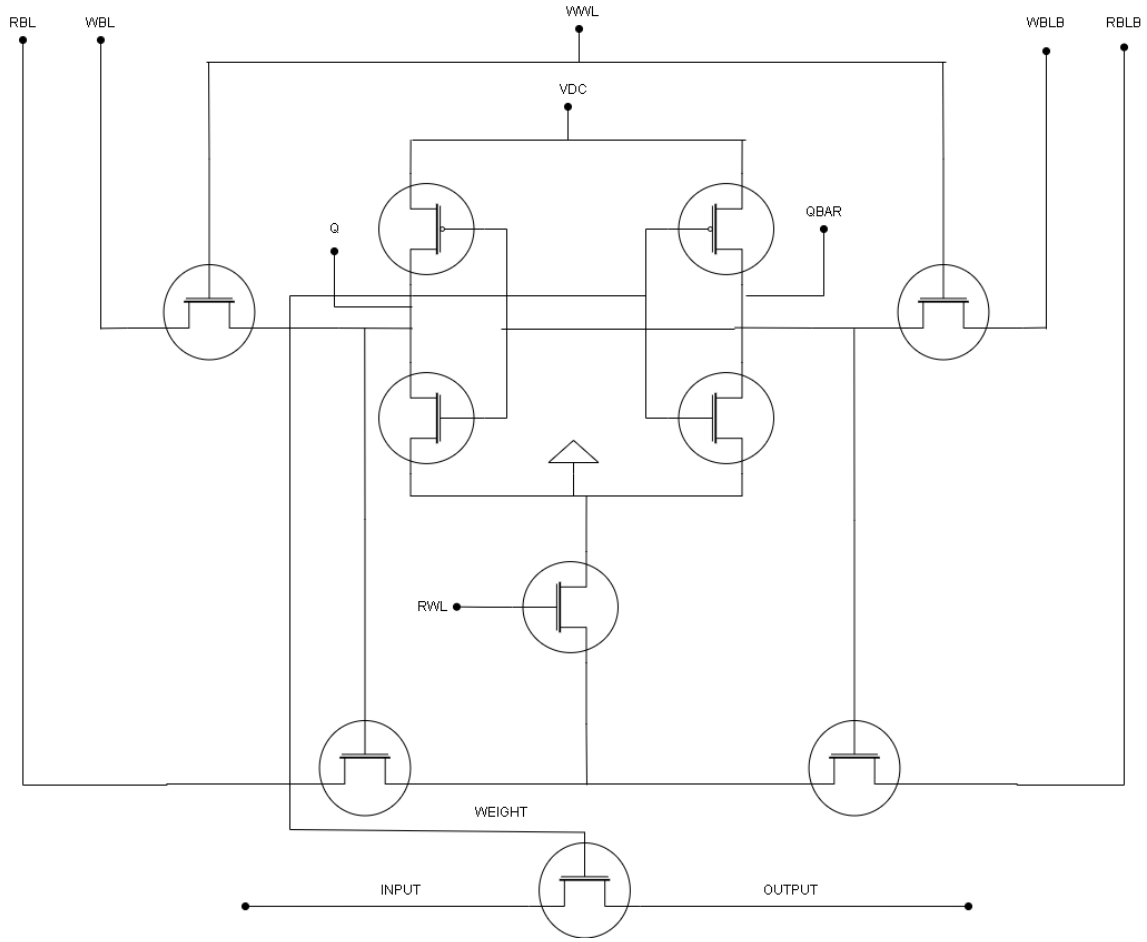

FIGURE 2.3 PROPOSED 10T SRAM CIM

2.4.1 WRITE OPERATION

To perform the write operation, when WWL = 1, the data from the write driver circuit is written into the SRAM through WBL and WBLB. At this time, RWL = 0, allowing the data to be safely stored in the internal node Q. Since the read and write paths are decoupled, RBL and RBLB are precharged during the write operation for the subsequent read cycle.

2.4.2 WRITE DRIVER CIRCUIT

During the write operation, when EN = 1, the write driver becomes active, and the input data is applied to its output. The outputs of the write driver, BL and BLB, are connected to the WBL and WBLB lines of the SRAM cell, allowing the data to be written into the internal nodes. This ensures that the correct data is stored in the SRAM whenever the write driver is enabled as shown in Figure 2.4.This circuit was referred in paper [2].

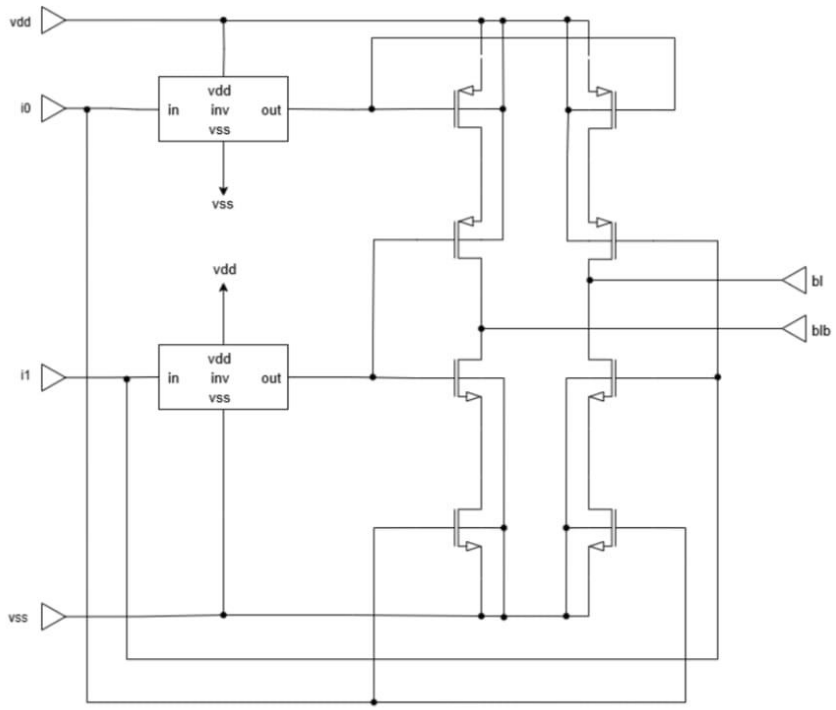

FIGURE 2.4 WRITE DRIVER CIRCUIT

2.4.3 READ OPERATION

To perform the read operation, the RBL and RBLB lines are already precharged from the previous write cycle. When RWL = 1 and WWL = 0, the data stored in the SRAM cell is transferred to the bitlines. The sense amplifier then detects this data, as the isolation signal is set to 1 and the sense amplifier enable signal is high, allowing the stored value to be accurately read from the SRAM.

2.4.4 PRECHARGE CIRCUIT

The precharge circuit initializes the bitlines (RBL and RBLB) to a known voltage level, typically VDD, ensuring reliable read operations. In the proposed 10T SRAM design, precharging is performed while the write and read paths are decoupled, so the bitlines are ready for the subsequent read cycle, reducing read delay and improving the sense amplifier's accuracy as shown in Figure 2.5 [5].

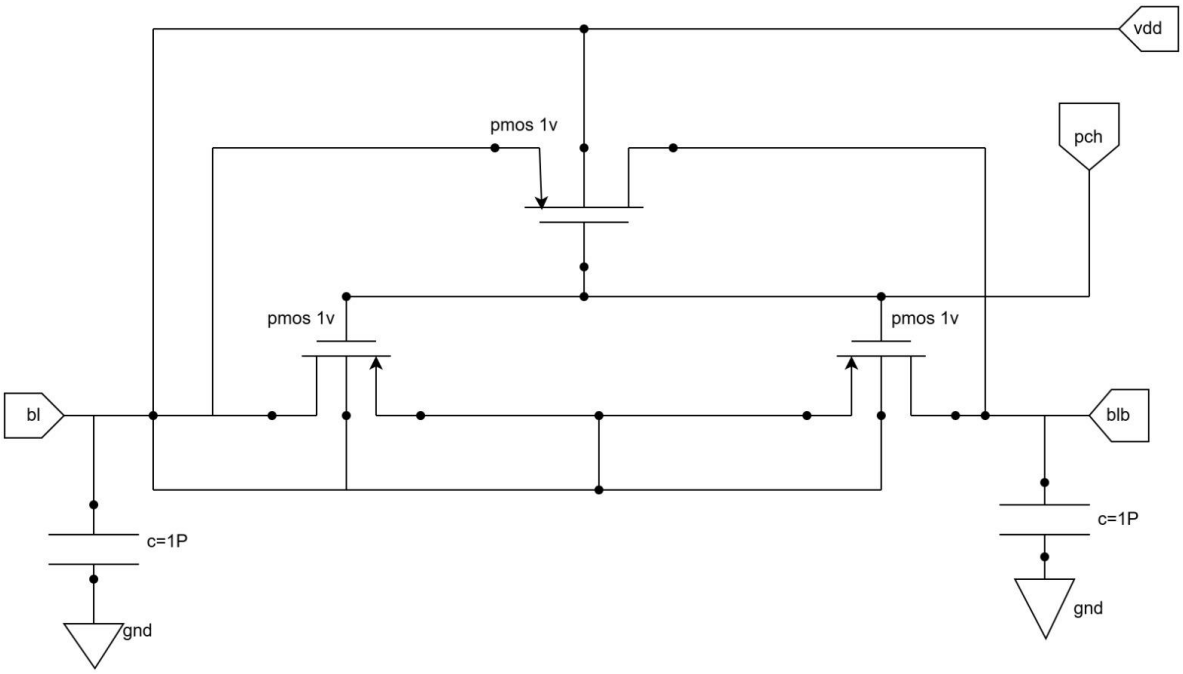

FIGURE 2.5 PRECHARGE CIRCUIT

2.4.5 ISOLATION CIRCUIT

The isolation circuit in the proposed 10T SRAM design controls the connection between the read bitlines (RBL/RBLB) and the sense amplifier. When a read operation is performed (RWL = 1 and ISO = 1), the sense amplifier is connected to the bitlines to detect the stored data. During write or idle periods, the isolation signal (ISO = 0) disconnects the sense amplifier, preventing any interference with the stored data and ensuring accurate sensing while reducing unnecessary power consumption as shown in Figure 2.6 [4].

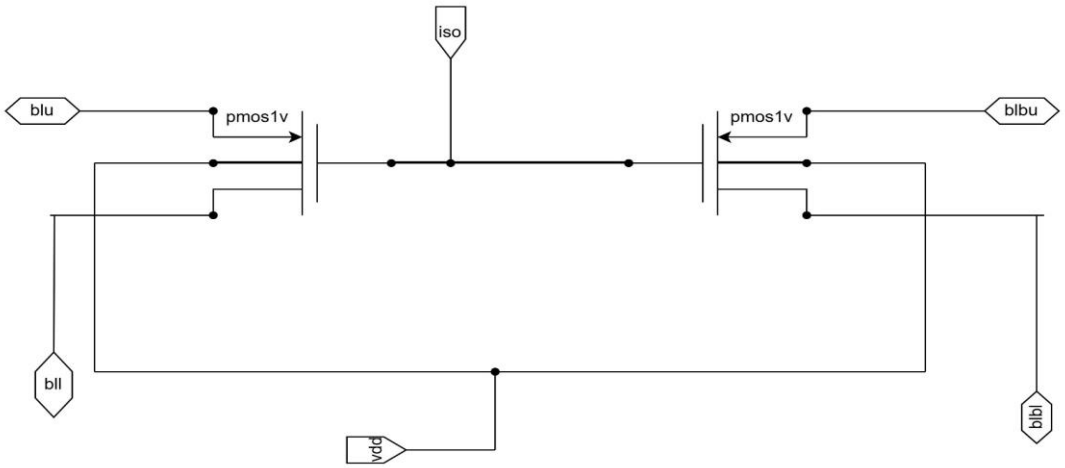

FIGURE 2.6 ISOLATION CIRCUIT

2.4.6 SENSE AMPLIFIER

The sense amplifier in the proposed 10T SRAM design is used to detect and amplify the small voltage difference on the read bitlines (RBL/RBLB) during a read operation. When RWL = 1 and ISO = 1, the stored data is transferred to the bitlines, and the sense amplifier quickly amplifies this differential signal to full logic levels, providing a reliable output. By accurately sensing the stored data, the sense amplifier ensures fast and stable read operation while minimizing read disturbance to the SRAM cell as shown in Figure 2.7 [3].

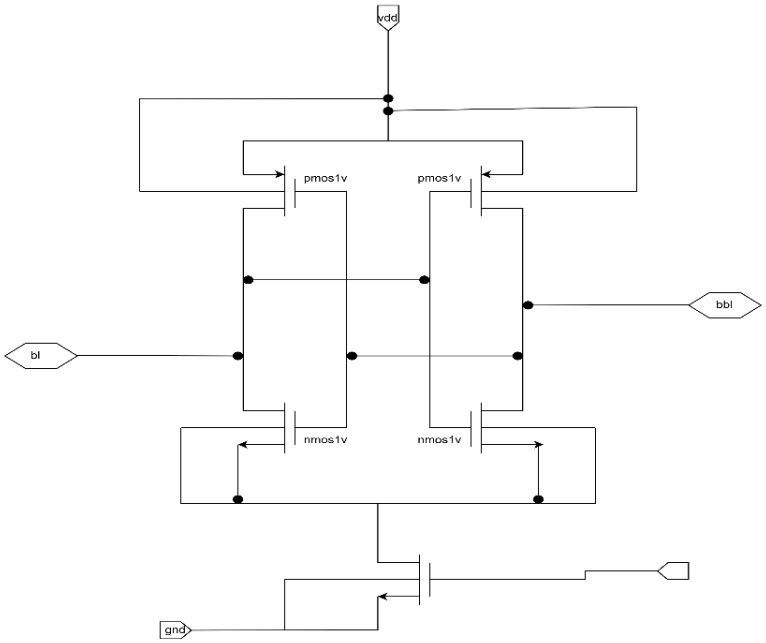

FIGURE 2.7 SENSE AMPLIFIER

2.4.7 HOLD OPERATION

In the hold operation, both the write wordline (WWL) and read wordline (RWL) are kept low, ensuring that the SRAM cell is completely isolated from both the write and read bitlines. During this state, no external signals affect the internal storage nodes, and the cross-coupled inverter pair maintains the stored logic value through positive feedback.

As a result, the data remains stable and preserved within the cell without any power dissipation due to switching activity. This condition ensures reliable data retention until the next read or write operation is initiated.

2.4.8 CIM OPERATION

In the proposed 10T SRAM, CIM functionality is achieved using a dedicated compute port controlled by an active signal. When the active signal is enabled, the data stored in the SRAM cell (representing the weight) is combined with the active data through a logical AND operation using a high-threshold compute NMOS transistor. The resulting CIM output is generated at the output node, enabling efficient in-memory computation without the need for separate processing circuitry.

2.5 COMPLETE 10T SRAM ARCHITECTURE

The proposed 10T SRAM architecture is integrated with essential peripheral circuits such as the write driver, precharge circuit, isolation circuit, and sense amplifier, as shown in Figure 2.8.

These peripherals play a vital role in ensuring reliable read and write operations. The write driver delivers data to the SRAM cell during write mode, while the precharge circuit initializes the read bitlines before every read cycle. The isolation circuit controls the connection between the read bitlines and the sense amplifier, preventing unwanted disturbances.

The sense amplifier detects and amplifies the small voltage difference on the read bitlines to generate a full-swing logic output. Together, these circuits enable stable, low-power, and high-speed operation of the proposed 10T SRAM cell, making it suitable for Compute-in-Memory applications.

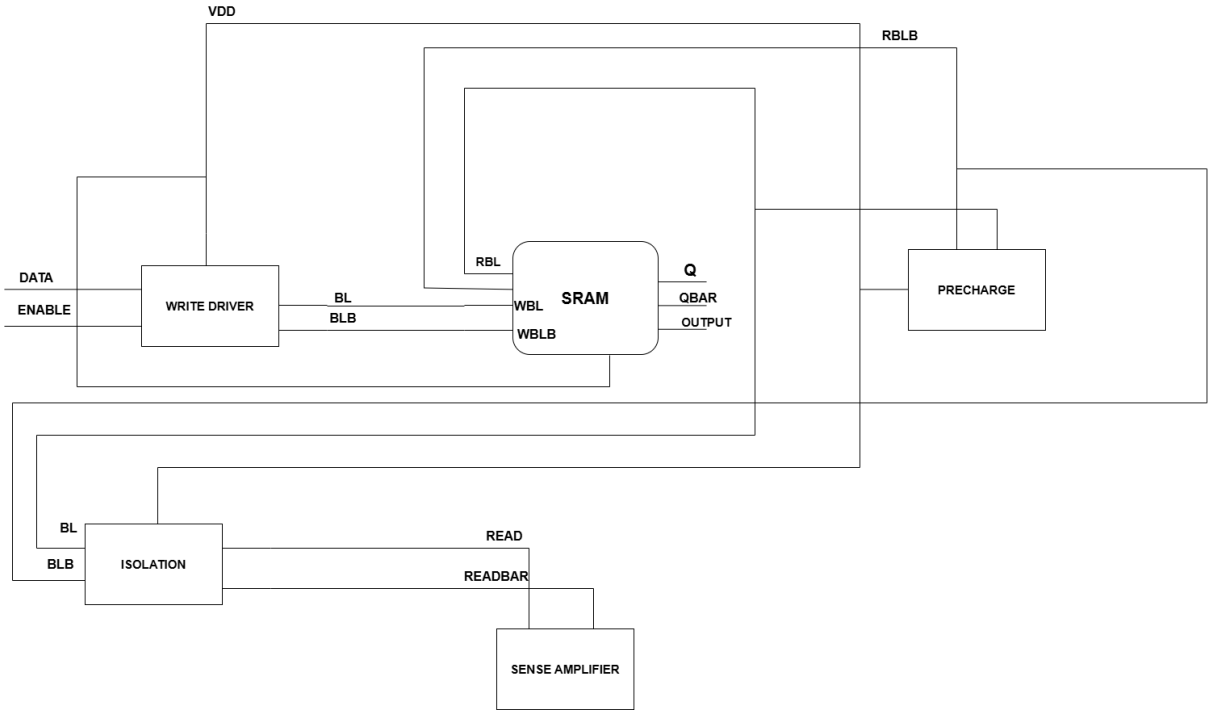

FIGURE 2.8 10T SRAM CIM ARCHITECTURE

2.5.1 DECODER CIRCUIT

As shown in fig 2.9, The decoder circuit is used to select the appropriate wordline in the 2×2 SRAM array during read and write operations. In this design, the same row decoder is shared for both read and write operations, controlled by a single control logic signal. When the control logic = 0, the write operation is enabled, and when the control logic = 1, the read operation is performed.

The decoder produces four outputs — D0, D1, D2, and D3. The outputs D0 and D1 are connected to the write wordlines (WWL1 and WWL2) of the first and second rows, respectively, while D2 and D3 are connected to the read wordlines (RWL1 and RWL2) of the corresponding rows.

When a particular WWL (for example, WWL1) is selected, both SRAM cells in that row are accessed, and data is written simultaneously through their respective bitlines. Based on the decoder output and the control signal, either a read or write operation is performed on the selected row of the SRAM array.

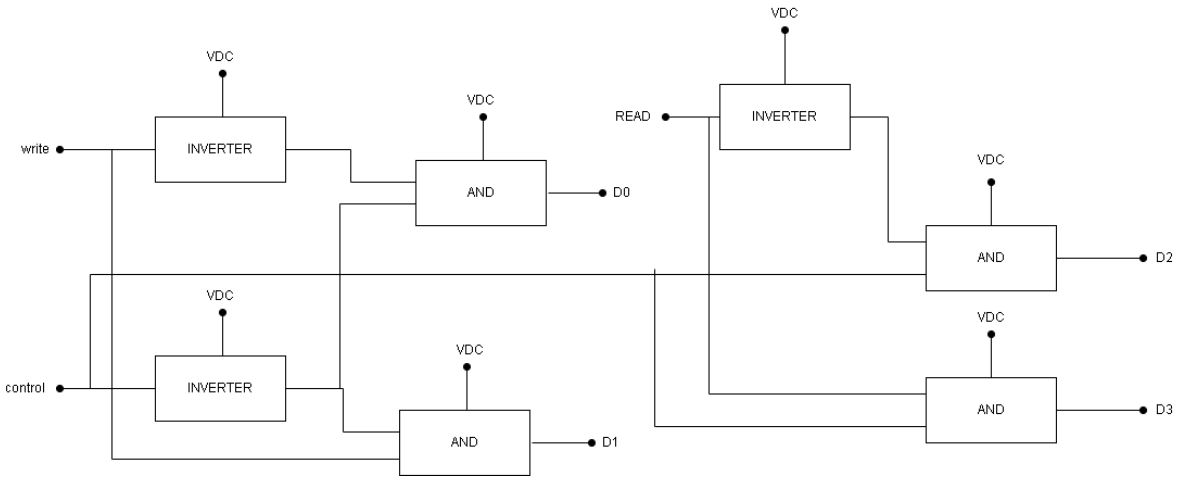

FIGURE 2.9 DECODER CIRCUIT

2.5.2 2*2 CIM-BASED SRAM ARRAY

As shown in fig 2.10, The proposed 2×2 SRAM array integrates peripheral circuits such as the write driver, precharge, isolation, and sense amplifier column-wise, with two columns connected to perform read, write, hold, and CIM operations. When WWL1 is selected, it connects to the write access transistors of both SRAM cells in the first row.

During the write operation, when the enable signal is high, data from the write driver circuit is written into the SRAM cells.

For CIM operation, when the active signal is applied through the active port of the SRAM, the stored weight (Q) within the cell is logically ANDed with the active data, and the resulting CIM output is produced at the output pin, enabling complete row-wise computation within memory.

The same process occurs for the second row when WWL2 is selected. During the read operation, the read wordline (RWL) is activated while the write wordline (WWL) remains low, allowing the sense amplifier to detect and amplify the stored data from the read bitlines. When WWL = 0, the SRAM retains its previously stored data, thereby performing the hold operation.

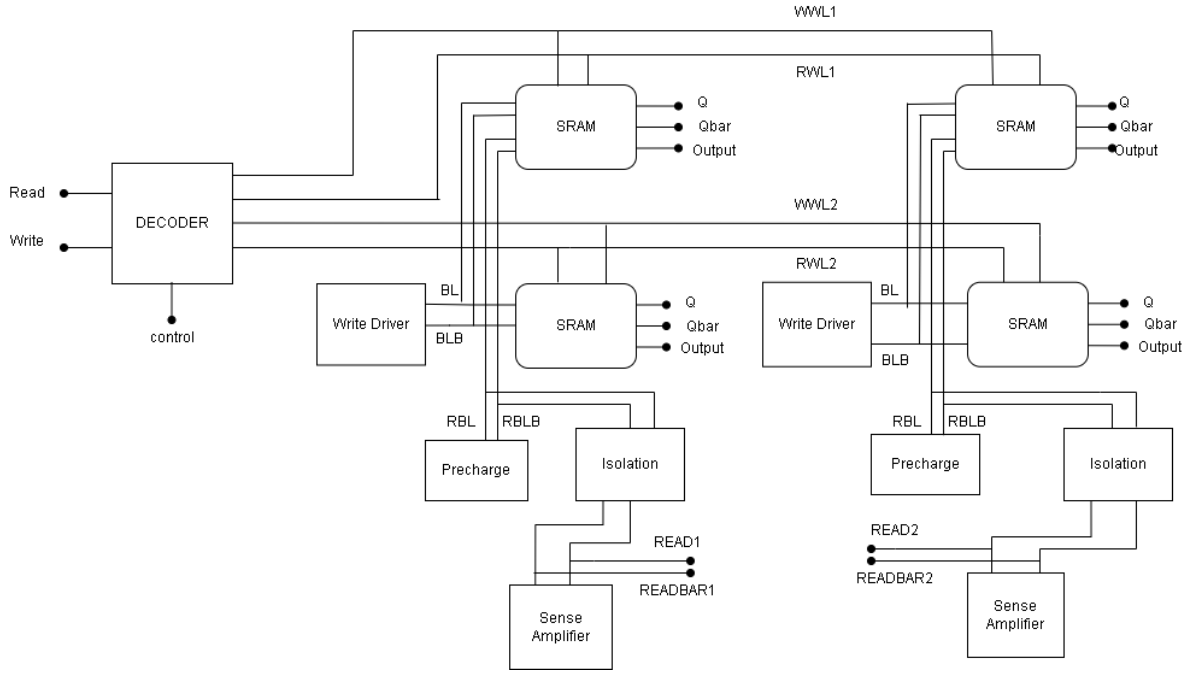

FIGURE 2.10 2*2 10T SRAM CIM ARRAY

RESULTS AND DISCUSSIONS

CHAPTER 3
RESULTS AND DISCUSSIONS

This chapter discuss the result of the proposed CIM based 10T SRAM.

TOOL: Cadence Virtuoso 90nm technology.

PROCESSOR: intel 3 core.

INSTALLED RAM: 8.00GB.

SYSTEM TYPE: 64-bit operating system, X64 based processor.

3.1 SIMULATION OF 10T SRAM CIM CELL

The simulation has been performed for 10T SRAM CIM cell using cadence virtuoso of 90 nm technology.

3.1.1 SIMULATION OUTPUT

The simulation results of the single 10T SRAM cell validate correct read, write, and CIM functionality. The cell reliably stores and retrieves data without disturbance, and the CIM mode accurately performs the AND operation, confirming the compute capability and stability of the proposed design.

From the figure 3.1, When the Write Word Line is activated (WWL = 1), the write driver enable signal goes high. The input data (logic 1 in this case) is driven through the write driver and stored in the SRAM cell at node Q.When WWL is deasserted (WWL = 0) and the Read Word Line is activated (RWL = 1), the previously stored data (logic 1) is accessed. The sense amplifier reads the voltage on the Read Bit Line (RB) and retrieves the stored value from the cell.

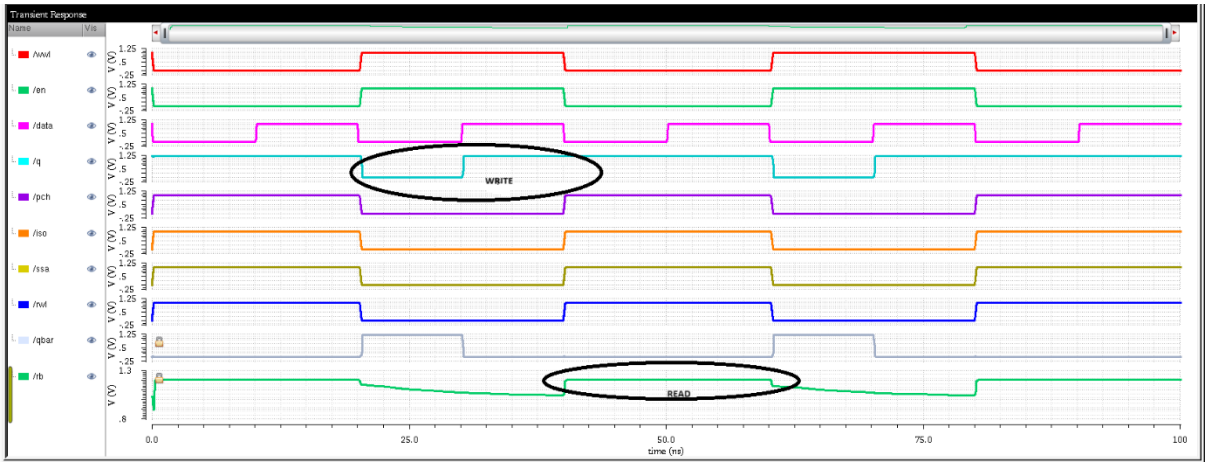

FIGURE 3.1 SINGLE 10T SRAM READ AND WRITE OPERATION

From figure 3.2, The stored data Q and the external activation signal are inputs to the CIM circuit, which performs a logical AND operation. The output port delivers logic 1 only when both Q and the activation signal are logic 1; otherwise, the output is logic 0

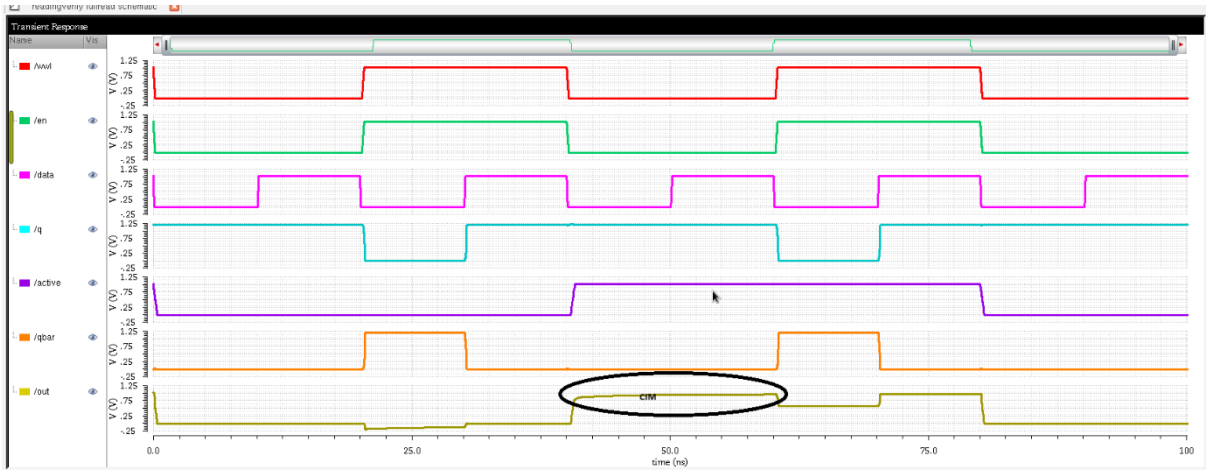

FIGURE 3.2 SINGLE 10T SRAM CIM OPERATION

3.1.2 SIMULATION RESULTS OF 2*2 SRAM ARRAY

From the figure 3.3, When the decoder control signal is low (Control = 0), the array enters write mode. The write signal selects the active row.

Row 1 Write (Control = 0, Write = 0):WWL1 is activated (WWL1 = 1), enabling the first row. Data logic 1 is written to Q1 and Q2. No output occurs at Q3 and Q4.

Row 2 Write (Control = 0, Write = 1) WWL2 is activated (WWL2 = 1), enabling the second row. Data logic 0 is written to Q3 and Q4. No output occurs at Q1 and Q2.

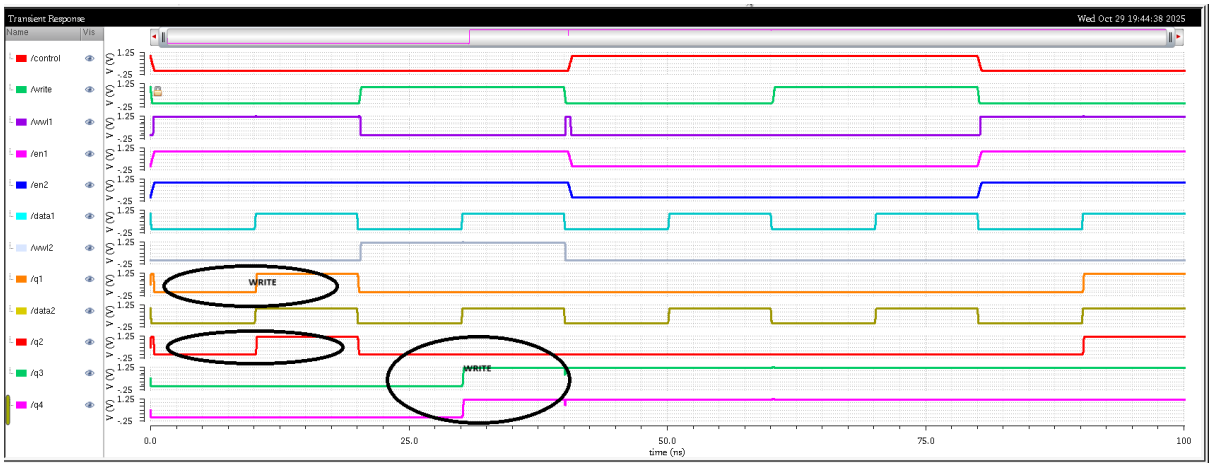

FIGURE 3.3 2*2 10T SRAM CIM ARRAY-WRITE OPERATION

From the figure 3.4, When the decoder control signal is high (Control = 1), the array enters read mode. The read signal activates the respective read word lines sequentially.

Row 1 Read : When RWL1 is activated (RWL1 = 1), the data stored in Q1 and Q2 (logic 1) is read through the sense amplifier, and the output appears on read bit line RB1.

Row 2 Read: When RWL2 is activated (RWL2 = 1), the data stored in Q3 and Q4 (logic 0) is read through the sense amplifier, and the output appears on read bit line RB2.

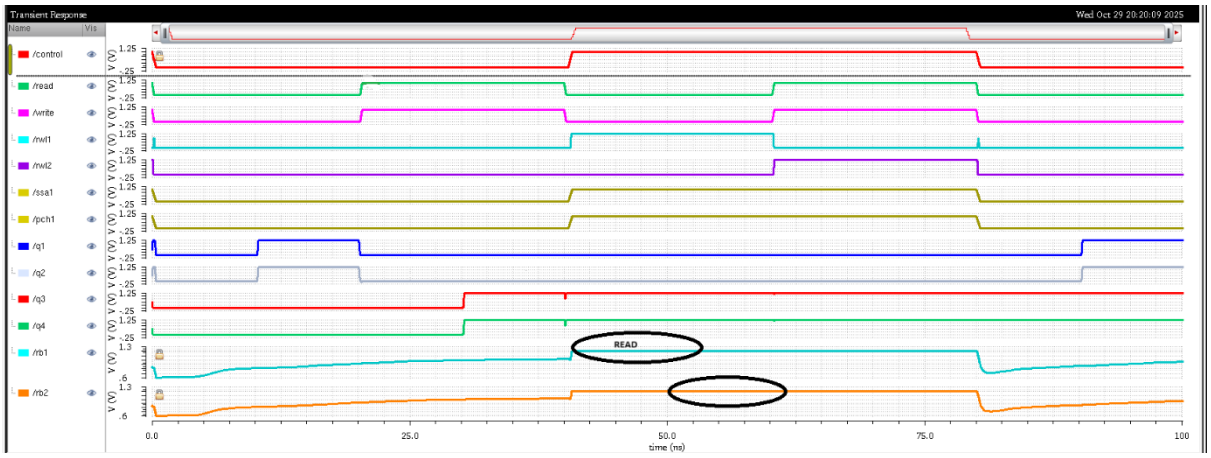

FIGURE 3.4 2*2 10T SRAM CIM ARRAY-READ OPERATION

Each SRAM cell executes a logical AND operation between its stored value (q, q1, q2, q3) and the external activation signal. When both the stored data and activation signal are logic 1, the output is logic 1; otherwise, it is logic 0. The computation results appear at the respective output ports:output, out1, out2, and out3.

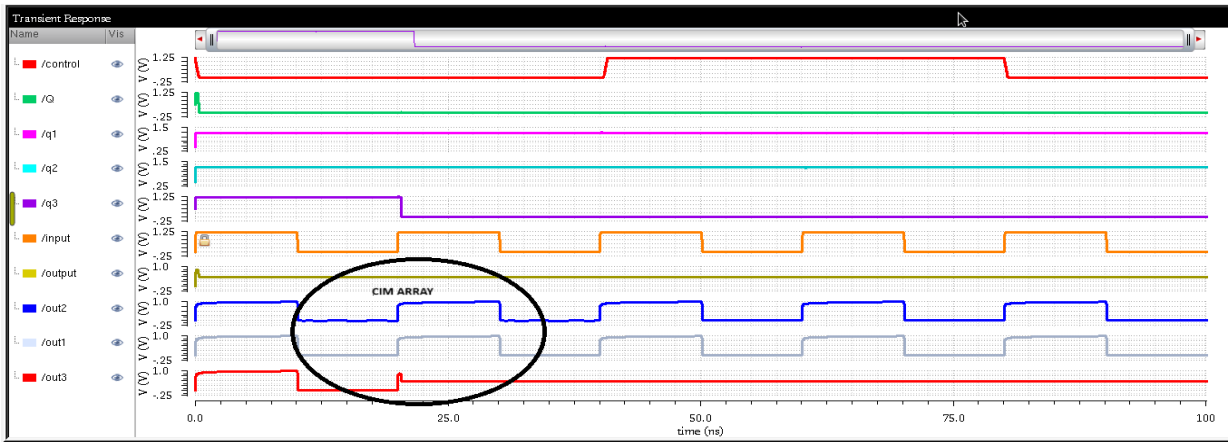

FIGURE 3.5 2*2 10T SRAM CIM ARRAY-AND OPERATION

3.2 ANALYSIS OF 10T SRAM CIM

The power and delay analysis for 10T SRAM CIM and 2*2 10T SRAM ARRAY were discussed in this section.

3.2.1 POWER AND DELAY ANALYSIS OF 10T SRAM CELL

The 10T SRAM CIM cell achieves low power consumption (17.06 µW) with a fast read access time of 20 ps, showing excellent read efficiency for CIM operations. Although the write access time is higher at 63 ps, the overall performance is efficient and suitable for low-power AI and edge applications.

TABLE 3.1 POWER AND DELAY ANALYSIS OF SINGLE 10T SRAM CIM

PARAMETER	SRAM
Power	17.06uW
Read access time	20ps
Write access time	63ps

3.2.2. POWER AND DELAY ANALYSIS OF 2*2 10T SRAM ARRAY

The SRAM array achieves low power (80 µW) with fast read (40 ps) and write (83 ps) operations. Overall, it delivers high-speed and energy-efficient performance suitable for CIM applications.

TABLE 3.2 POWER AND DELAY ANALYSIS OF 2*2 10T SRAM ARRAY

PARAMETER	SRAM
Power	80uW
Read access time	40ps
Write access time	83ps

3.2.3 STABILITY ANALYSIS FOR SINGLE 10T SRAM CIM

The stability analysis of our proposed 10T SRAM design evaluates the read, write, and hold noise margins, confirming improved data stability and reliable operation under different conditions.

WRITE NOISE MARGIN

This figure 3.6 shows that, the proposed 10T SRAM design achieves a write noise margin of 307 mV, ensuring better write ability. This higher WNM indicates improved stability and reliable data storage during write operations.

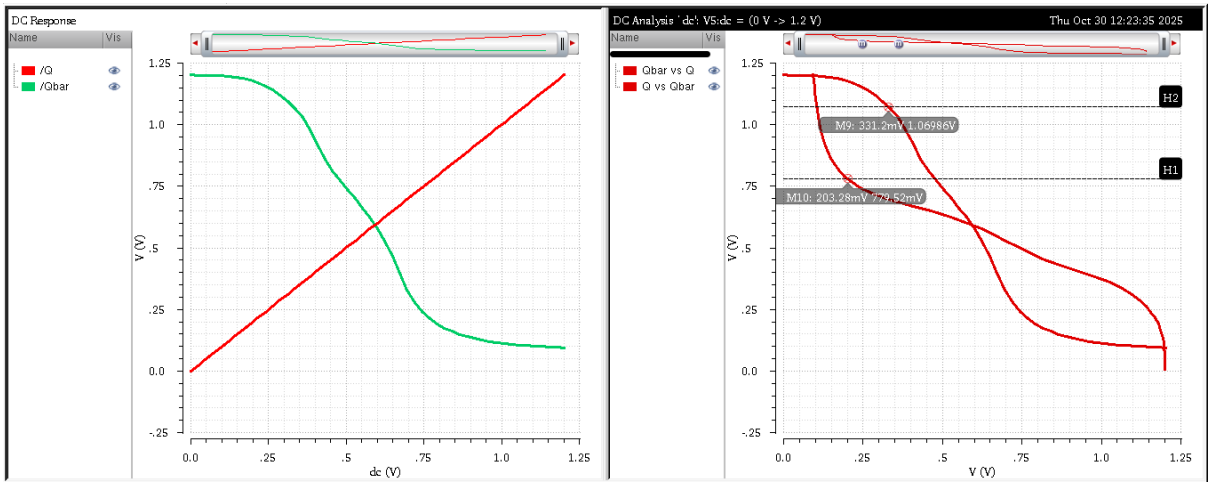

FIGURE 3.6 WRITE SNM

READ NOISE MARGIN

This figure 3.7 shows that, the proposed 10T SRAM cell achieves a read noise margin of 439 mV, ensuring stable read operation without disturbing the stored data.

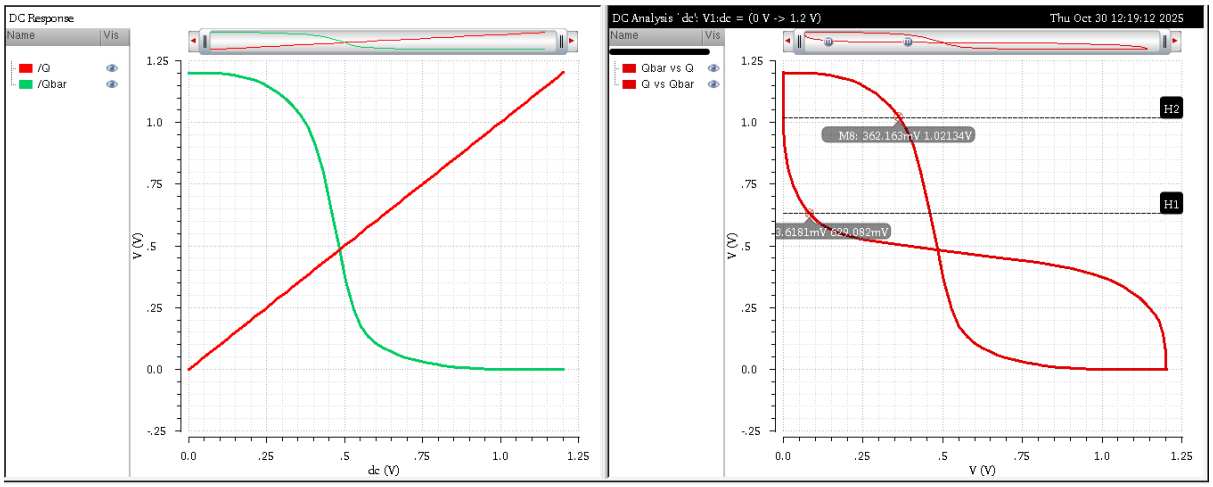

FIGURE 3.7 READ SNM

HOLD NOISE MARGIN

This figure 3.8 shows that, the proposed 10T SRAM cell attains a hold noise margin of 509 mV, indicating strong data retention capability. This high HNM ensures reliable stability when the cell is in the hold state.

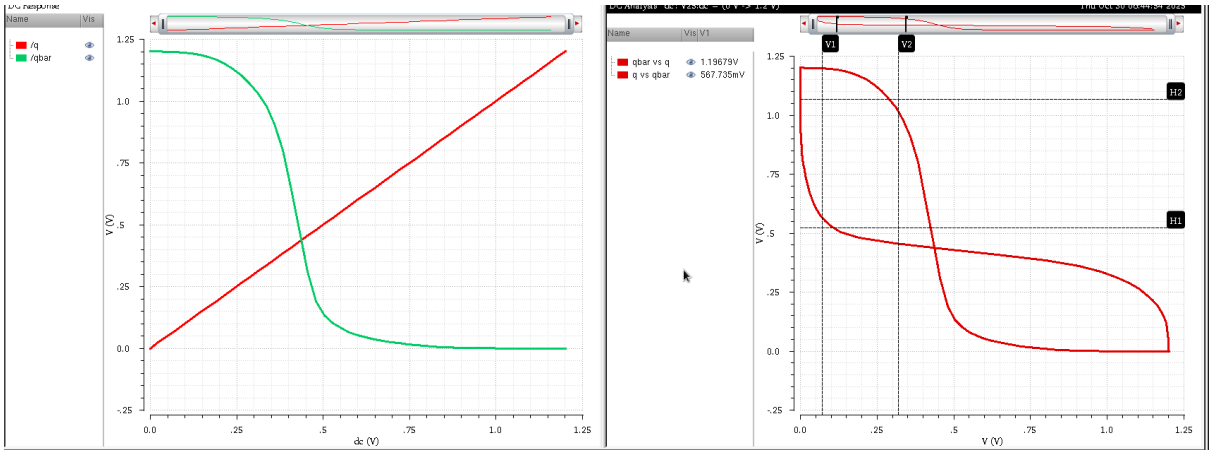

FIGURE 3.8 HOLD SNM

CONCLUSION AND FUTURE WORKS

CHAPTER 4

CONCLUSION AND FUTURE WORKS

4.1 CONCLUSION

The proposed 10T CIM-based SRAM design, implemented in 90 nm technology, achieves improved stability and efficiency with decoupled read/write paths and a high-threshold compute NMOS. The measured noise margins — WNM: 307 mV, RNM: 439 mV, and HNM: 508 mV — demonstrate enhanced reliability and robust performance, making the design well-suited for low-power in-memory computing applications.

4.2 FUTURE WORKS

Future work includes extending the design to larger SRAM arrays, performing PVT and post-layout analysis, and optimizing peripheral circuits for improved speed, power, and reliability in advanced technology nodes.

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SUSTAINABLE DEVELOPMENT GOALS (SDG)

Complete SDG Mapping for Project: 10T CIM-Based Reconfigurable SRAM

SDG	Target	Outcome / Relevance to Project	Percentage %
SDG 1 – No Poverty	1.4	Better technical skills → better employability → reduces poverty	30%
SDG 2 – Zero Hunger	2.4	Low-power chips can support smart agriculture sensors	20%
SDG 3 – Good Health & Well-being	3.8	Low-power chips used in portable medical devices	20%
SDG 4 – Quality Education	4.4	Enhances VLSI, research, and semiconductor skills	95%
SDG 5 – Gender Equality	5.5	Equal participation: 2 boys + 2 girls in the team	100%
SDG 6 – Clean Water & Sanitation	6.3	Low-power design indirectly reduces water usage in semiconductor cooling systems	25%
SDG 7 – Affordable & Clean Energy	7.3	Ultra low-power SRAM saves energy	90%
SDG 8 – Decent Work & Economic Growth	8.6	High-skill engineering work → enhances career growth	40%
SDG 9 – Industry, Innovation & Infrastructure	9.5	CIM architecture improves AI/ML hardware innovation	85%
SDG 10 – Reduced Inequalities	10.2	Equal team participation + research access	50%
SDG 11 –	11.6	Low-power chips for smart city IoT	75%

Sustainable Cities & Communities		devices	
SDG 12 – Responsible Consumption & Production	12.2	Low-leakage design reduces power wastage	80%
SDG 13 – Climate Action	13.3	Low power = lower carbon emissions	70%
SDG 14 – Life Below Water	14.3	Reduced energy → less pollution affecting oceans	40%
SDG 15 – Life on Land	15.1	Low-carbon design benefits terrestrial ecosystems	40%
SDG 16 – Peace, Justice & Strong Institutions	16.7	Teamwork, ethical research, inclusive participation	20%
SDG 17 – Partnerships for the Goals	17.7	Team collaboration + academic partnerships	30%