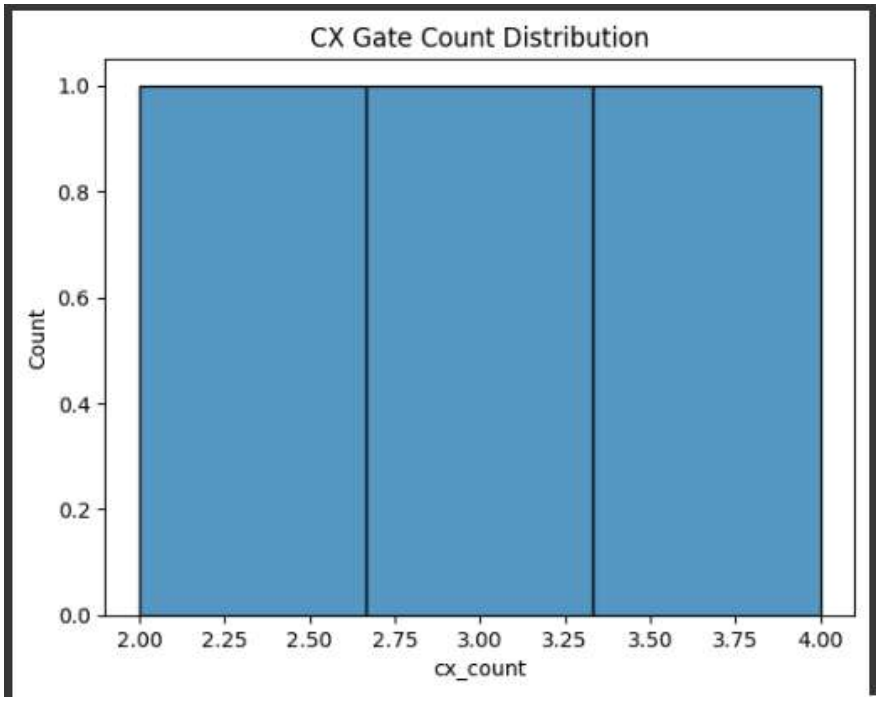
Generated Circuits :

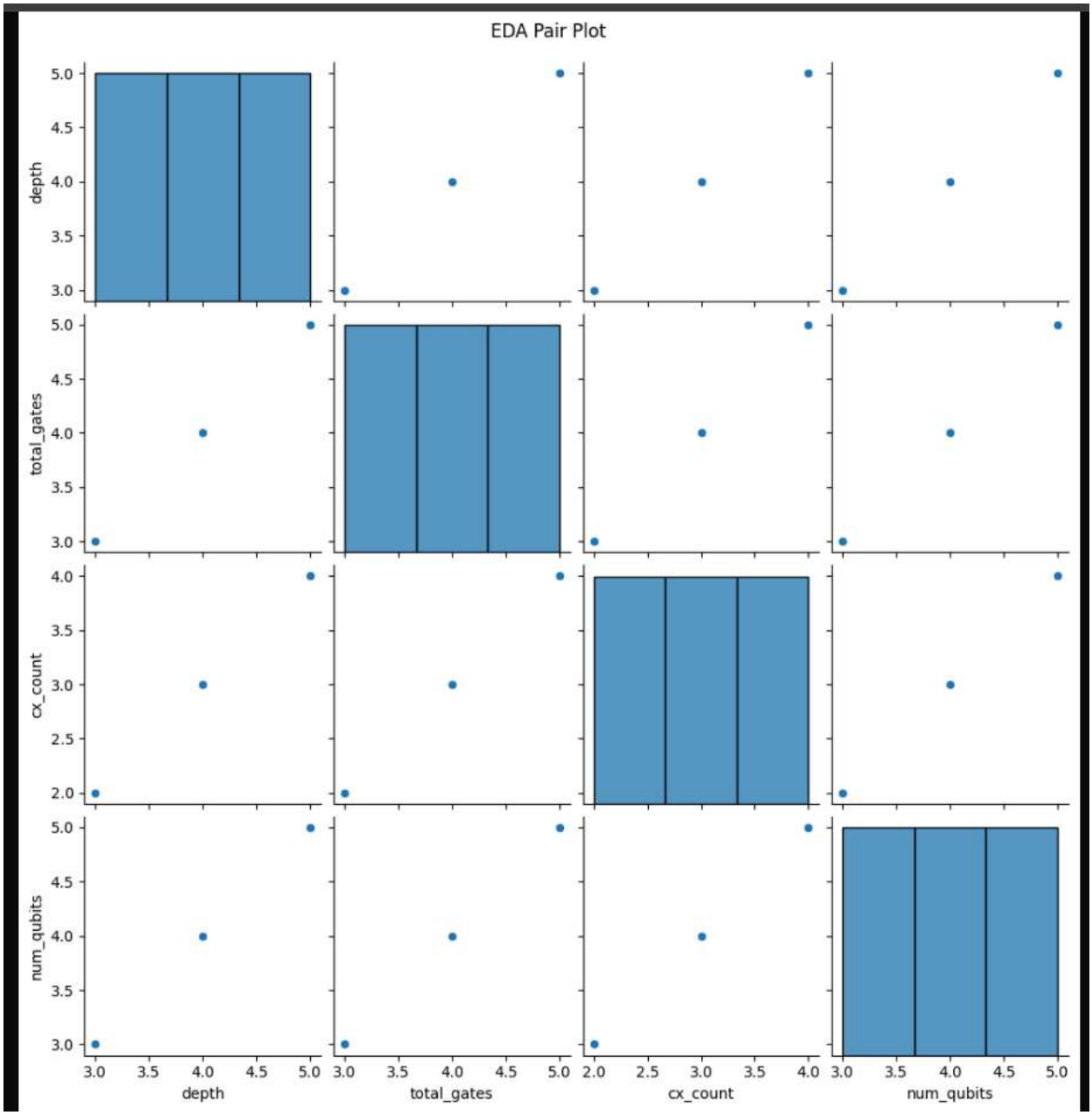
	name	num_qubits	depth	width	total_gates	cx_count
0	GHZ_3	3	3	3	3	2
1	GHZ_4	4	4	4	4	3
2	GHZ_5	5	5	5	5	4

Feature Analysis report :

{'total_gates': 4,
'depth': 4,
'num_qubits': 4,
'cx_count': 3,
't_count': 0,
'h_count': 1}

EDA

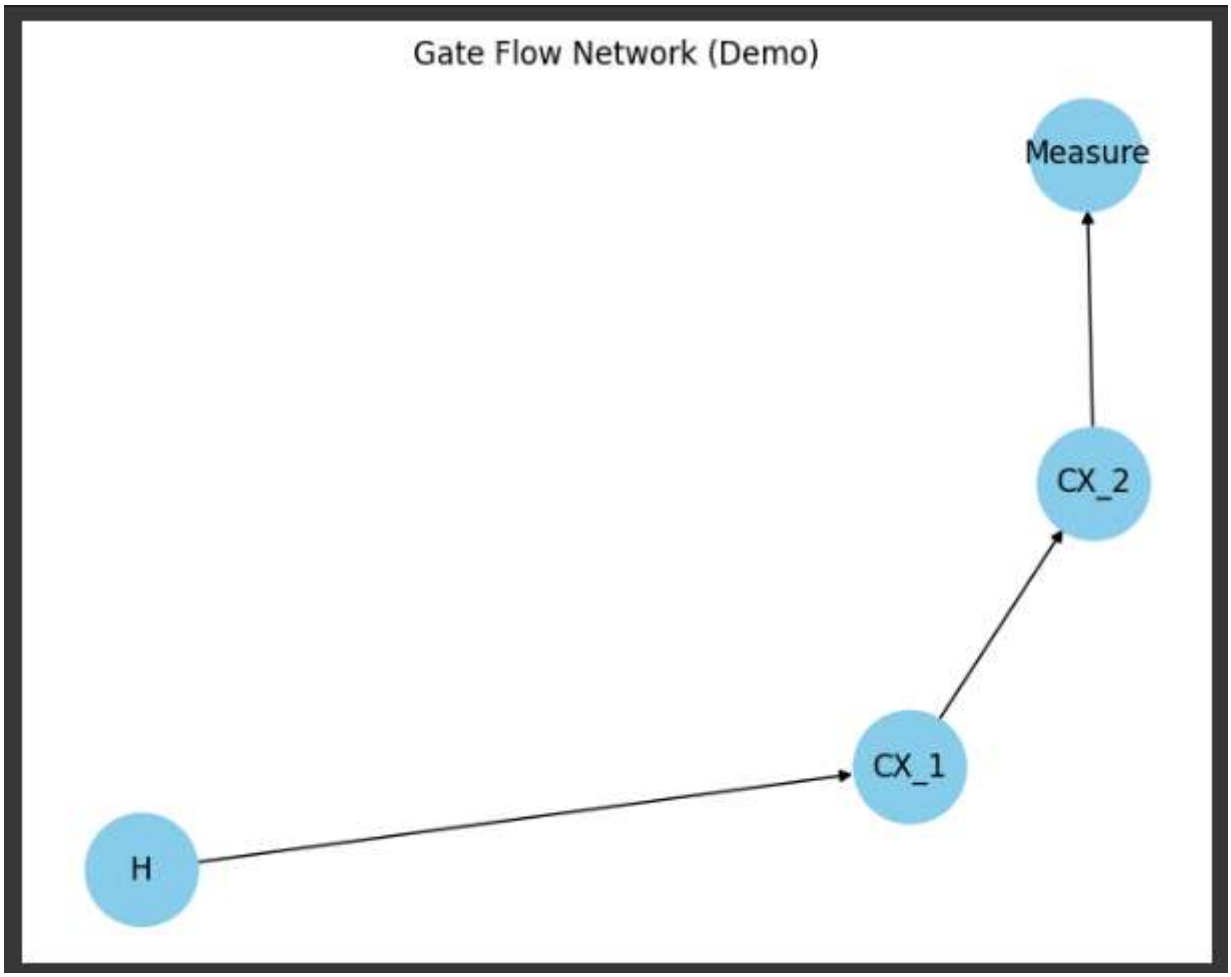



EDA Pair Plot
depth
total_gates
cx_count
num_qubits
depth
total_gates
cx_count
num_qubits

Analysis:

	compiler	depth	cx_count	total_gates	width	circuit
0	Qiskit	3	2	3	3	GHZ_3
1	Qiskit	4	3	4	4	GHZ_4
2	Qiskit	5	4	5	5	GHZ_5
3	Cirq	3	2	3	3	GHZ_3
4	Cirq	4	3	4	4	GHZ_4

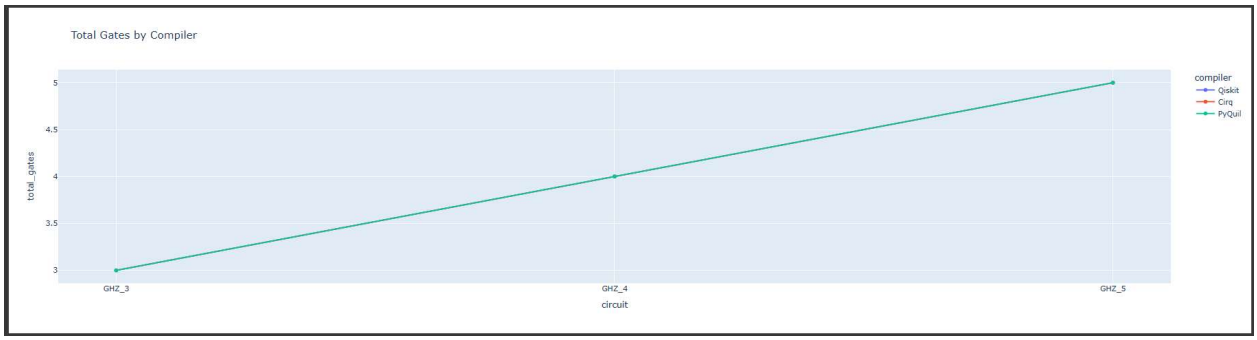
Plot :



Alert Rules Output :

```
[]
```

Report Plot :



Report :

```
For GHZ_3, best compiler by depth is: Qiskit (Depth = 3)
For GHZ_4, best compiler by depth is: Qiskit (Depth = 4)
For GHZ_5, best compiler by depth is: Qiskit (Depth = 5)
```