ECE4063 - Image Thresholding

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1 Assumptions

2 Documentation

2.1 RGB to Grayscale conversion

2.2 Histogram Module

2.2.1 Description

The histogram module was based on a design from an article found on the IEEE website. The biggest problem we had in our initial attempts to create a histogram module as the latency in RAM access. The issue is that one cannot simultaneously read and write to a RAM, so when consecutive grayscale input values are identical, we are unable to correctly update the relevant RAM address. Our design overcomes this problem by specifically addressing the RAM latency issue. This histogram design consists of individual histogram cells, each of which accesses its own RAM. By switching between these cells, the histogram is able to share the latency burden across multiple RAMs. Our histogram cells had a latency of three cycles, so we used three cells. This means that each cycle, one histogram cell is always ready to take in an input value. In order to get data out, we simply used a combinational logic block to address all three RAMs simultaneously and sum their outputs to get the true histogram value. Whilst this architecture does use more RAM resources, it is much easier to understand and thus enabled us to be confident that the system worked correctly.

2.2.2 RTL Diagram

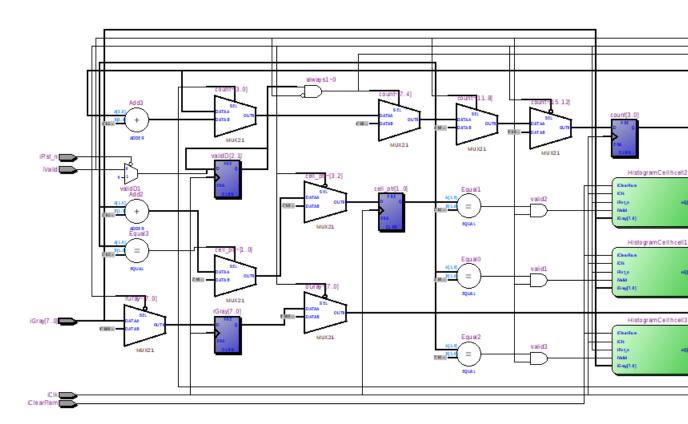


Figure 1: Histogram module RTL

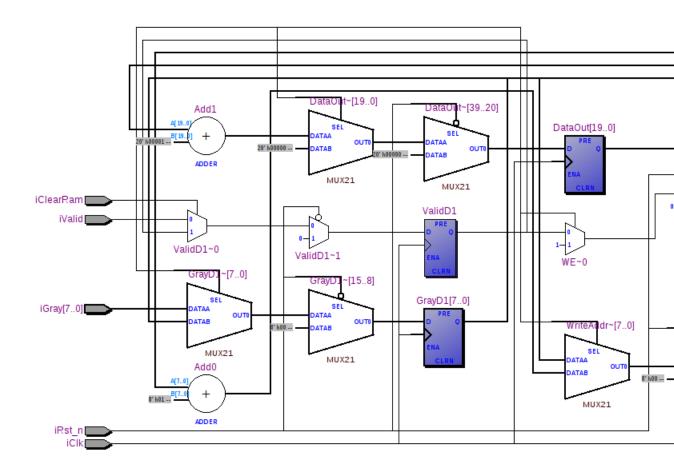


Figure 2: Histogram Cell module RTL

2.2.3 Module Testbench Results

2.3 Cumulative Histogram Module

2.4 Thresholding Module

2.4.1 Description

The thresholding module is extremely simple. All it needs to do is take in an 8 bit greyscale value and output either a white (255) if the value is above the threshold, or a black (0) if the value is below the threshold.

2.4.2 RTL Diagram

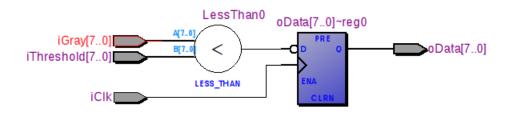


Figure 3: Thresholding module RTL

2.5 Displaying things

2.5.1 Description

In order to display the greyscale image, histogram, cumulative histogram, and threshold, we wrote a module to handle multiplexing between them using the switches on the DE2 board, called Arbitrator. This module takes in pixel outputs from the various modules and multiplexes them depending on the switch positions. In order to display images, we simply piggyback on the X_Cont and Y_Cont signals and modify the $wr1_data$ and $wr2_data$ inputs to the SDRAM with the appropriate pixel data.

Displaying the actual histogram data requires slightly more effort. First we need to extract the histogram data from the histogram RAM and convert the histogram bin sizes into pixels for display on the screen. To do this we have a module called HistogramDisplayer. This module takes in the Y_Cont signal and uses it to index the histogram RAM. Based on the histogram value from the RAM, it scales the histogram value, and uses the X_Cont signal to determine the length of the line to be displayed.

- ${\bf 3}\quad {\bf Acknowledgements}$
- 4 Improvements
- 5 Conclusion