Foxconn Precision Co. Inc.
945M09 Schematic

Fab.1.0
Data: 2007/08/18

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Title: Page Map

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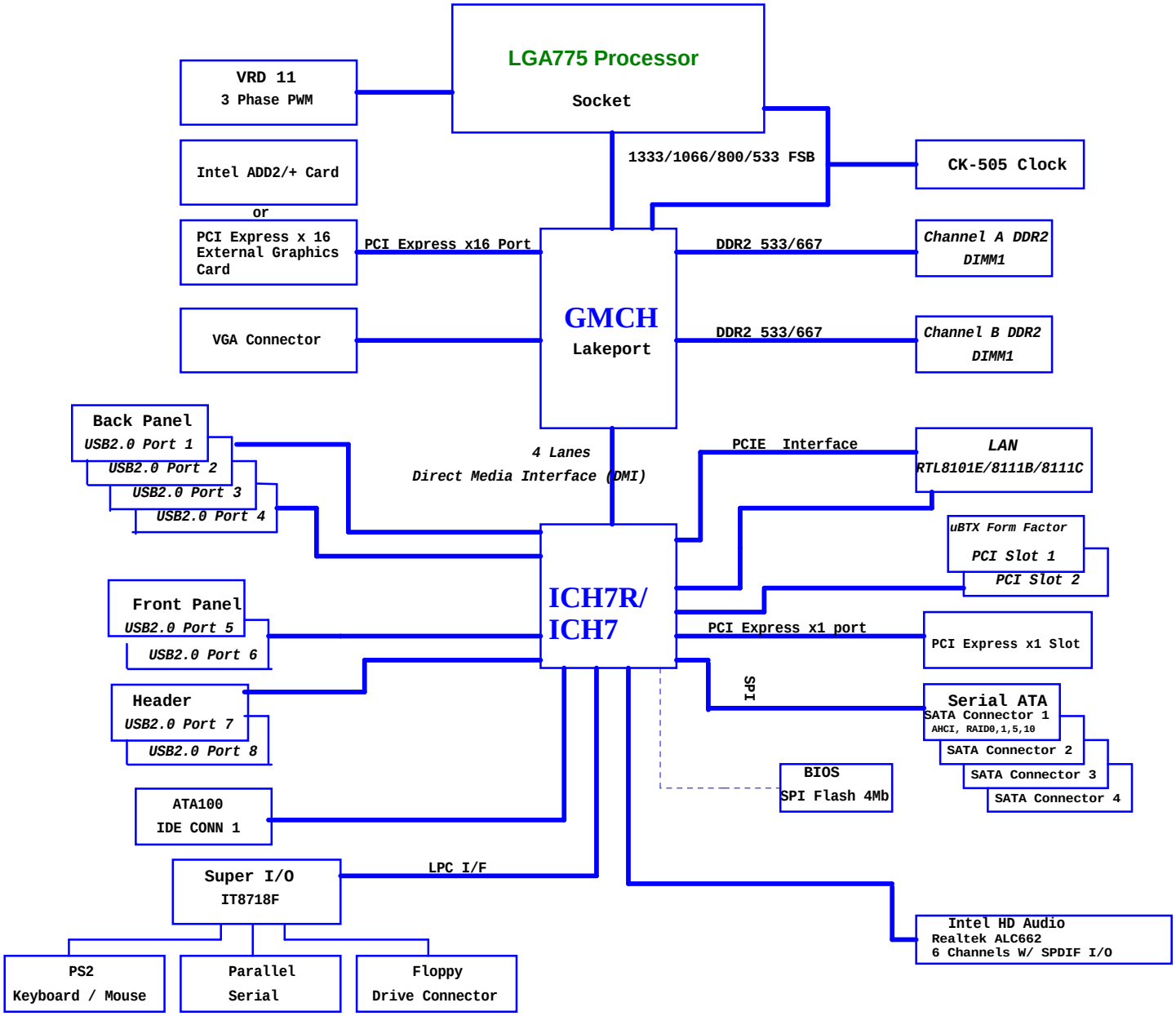

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Title: Topology

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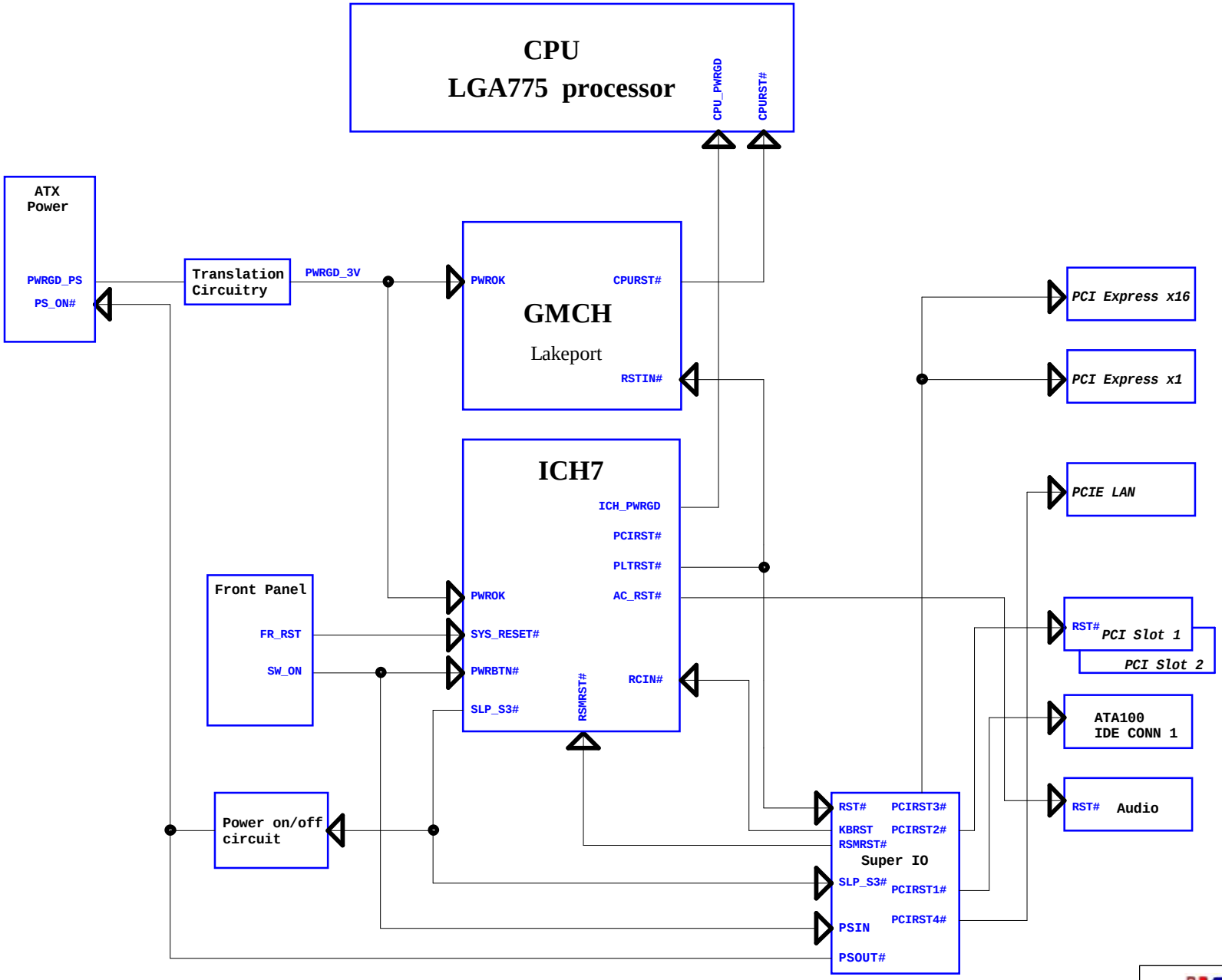

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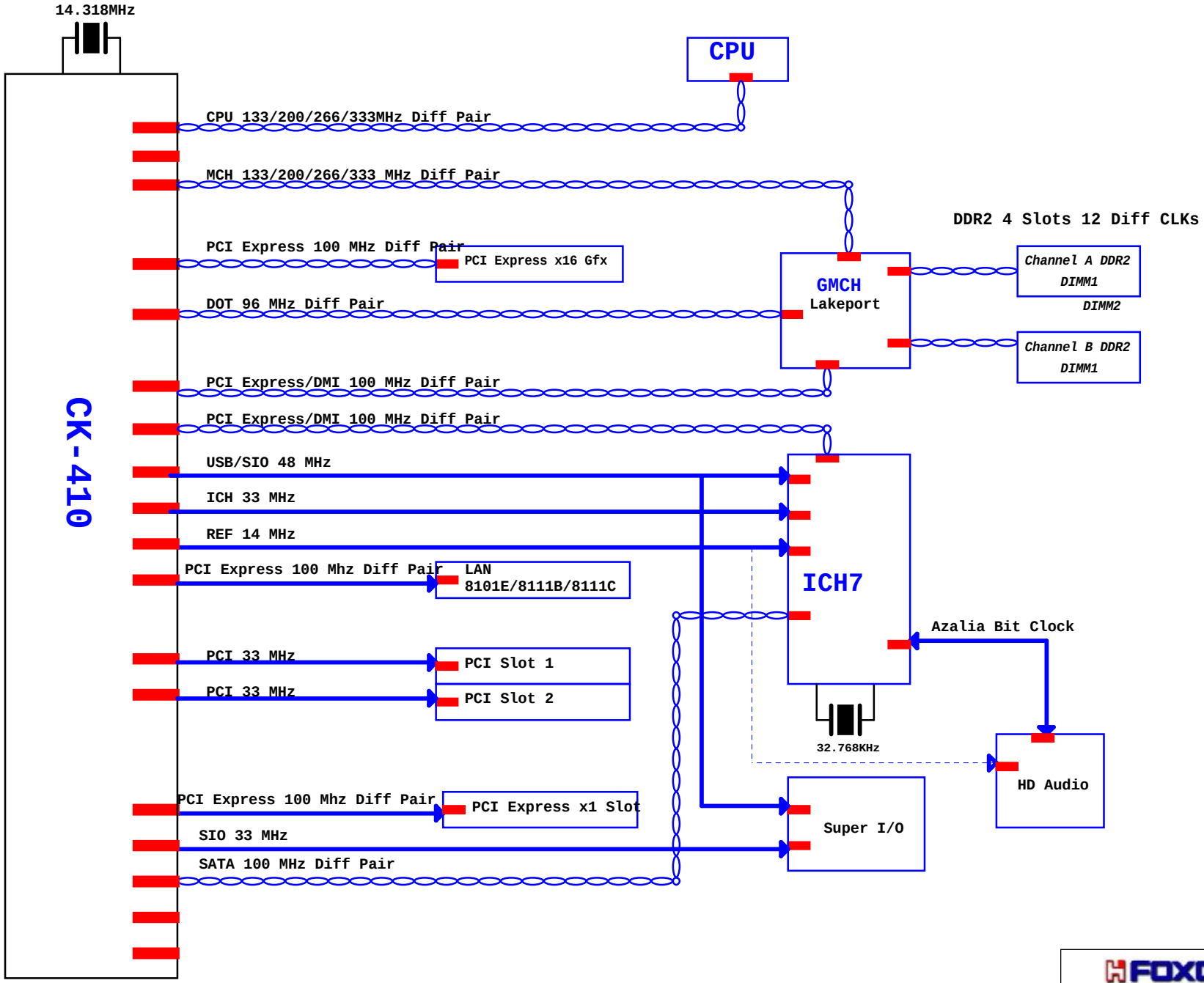
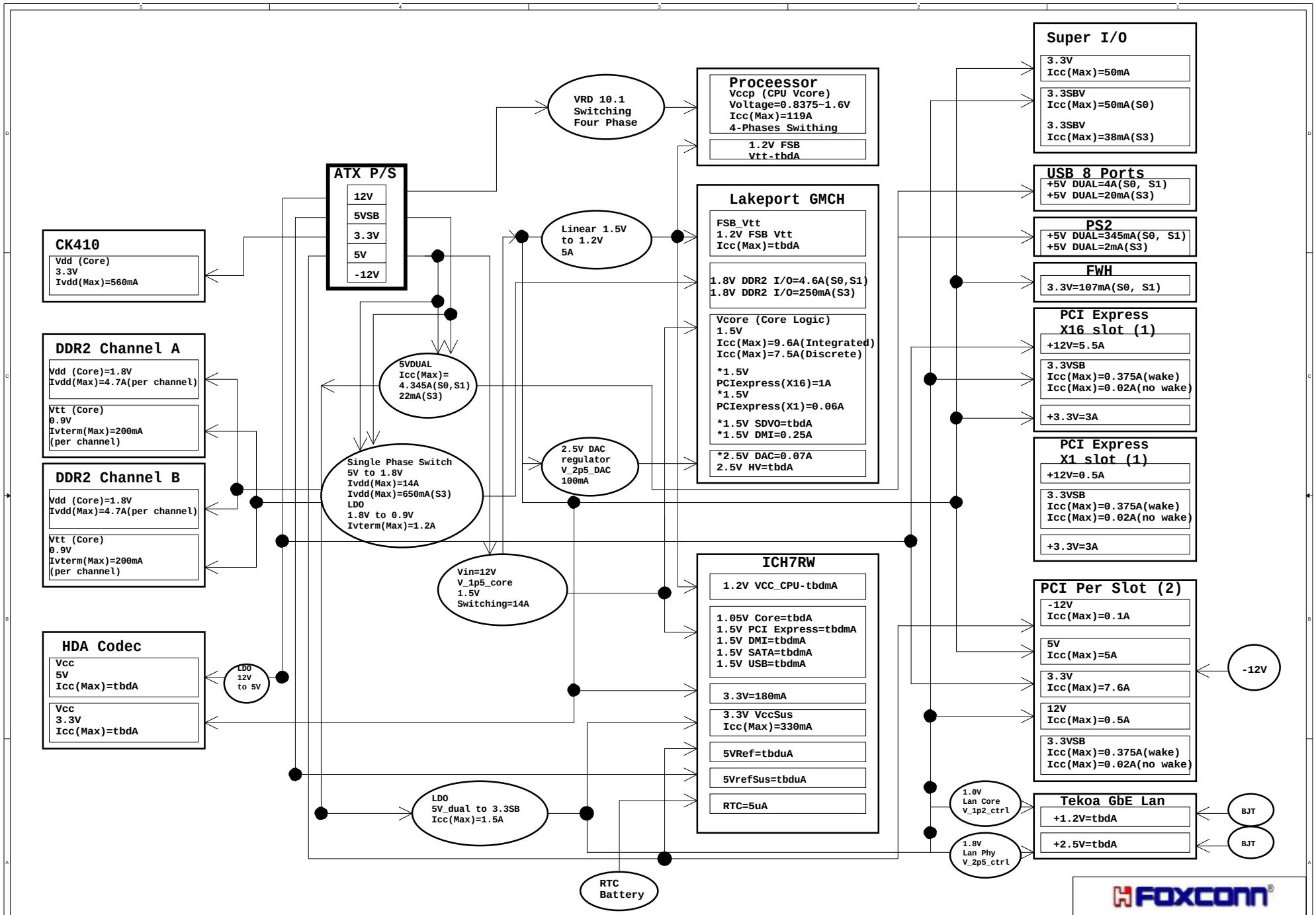
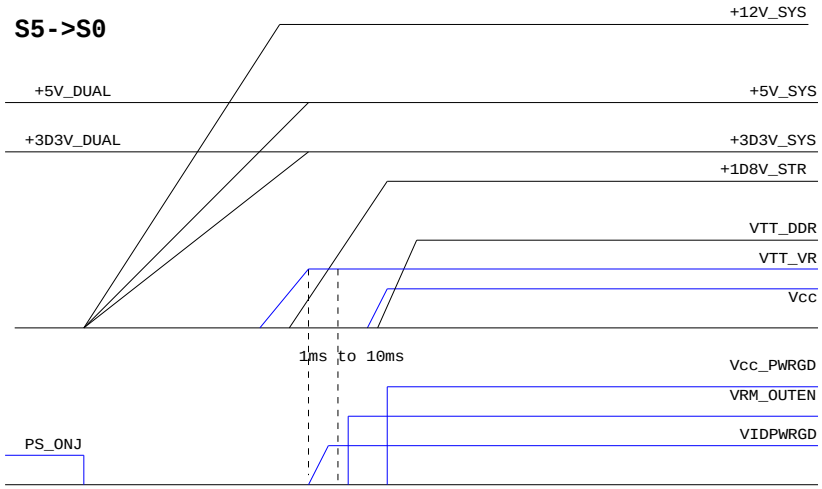
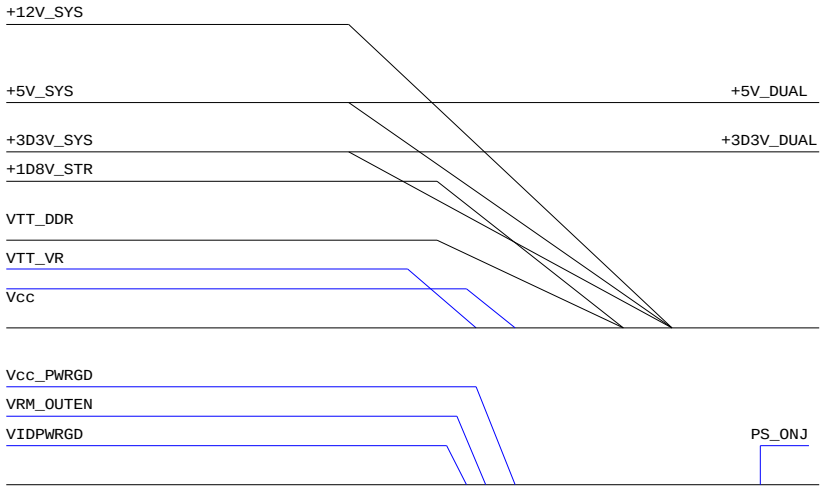




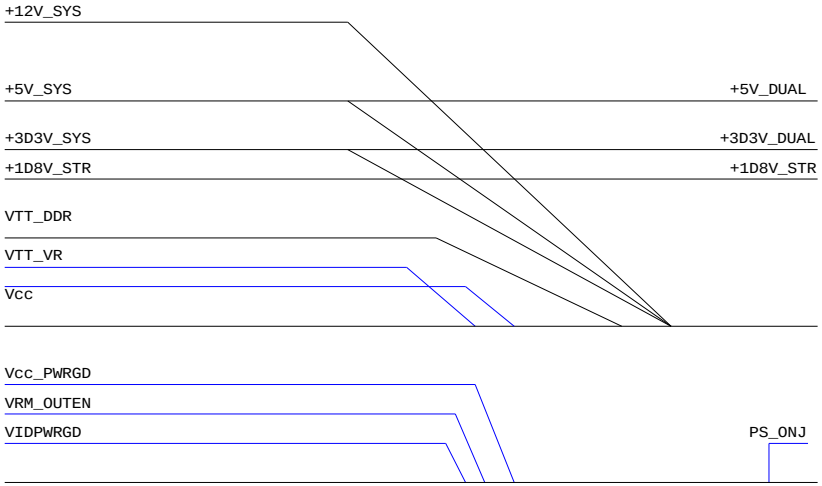
S5->S0



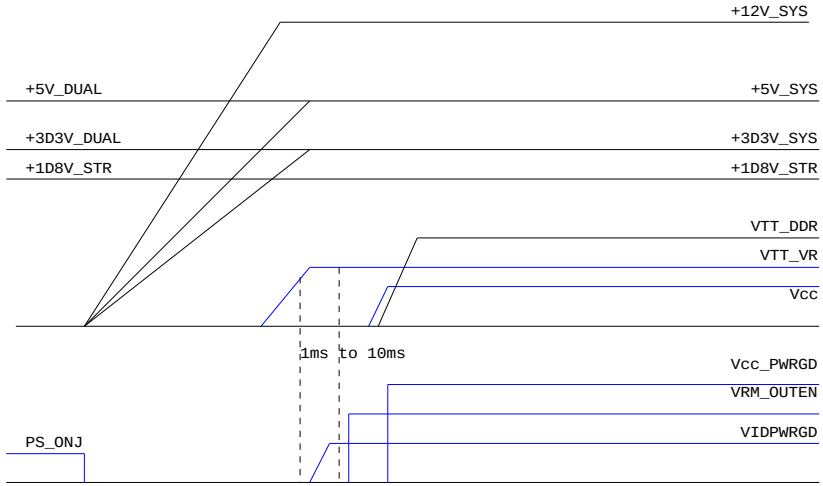
S0->S5



S0->S3



S3->S0



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Title: Power Sequence		
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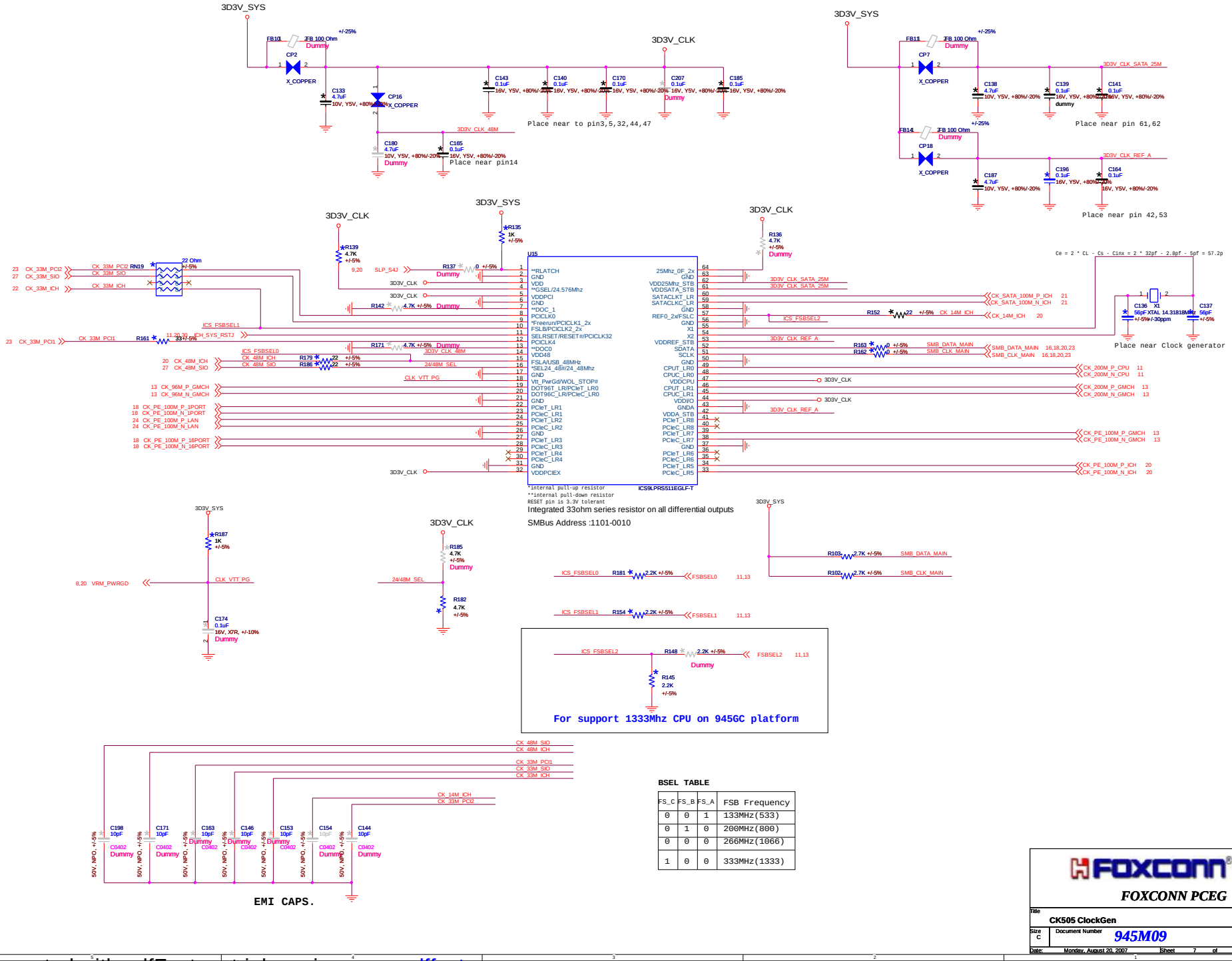
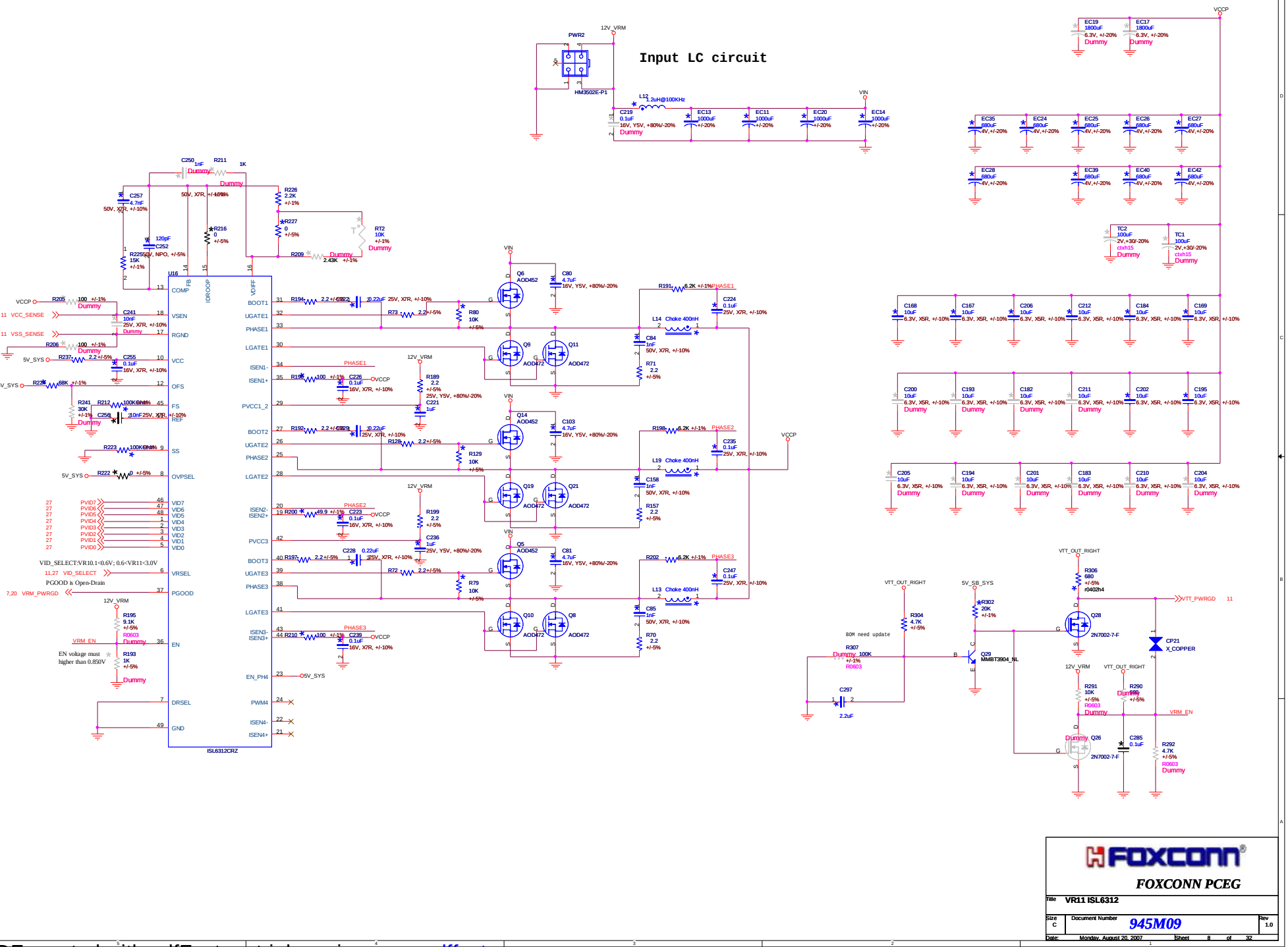
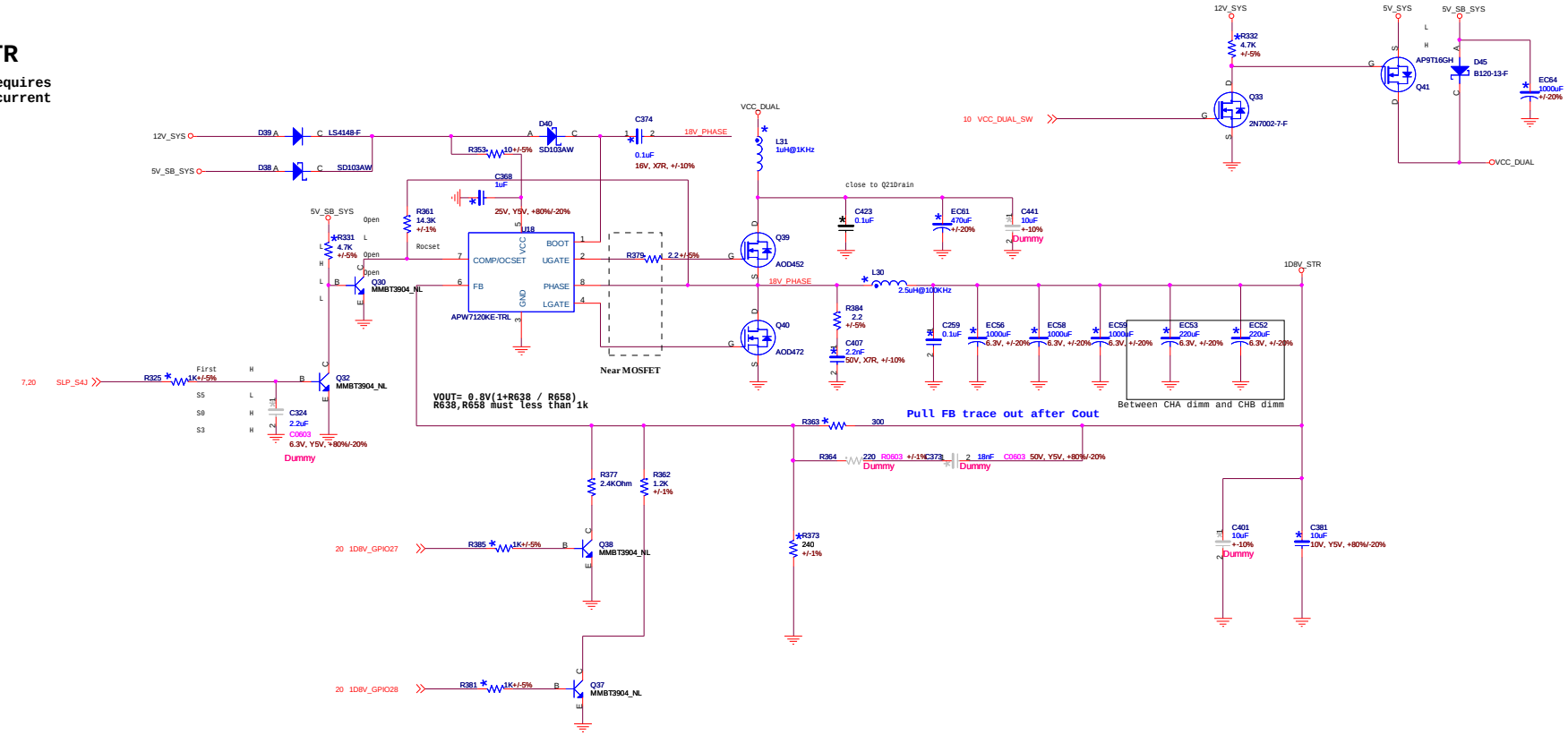


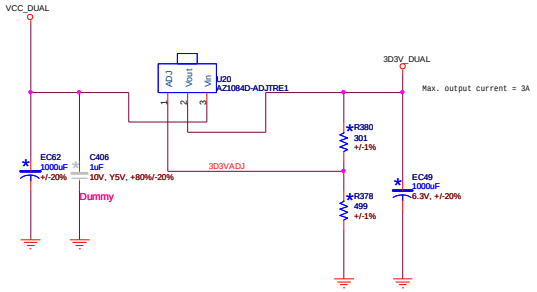


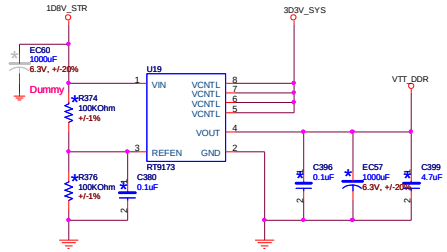
1D8V_STR

1.8V Power requires
17A maximum current



DDR_VTT





Vout=Vref(1+R2/R1)+IadjR2
R1 is Up Resistor.
Iadj=50uA
Vref=1.25V

3D3V_DUAL

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Title	DDR2 1.8V/0.9V 5VDUAL	
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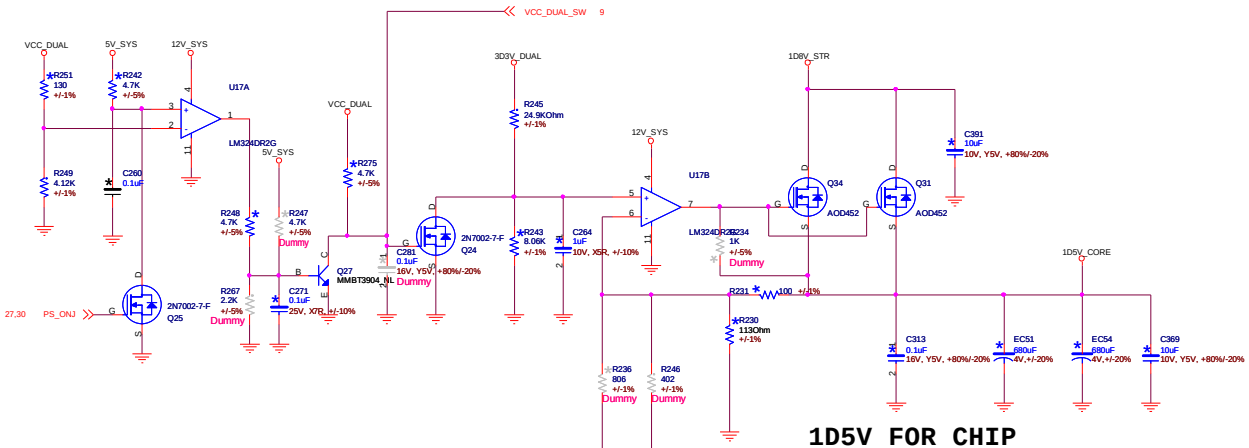
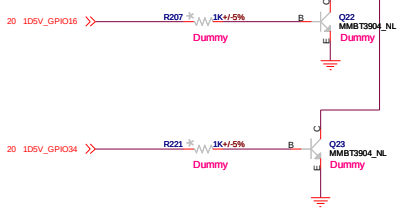
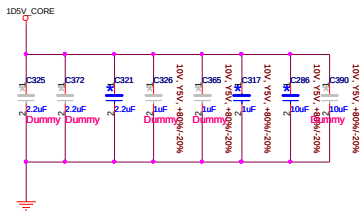
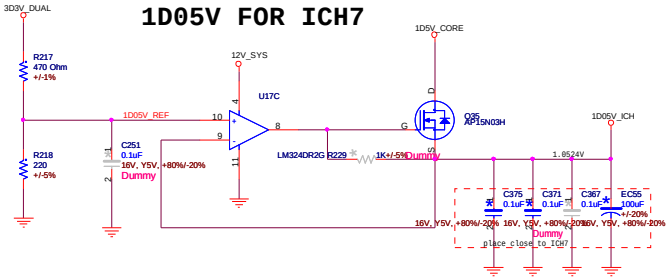


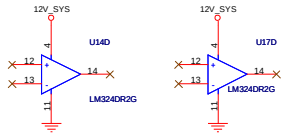
1D5V FOR CHIP



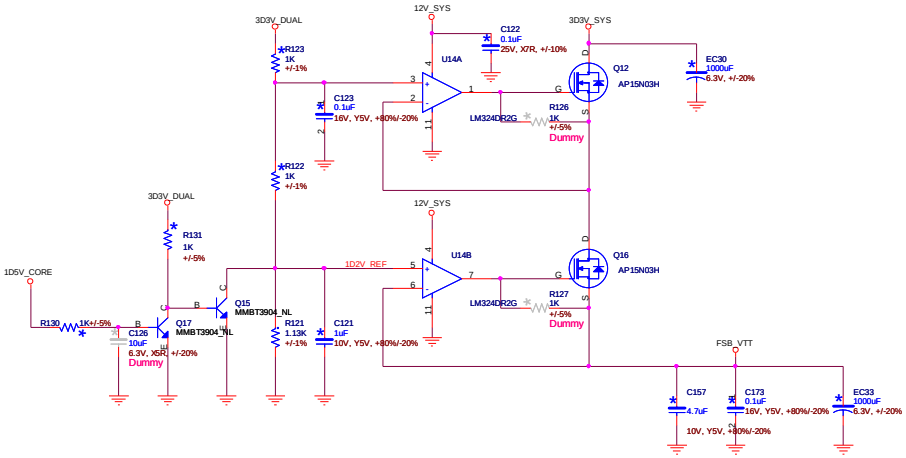


1D05V FOR ICH7

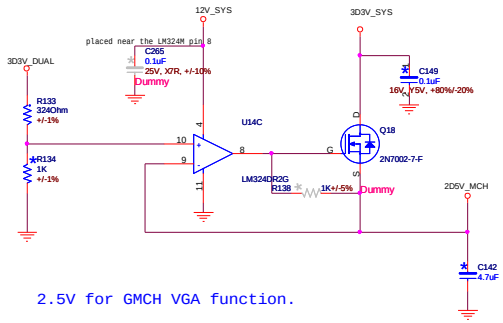




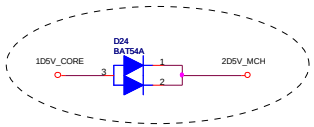
FSB_VTT



2D5V FOR GMCH



2.5V for GMCH VGA function.



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Title: Power 1.5V 1.2V 1.05V

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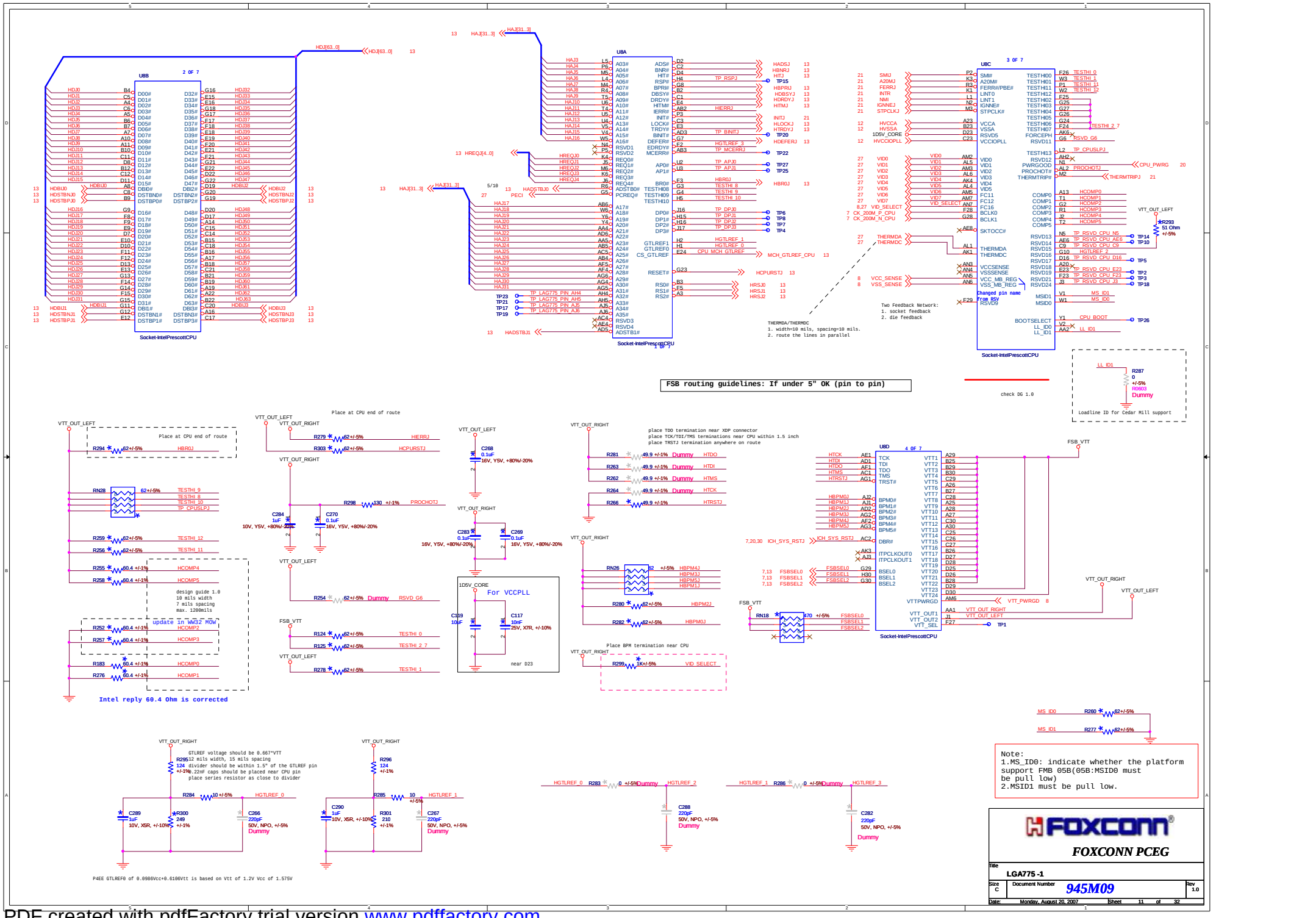

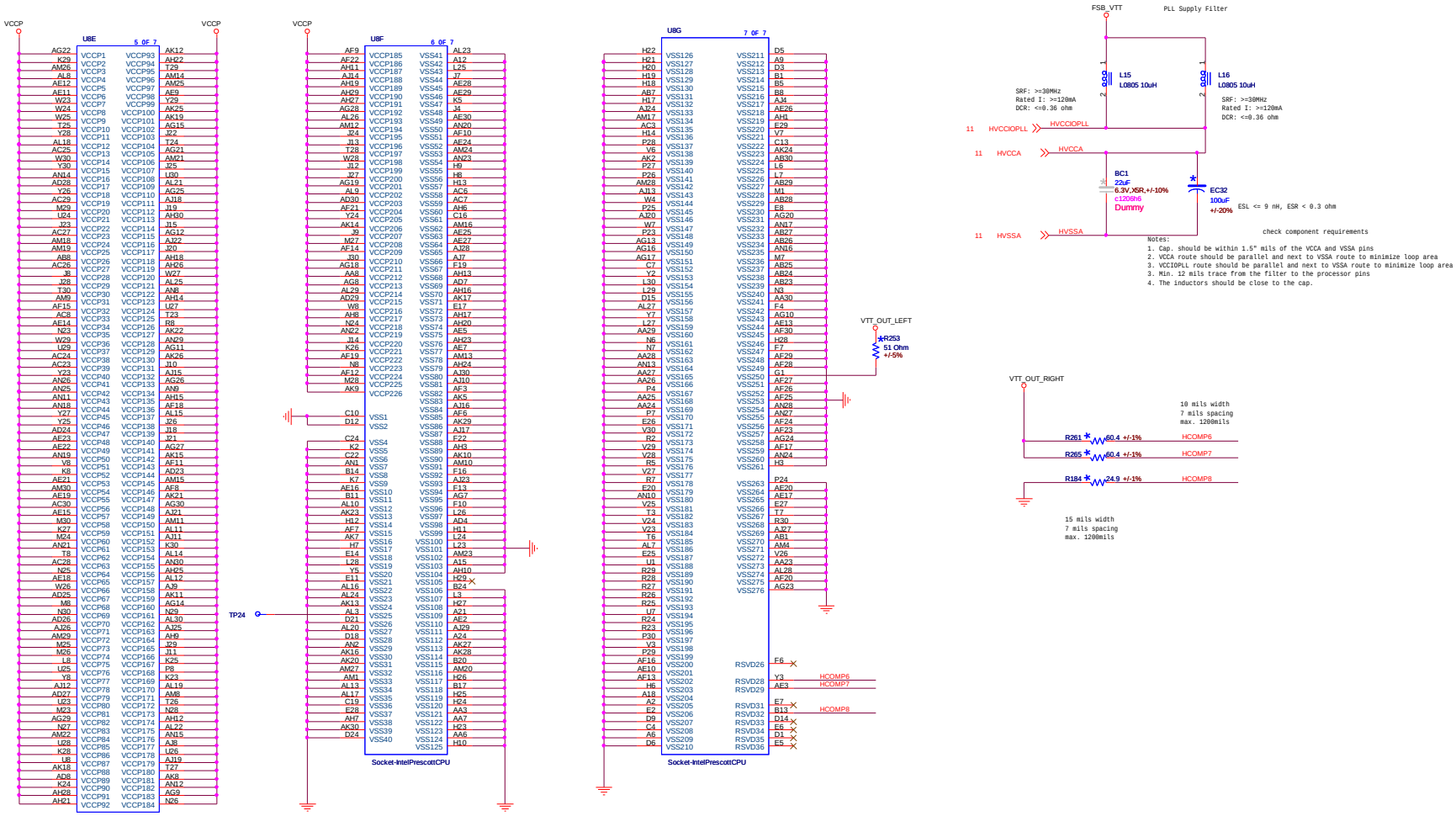

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Title: LGA775 -2

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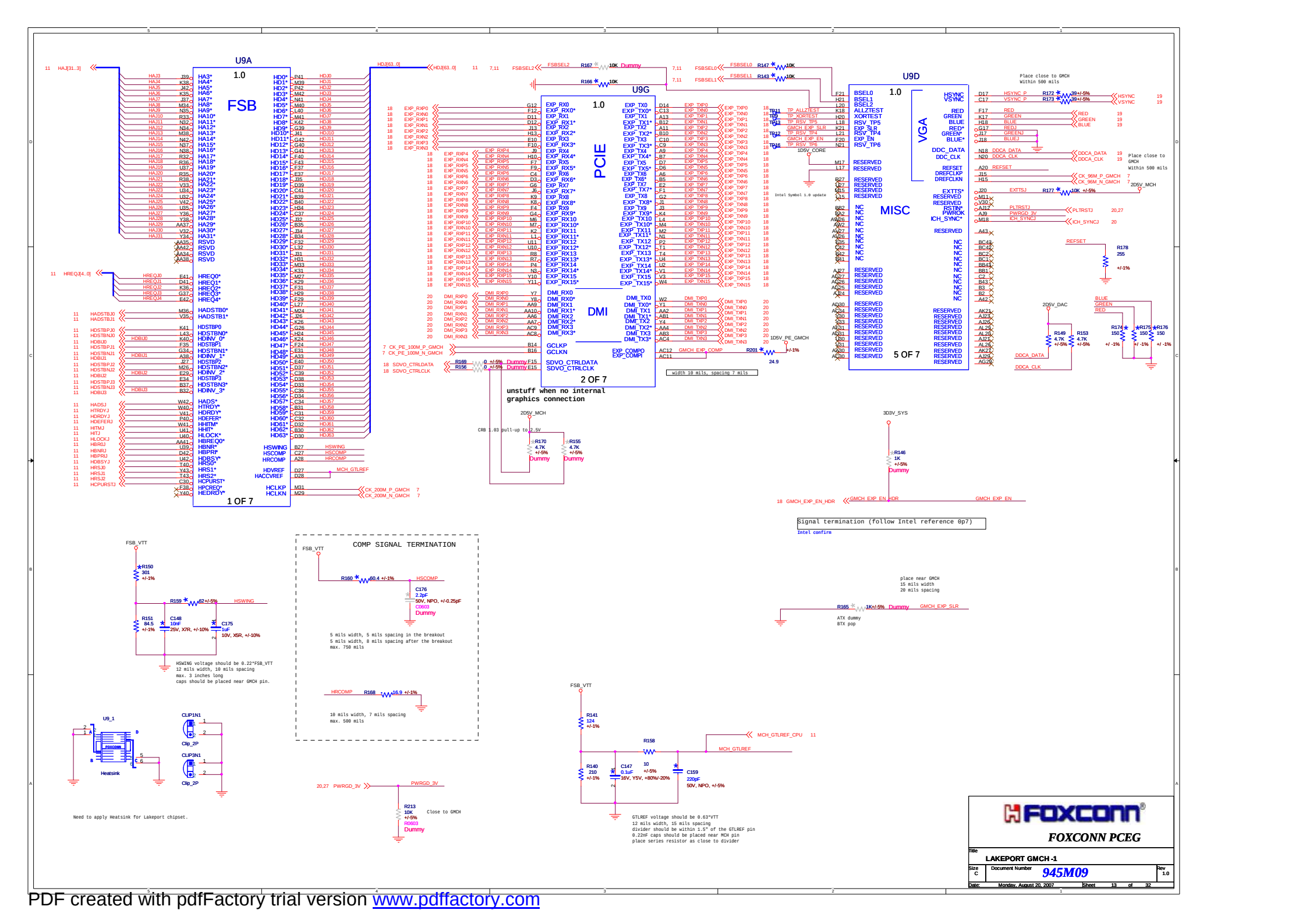

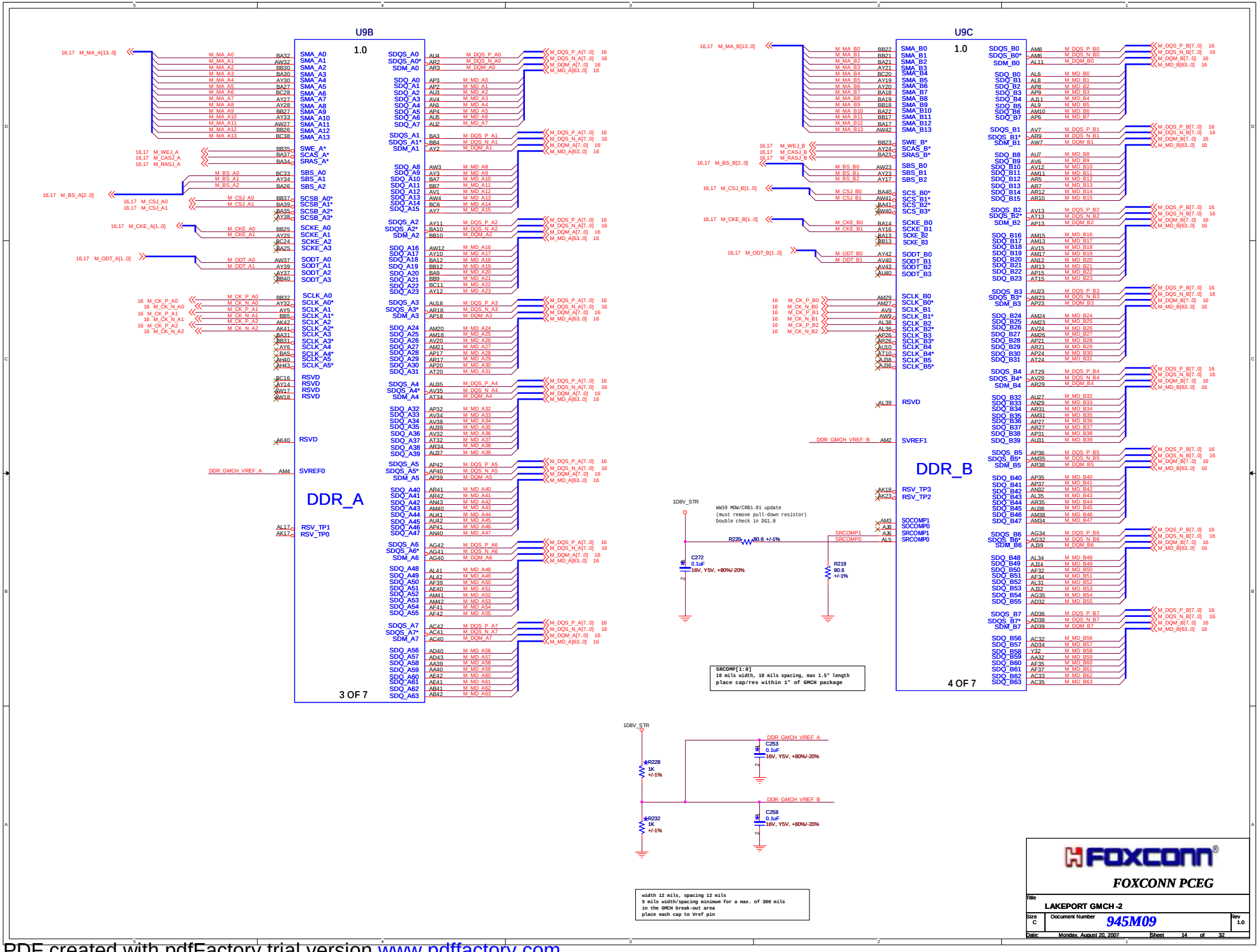

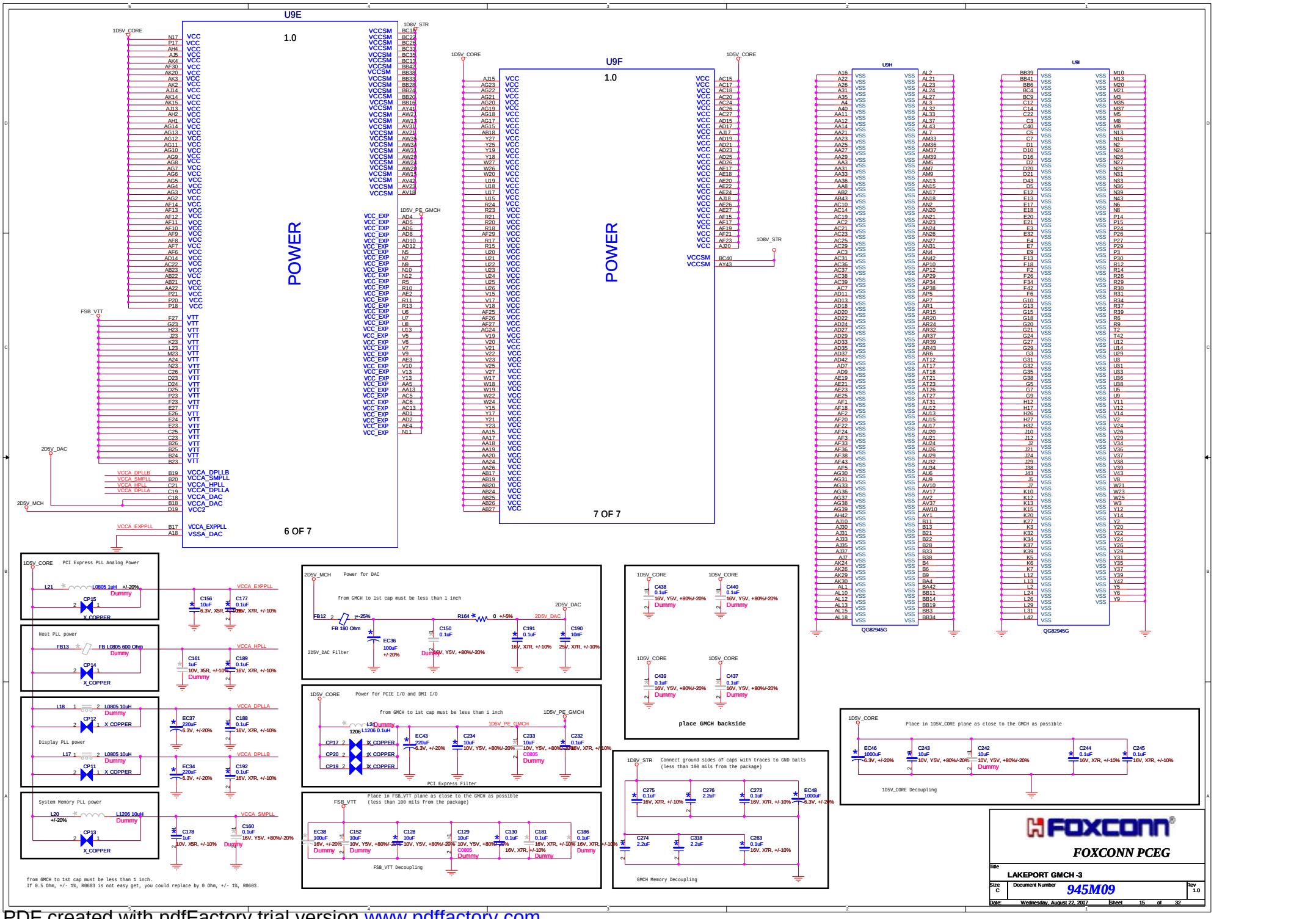

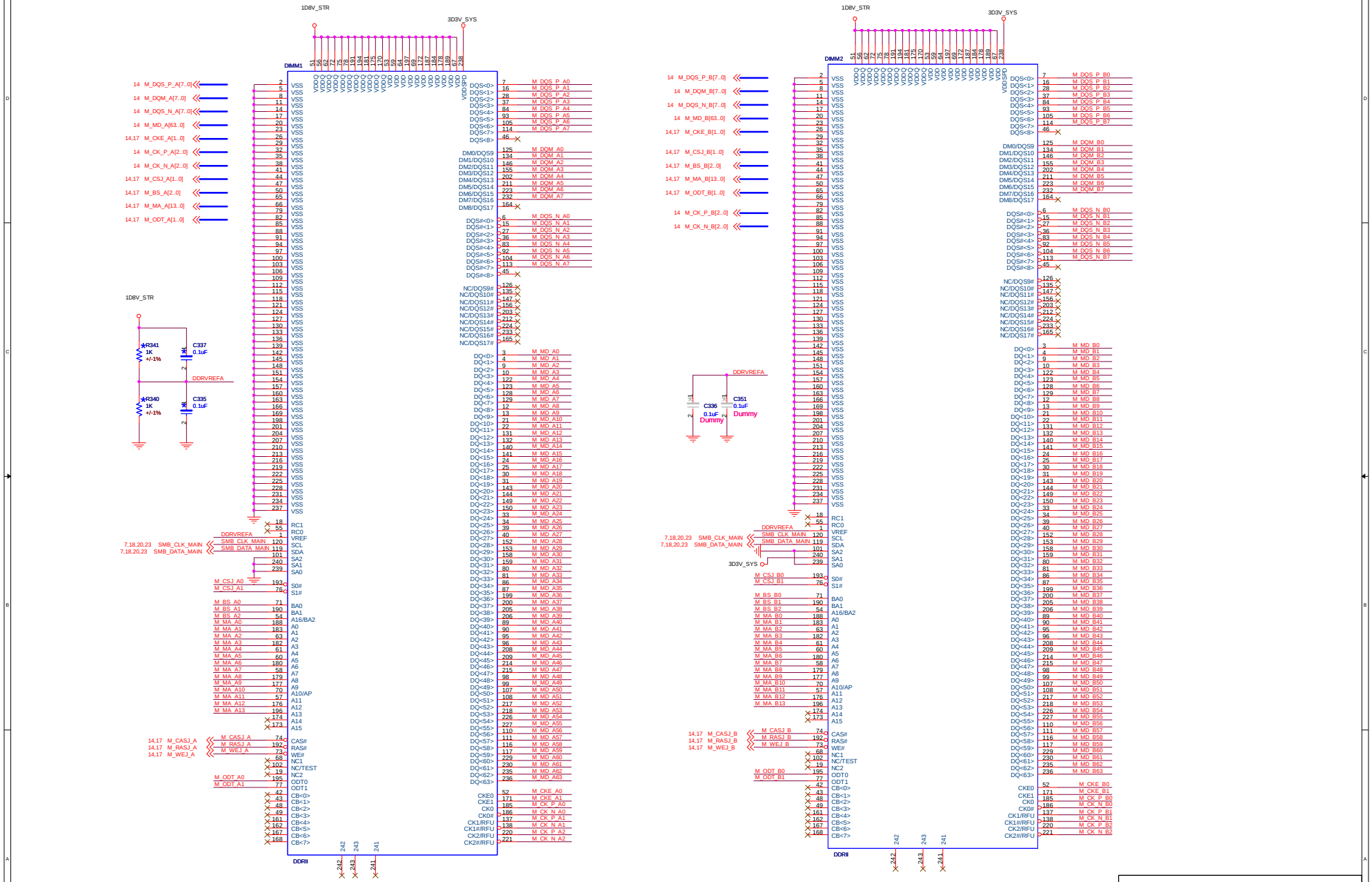

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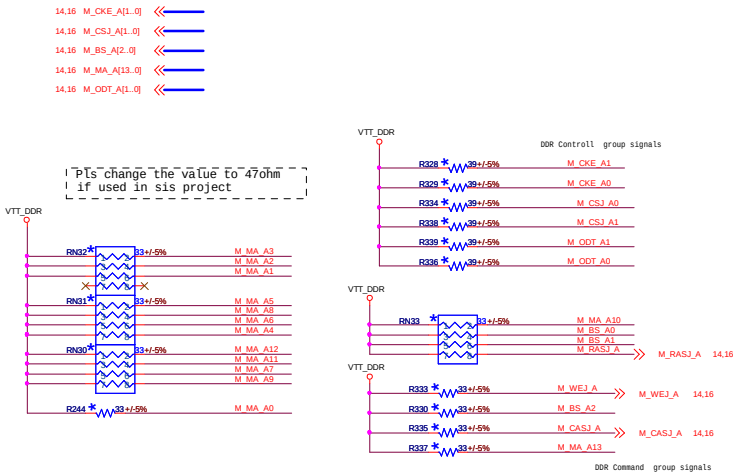
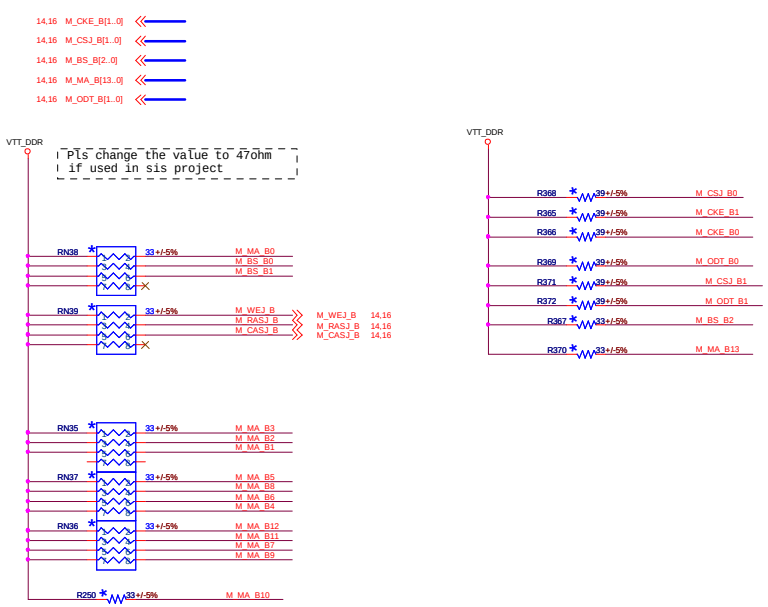
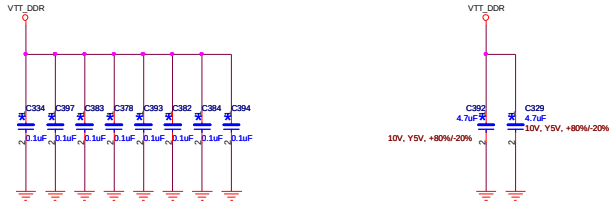
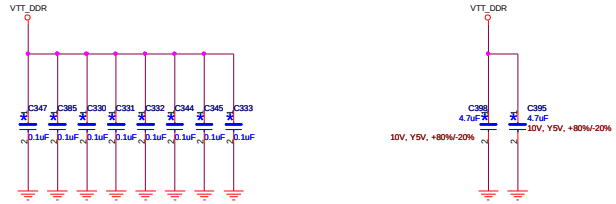
channel A

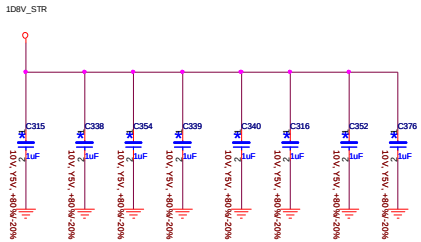
channel B

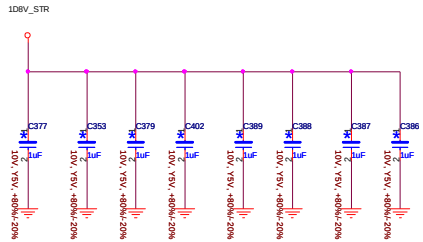












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Title: DDRII A & B Term

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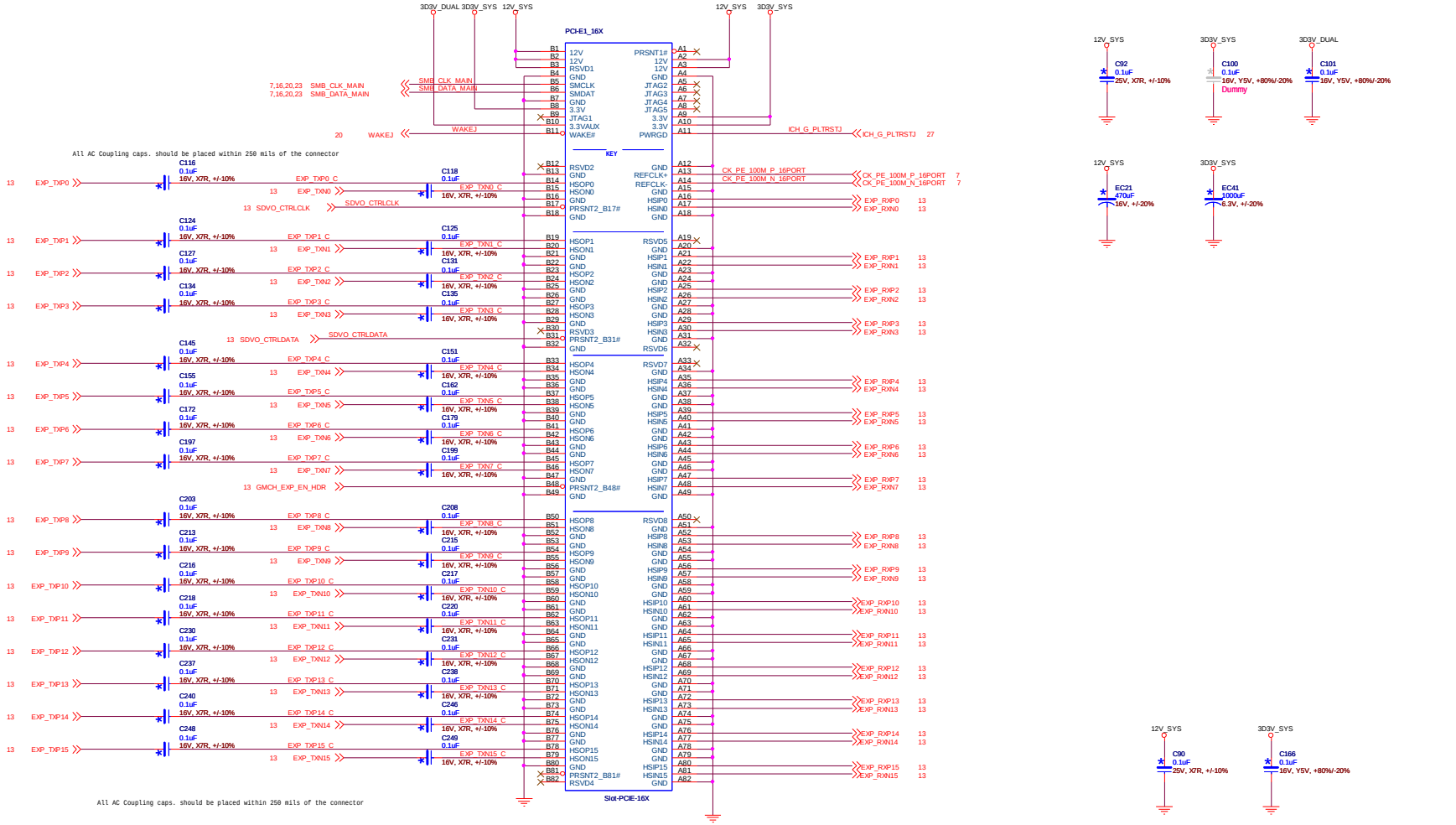

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Title: PCI Express x16 Gfx Slot

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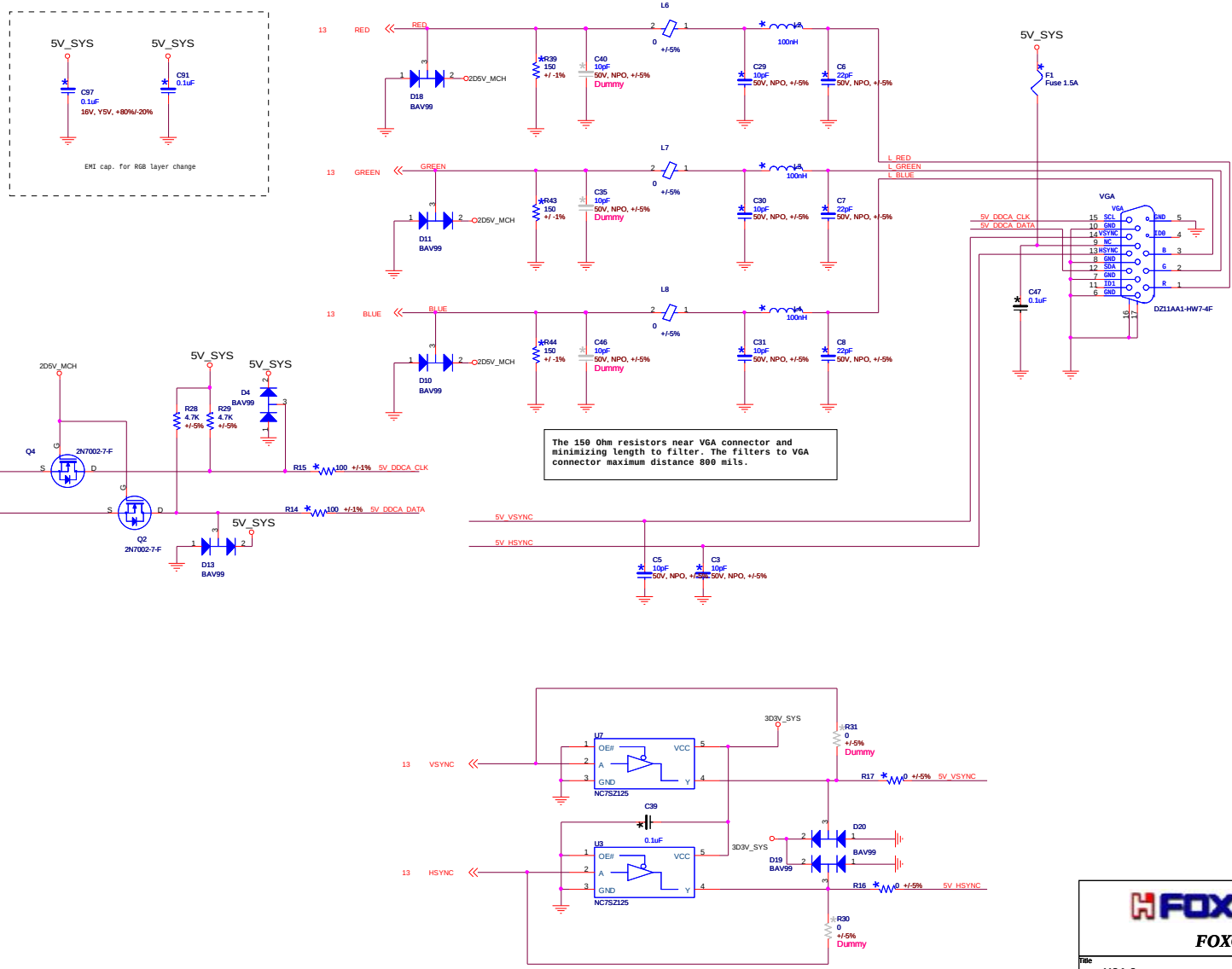
RGB routing
1. from GMCH to the first 150 ohm resistor: 12 mils(min. 6 mils spacing)
2. from the first 150 ohm res. to the second 150 ohm resistor: 7 mils
3. from the second 150 ohm resistor to connector: 4 mils
4. spacing minimum 6 mils, 30 mils spacing is recommended
5. R,G,B should be length matched to 200 mils, max. length is 8400 mils
6. R,G,B signals should be ground referenced



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Title	VGA Connector	
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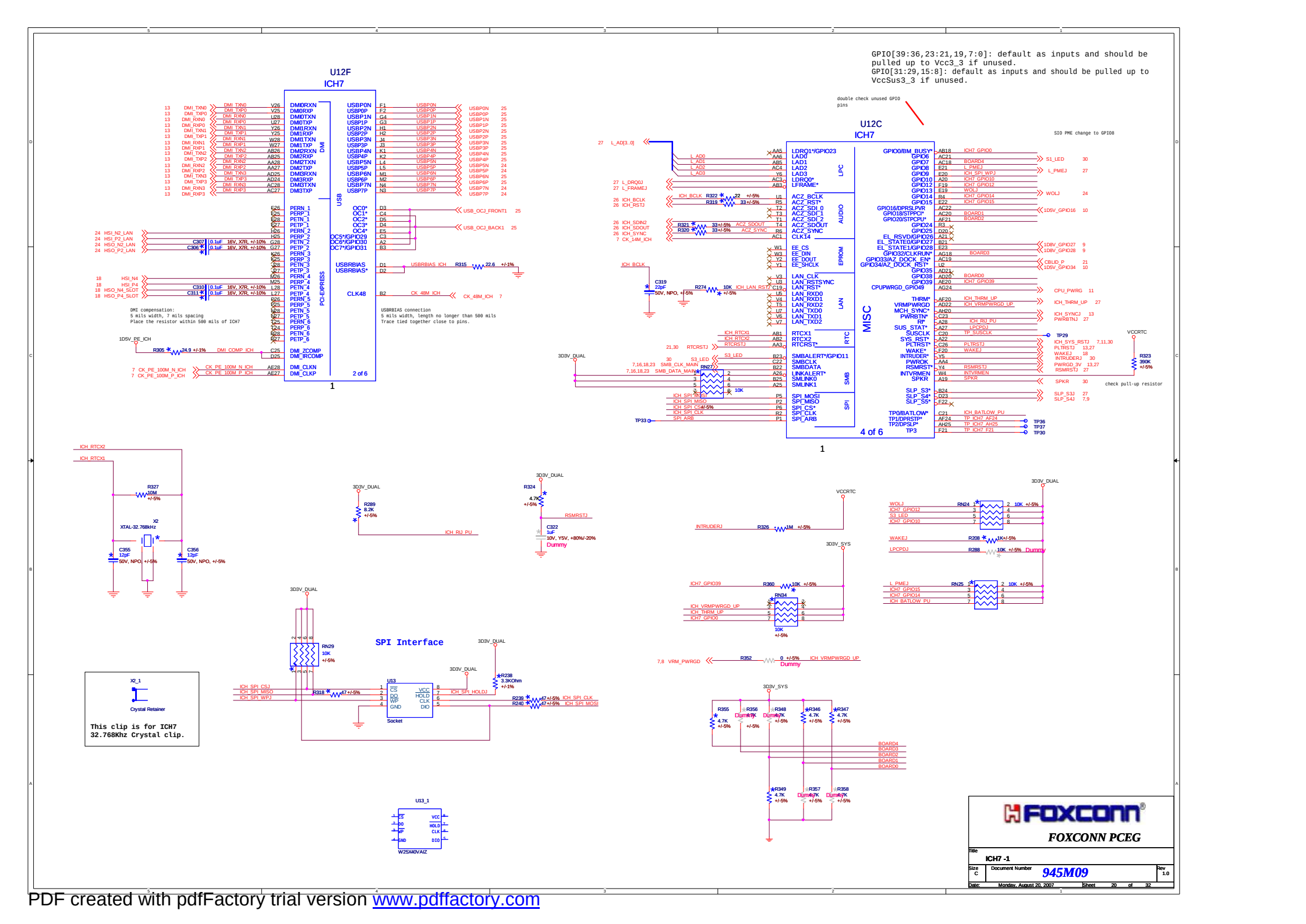
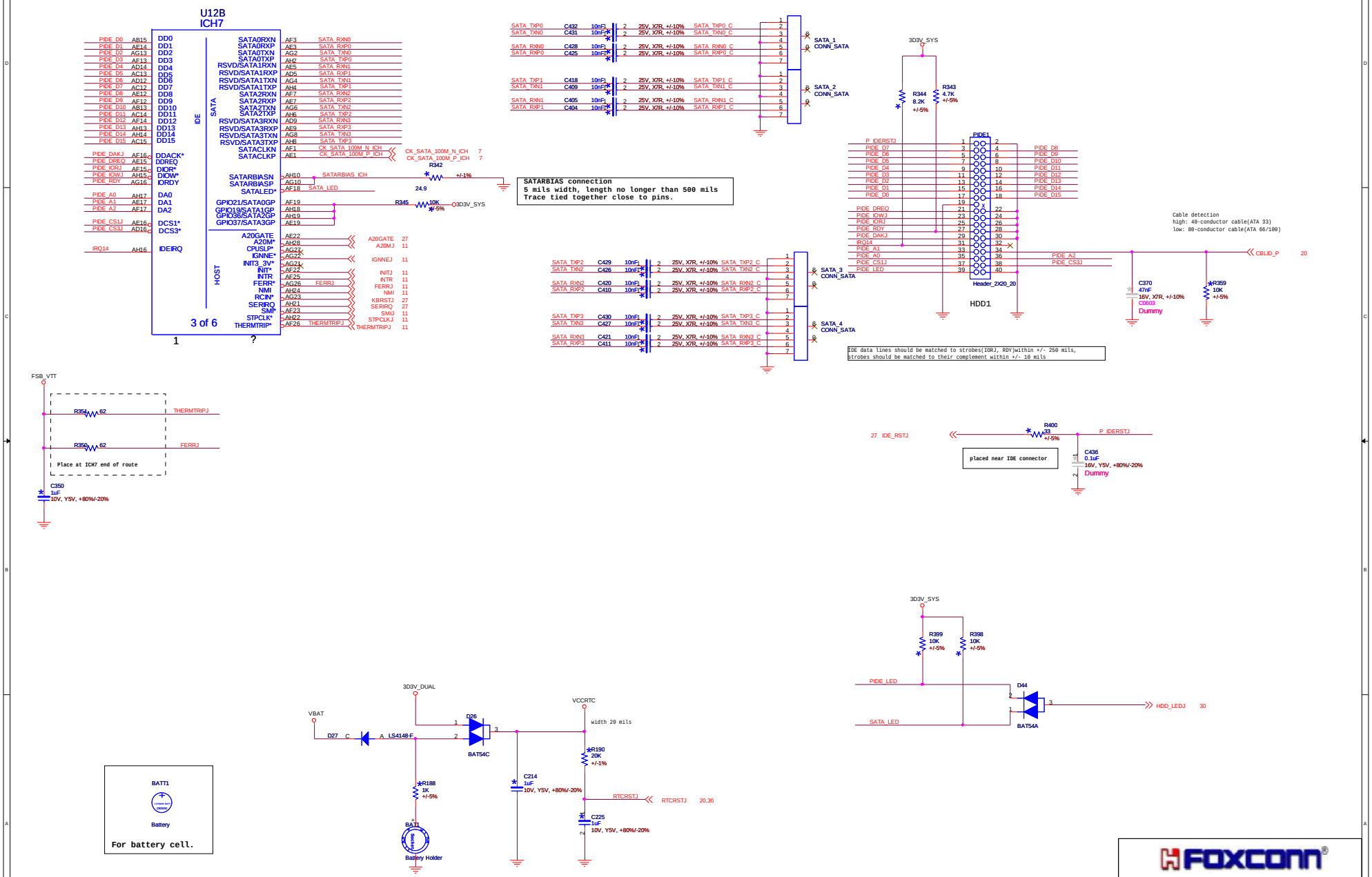
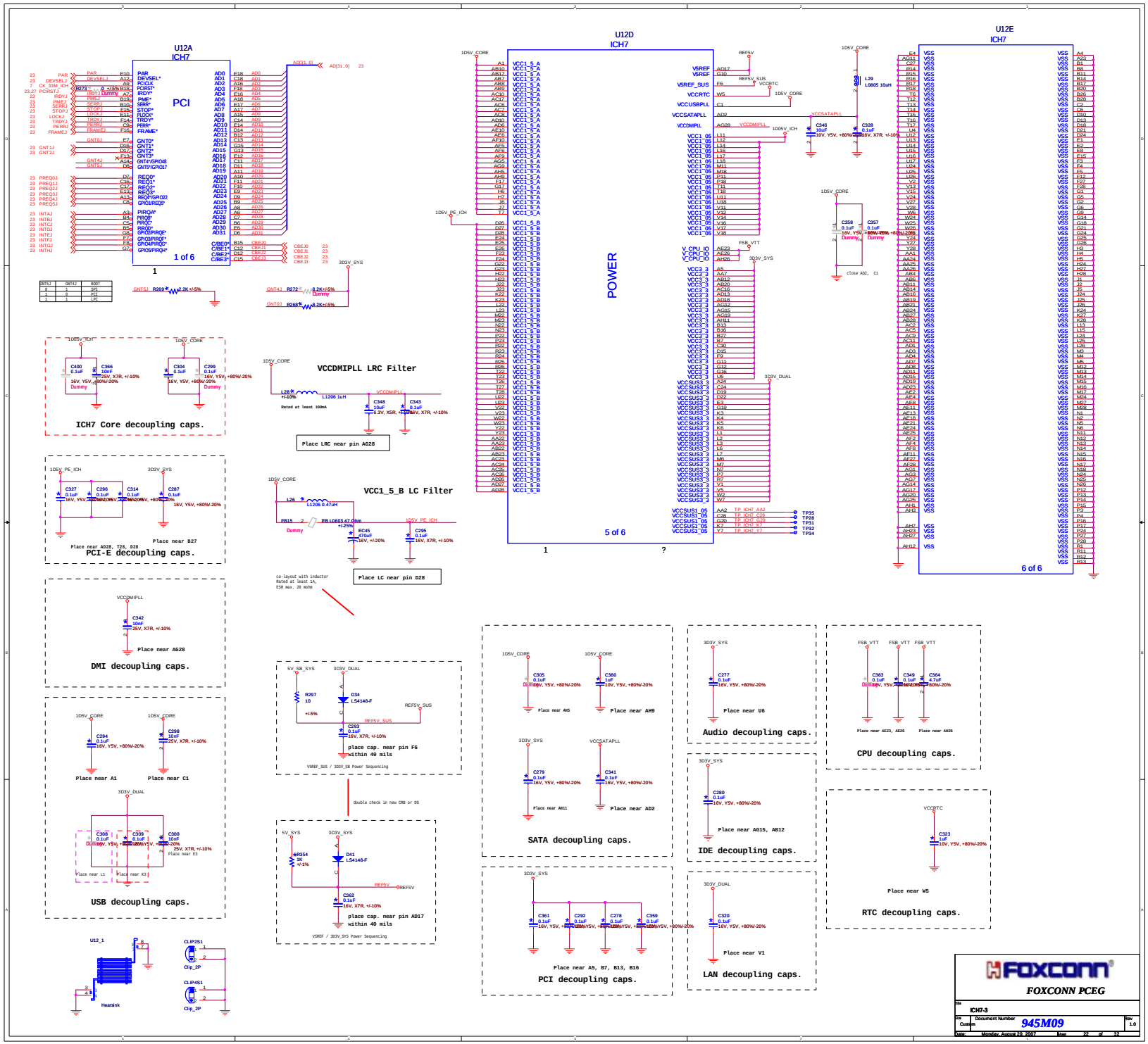
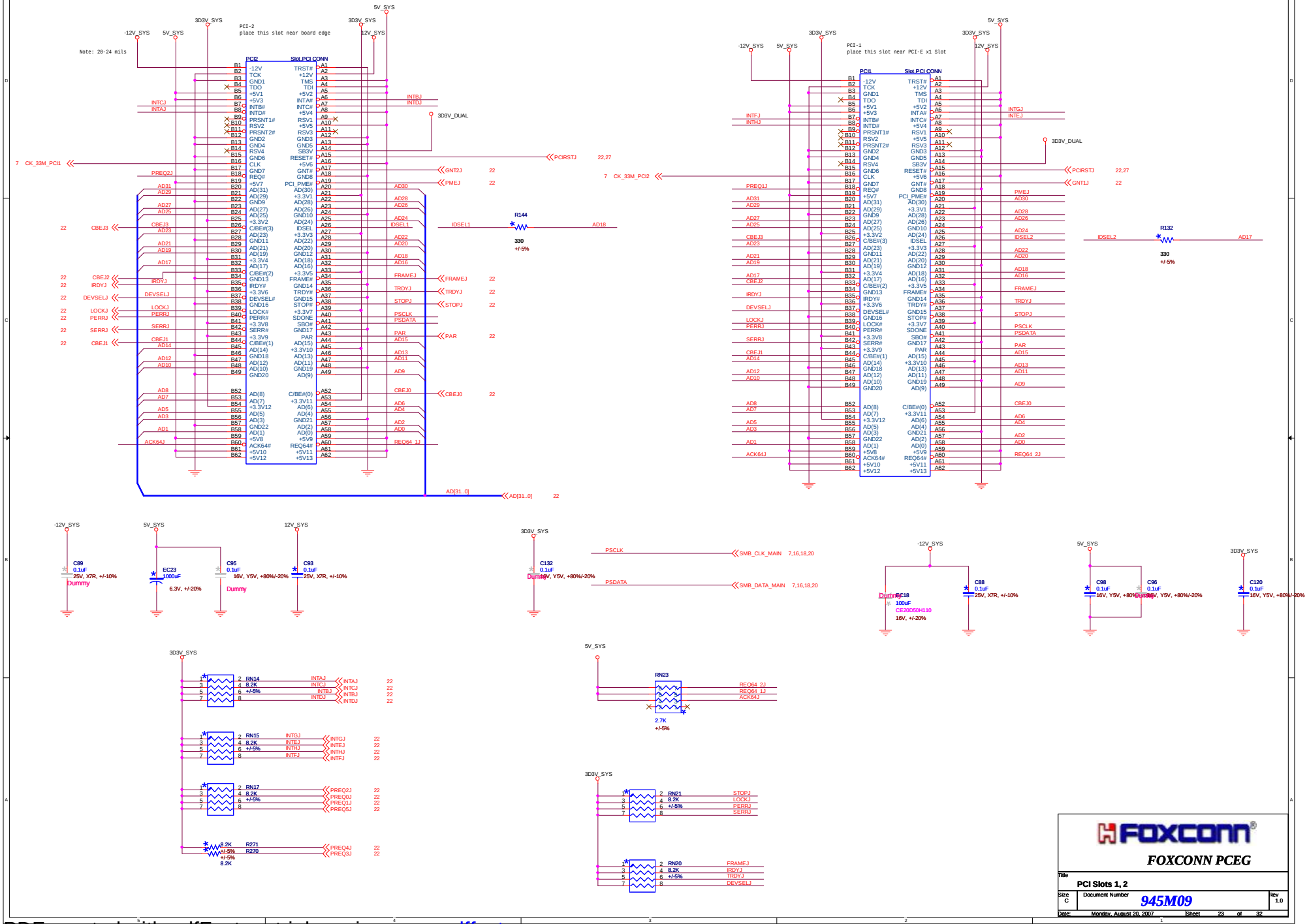
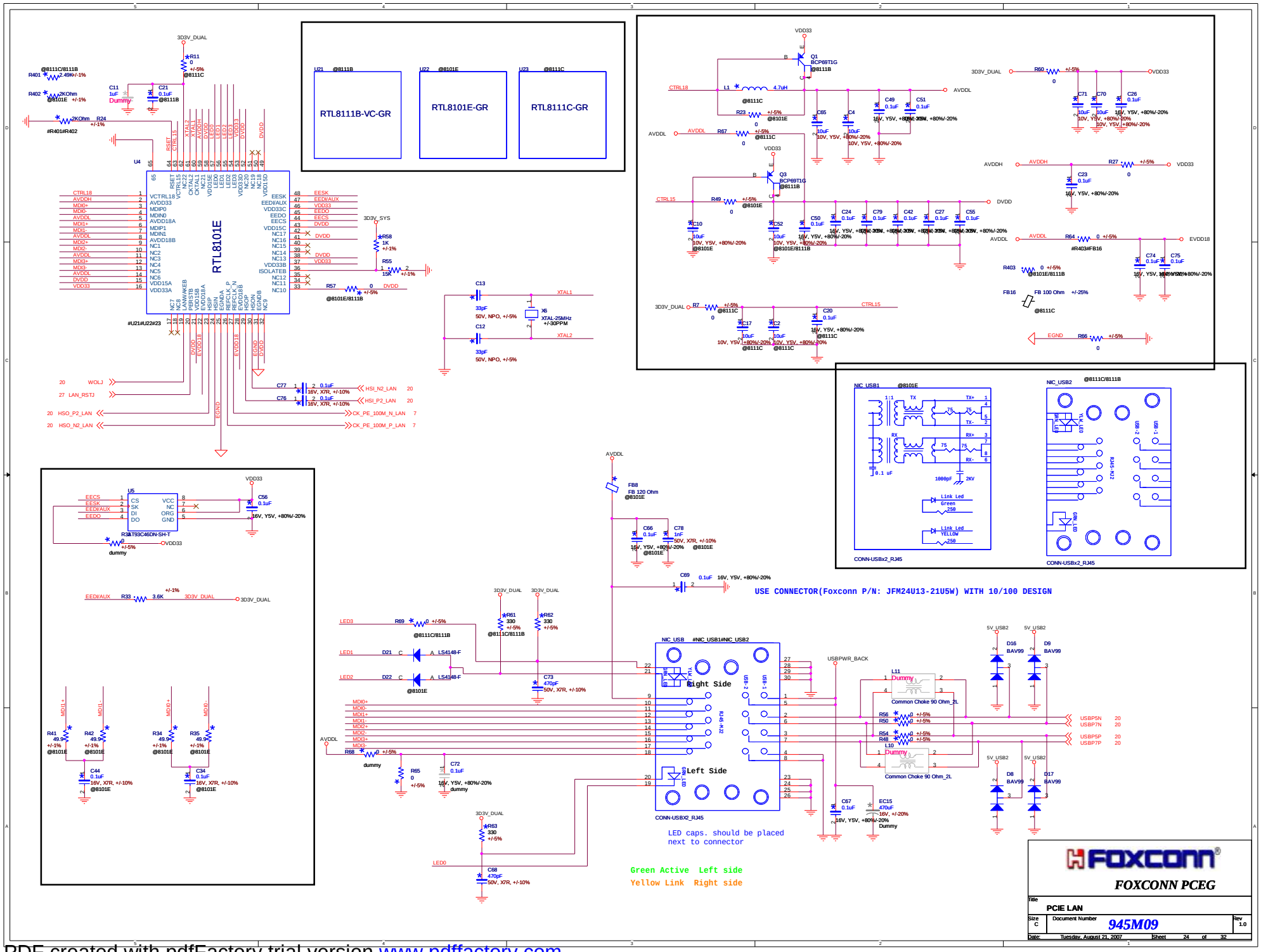


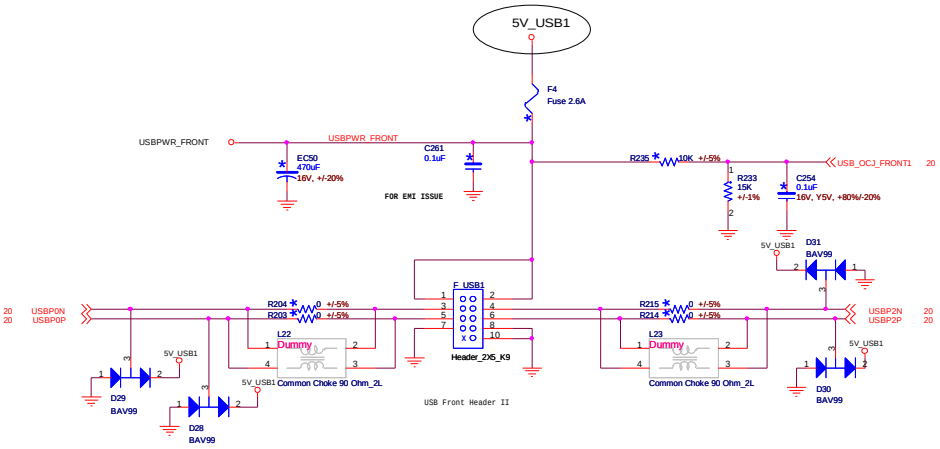




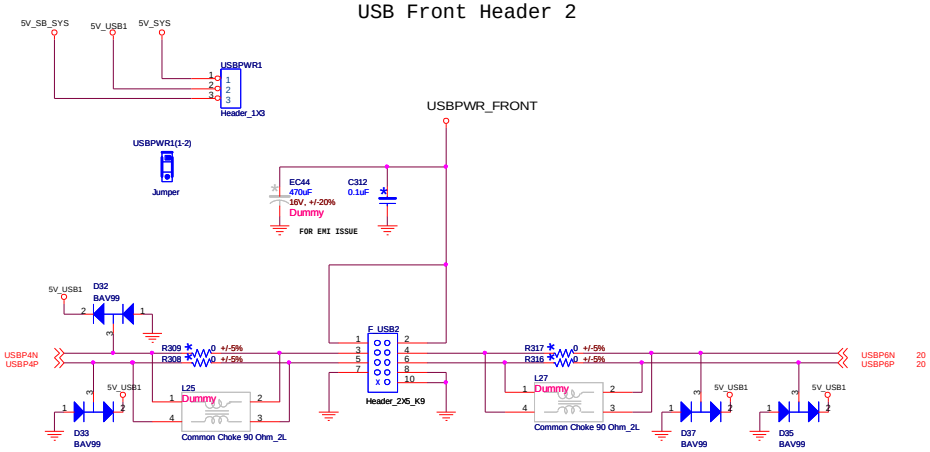




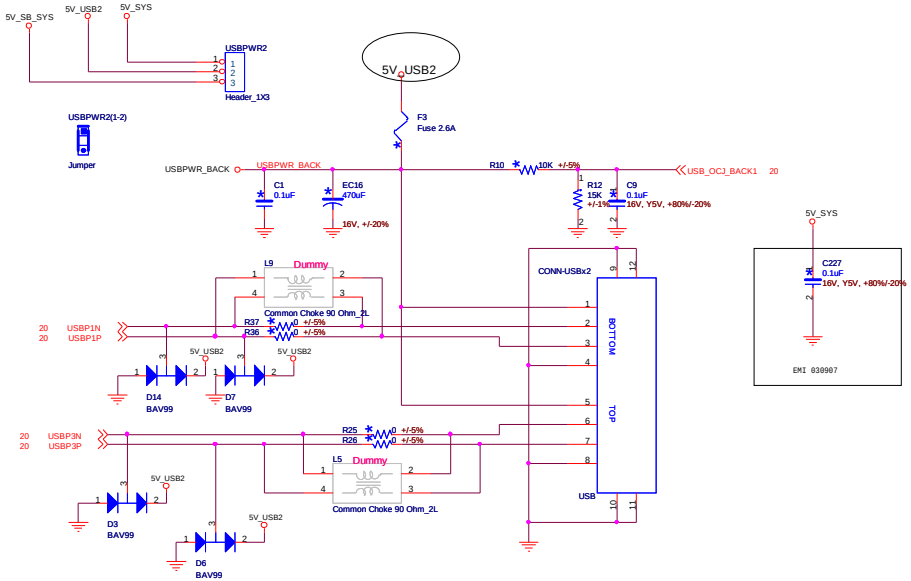
USB Front Header 1

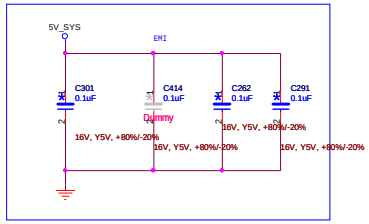


USB Front Header 2



Rear Dual USB Connector





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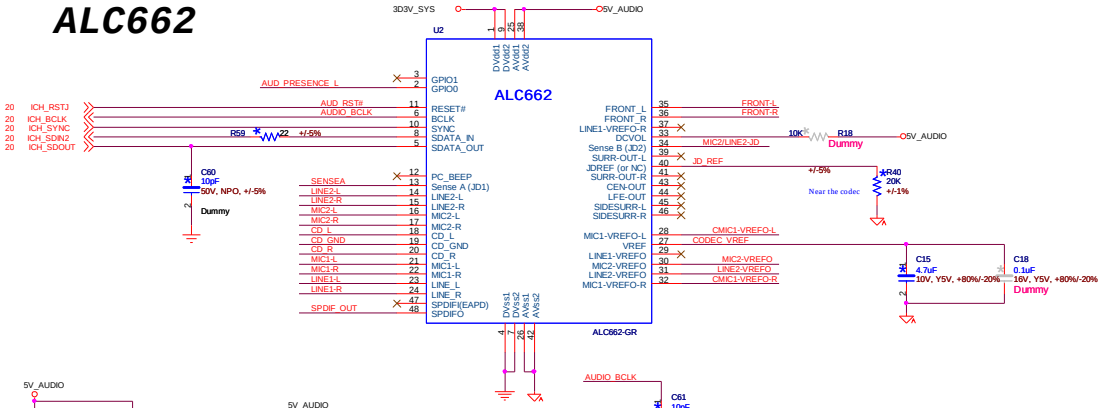
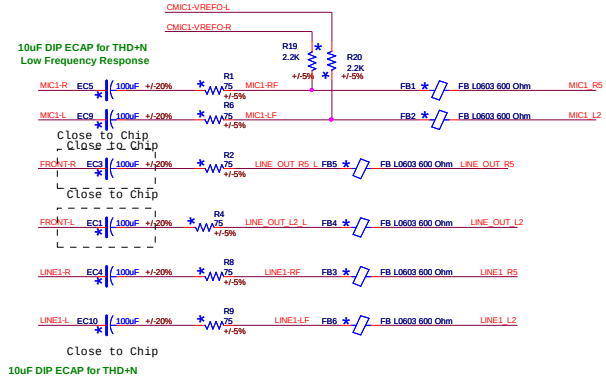
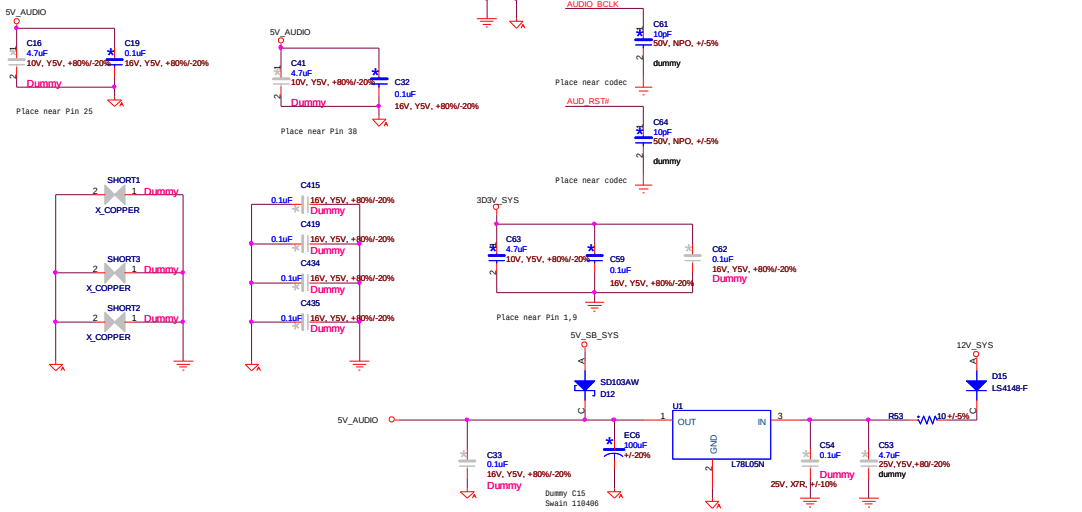
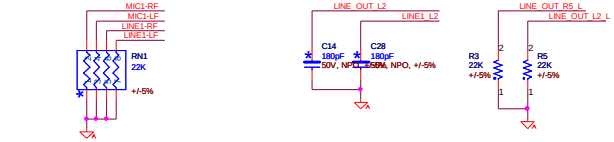
ALC662



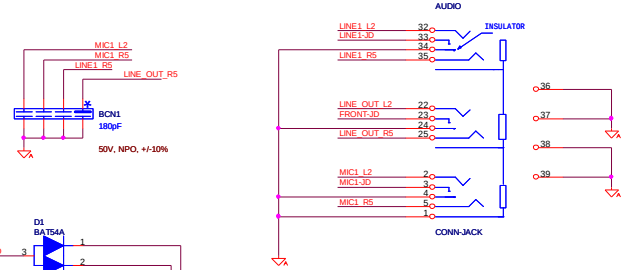
Rear AUDIO



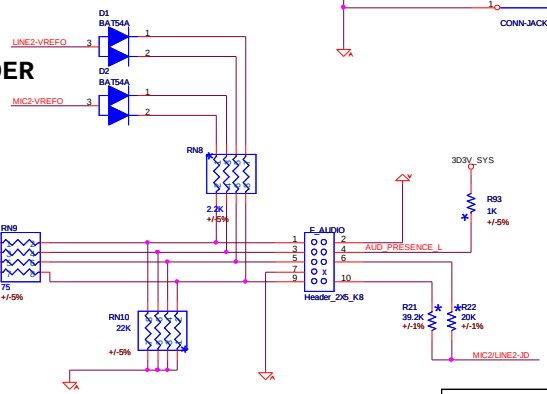




12V to 5V Power Regulator



FRONT AUDIO HEADER



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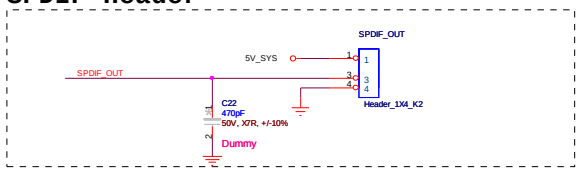
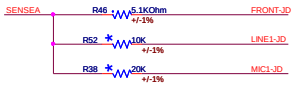


All JD resistors should be placed near CODEC



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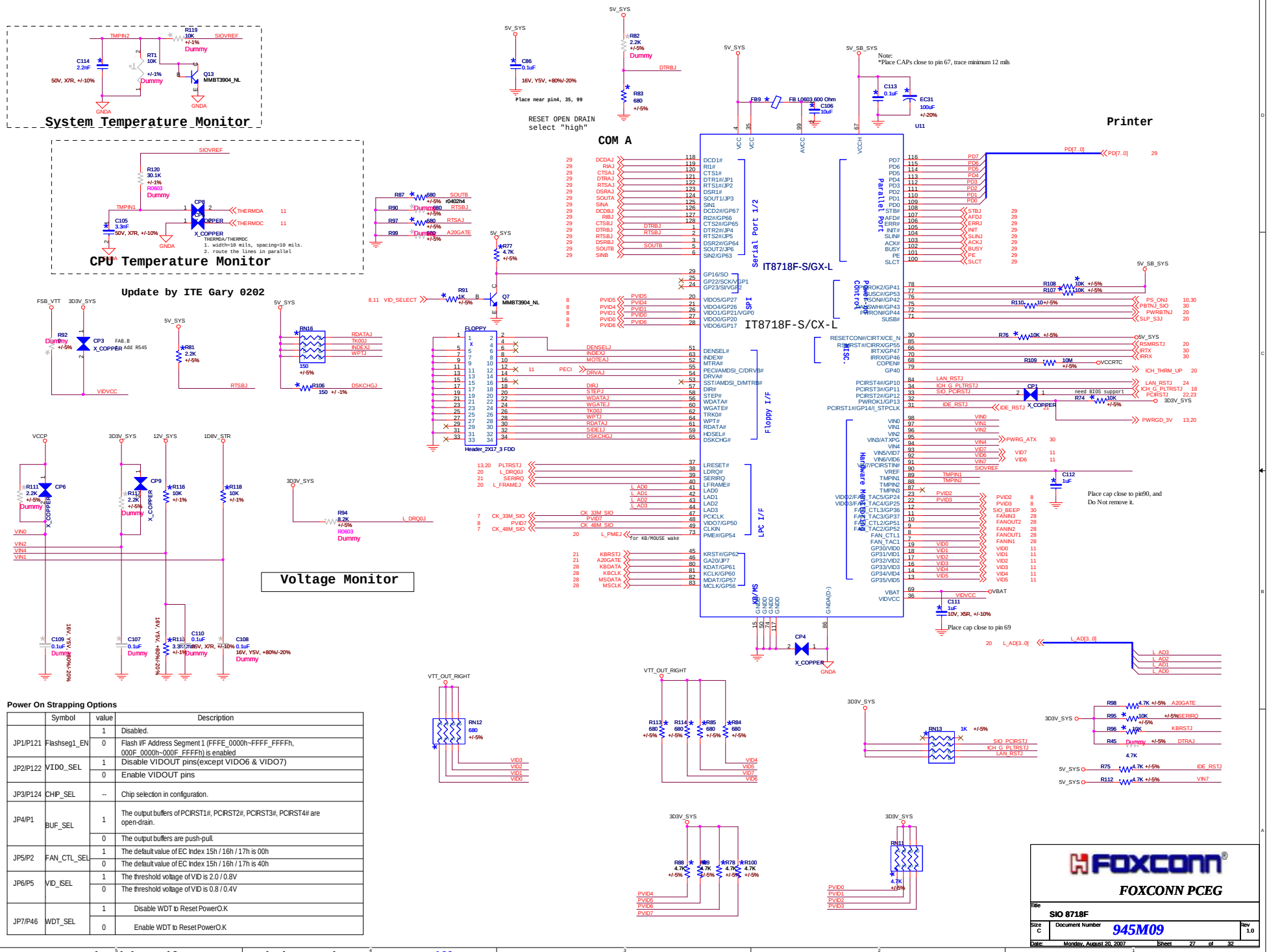
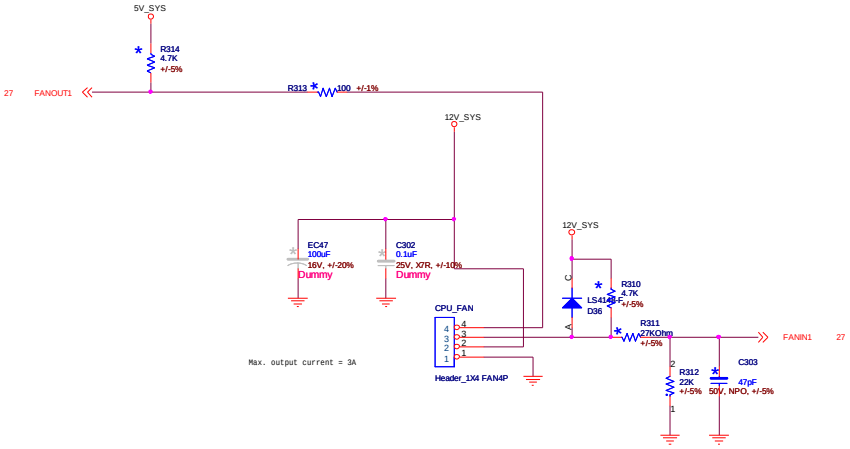


Power On Strapping Options

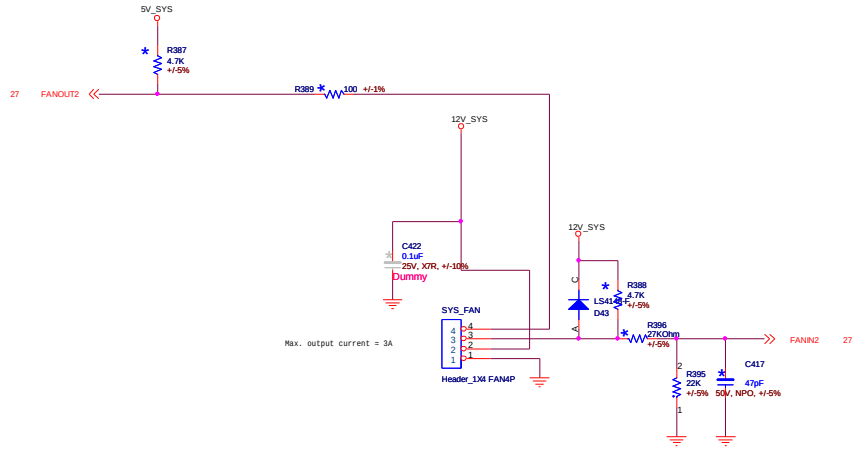
	Symbol	value	Description
JP1/P121	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFFE_0000h~FFFF_FFFFh, 000F_0000h~000F_FFFFh) is enabled
JP2/P122	VIDO_SEL	1	Disable VIDOUT pins(except VIDO6 & VIDO7)
		0	Enable VIDOUT pins
JP3/P124	CHIP_SEL	--	Chip selection in configuration.
JP4/P1	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# are open-drain.
		0	The output buffers are push-pull.
JP5/P2	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6/P5	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V
JP7/P46	WDT_SEL	1	Disable WDT to Reset PowerO.K
		0	Enable WDT to Reset PowerO.K

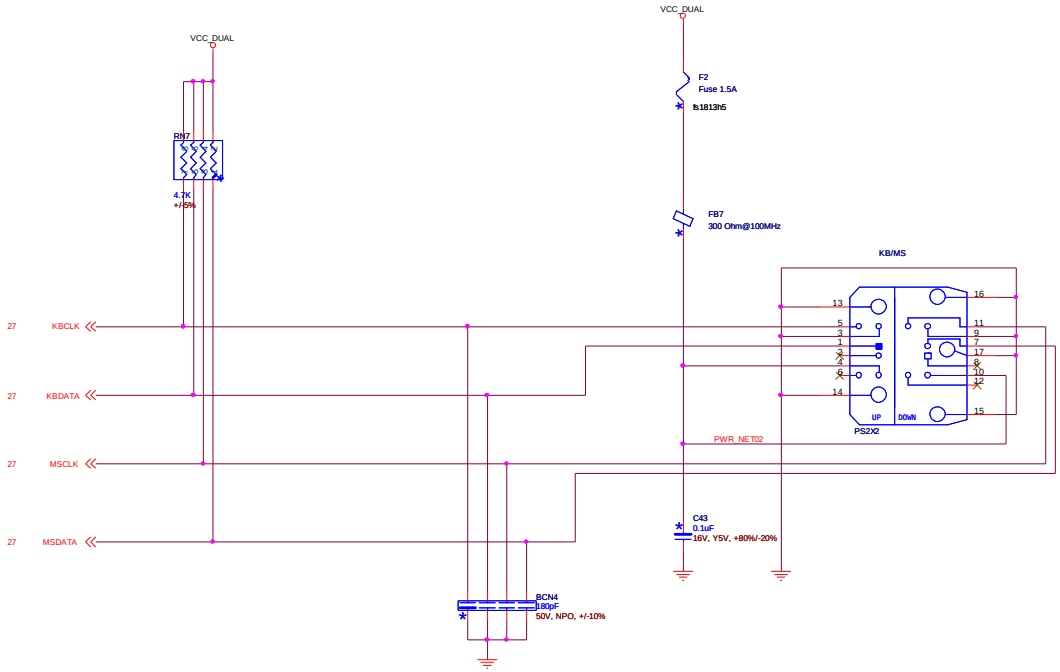
Peak fan current draw: 1.5A
Average fan current draw: 1.1A
Fan start-up current draw: 2.2A
Fan start-up current draw maximum duration: 1.0 second
Fan header voltage: 12V +/- 10%

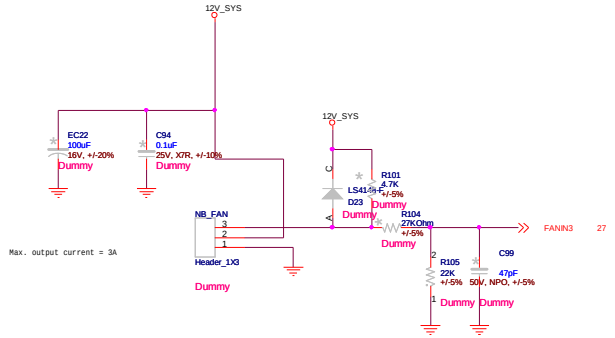
CPU FAN



System FAN







FOXCONN PCEG

Title: Keyboard / Mouse / Fan

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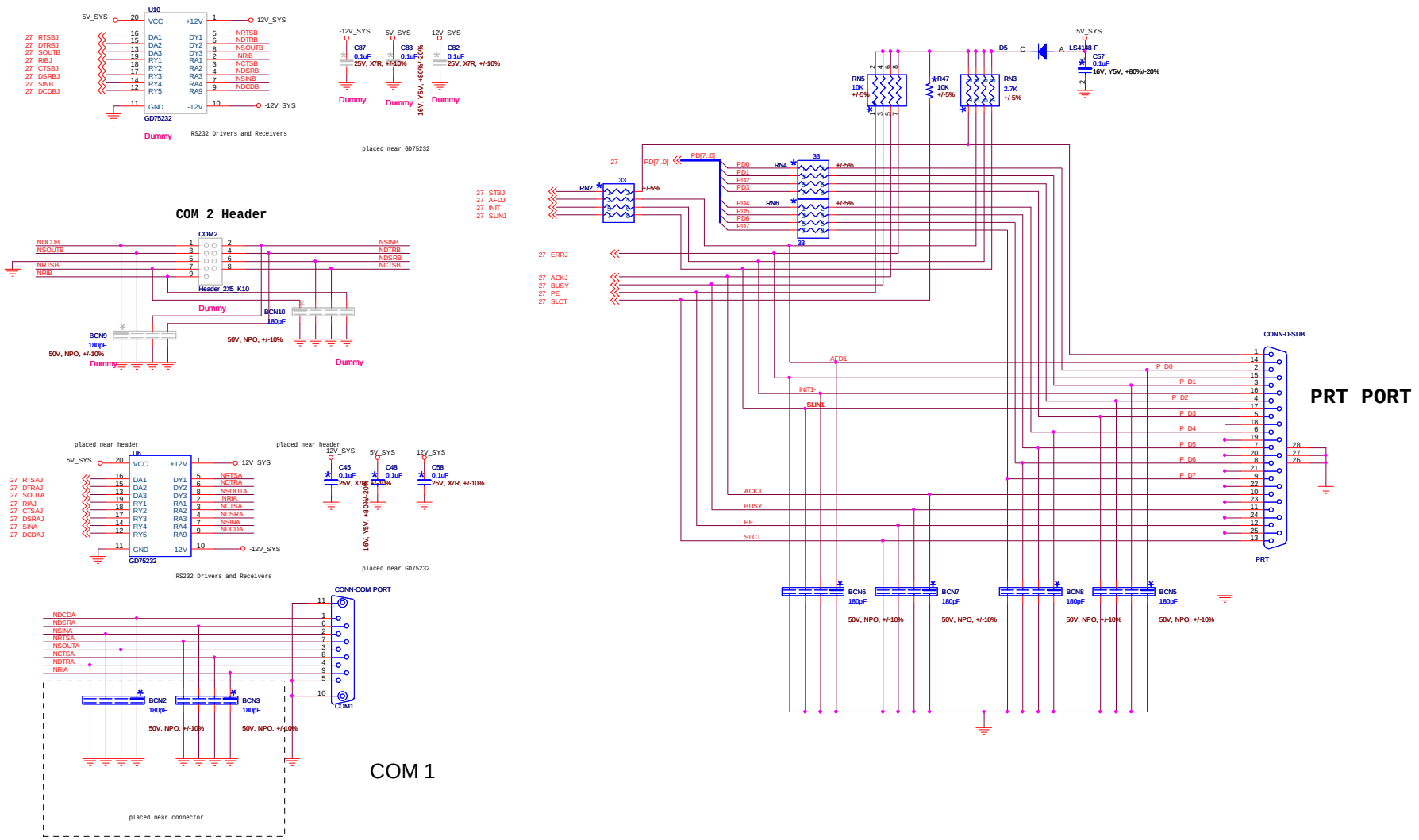

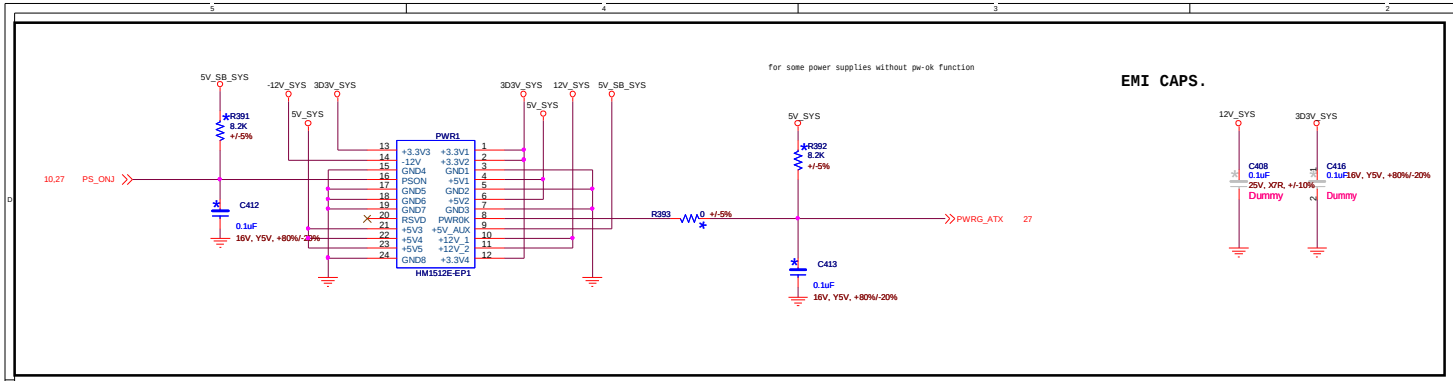

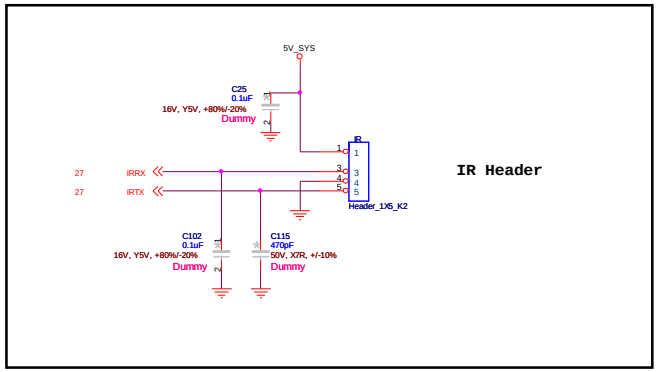

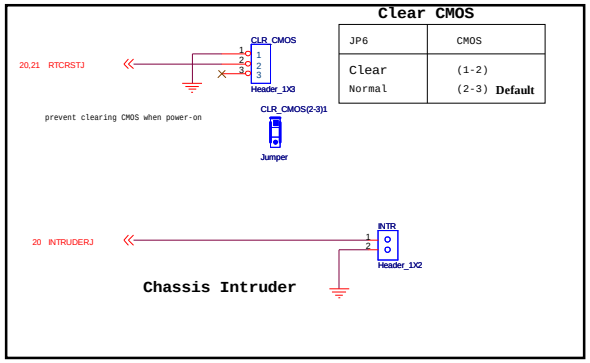

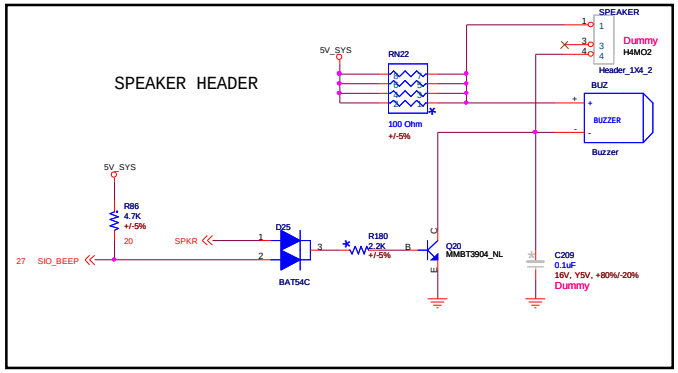

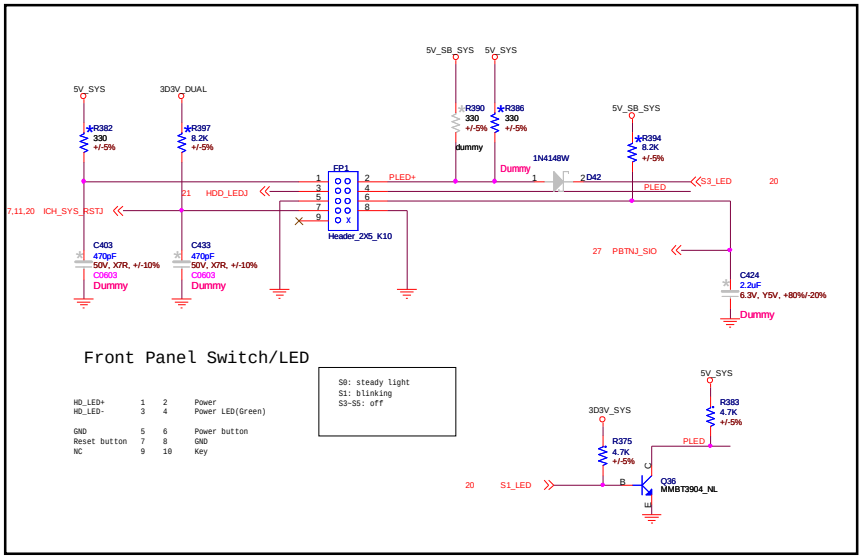

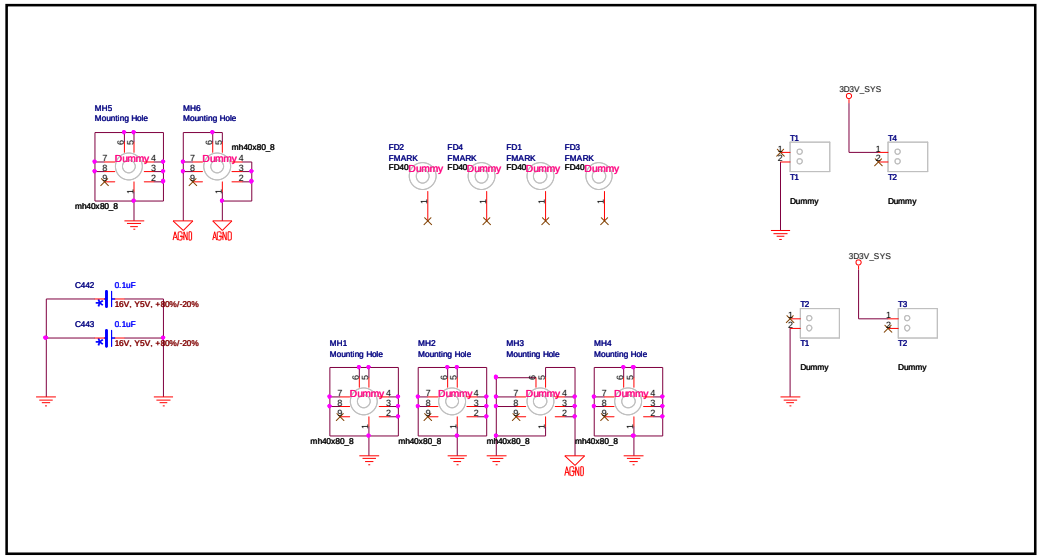

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Title	Power / MISC Connector	
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ICH7 GPIO Summary

Name	Power Well	Type	Description
GPIO0	Vcc3_3	I/O	Pull-up through 10K resistor(Unused)
GPIO1	V5REF	I/O	REQ_5#
GPIO2	V5REF	I/OD	PIRQE#
GPIO3	V5REF	I/OD	PIRQF#
GPIO4	V5REF	I/OD	PIRQG#
GPIO5	V5REF	I/OD	PIRQH#
GPIO6	Vcc3_3	I/O	1D5V Over voltage
GPIO7	Vcc3_3	I/O	1D5V Over voltage
GPIO8	VccSus3_3	I/O	L_PMEJ
GPIO9	VccSus3_3	I/O	DDR 1.8V Over voltage
GPIO10	VccSus3_3	I/O	DDR 1.8V Over voltage
GPIO11	VccSus3_3	I/O	Pull-up through 10K resistor(Unused)
GPIO12	VccSus3_3	I/O	DDR 1.8V Over voltage
GPIO13	VccSus3_3	I/O	Wake On LAN
GPIO14	VccSus3_3	I/O	Pull-up through 10K resistor(Unused)
GPIO15	VccSus3_3	I/O	DDR 1.8V Over voltage
GPIO16	Vcc3_3	I/O	BOAD ID 0
GPIO17	Vcc3_3	I/O	GNT_5#
GPIO18	Vcc3_3	I/O	BOAD ID 1
GPIO19	Vcc3_3	I/O	SATA_1GP
GPIO20	Vcc3_3	I/O	BOAD ID 2
GPIO21	Vcc3_3	I/O	SATA_0GP
GPIO22	Vcc3_3	I/O	REQ_4#
GPIO23	Vcc3_3	I/O	Pull-up through 10K resistor(Unused)
GPIO24	VccSus3_3	I/O	(Unused)
GPIO25	VccSus3_3	I/O	(Unused)
GPIO26	VccSus3_3	I/O	Pull-up through 10K resistor(Unused)
GPIO27	VccSus3_3	I/O	Pull-up through 10K resistor(Unused)
GPIO28	VccSus3_3	I/O	Pull-up through 10K resistor(Unused)
GPIO29	VccSus3_3	I/O	USB OC5#
GPIO30	VccSus3_3	I/O	USB OC6#
GPIO31	VccSus3_3	I/O	USB OC7#
GPIO32	Vcc3_3	I/O	BOAD ID 3
GPIO33	Vcc3_3	I/O	IDE1 Cable Detection(33 or 66/100)
GPIO34	Vcc3_3	I/O	BOAD ID 4
GPIO35	Vcc3_3	I/O	(Unused)
GPIO36	Vcc3_3	I/O	SATA_2GP
GPIO37	Vcc3_3	I/O	SATA_3GP
GPIO38	Vcc3_3	I/O	FWH_TBLJ
GPIO39	VccSus3_3	I/O	Pull-up through 10K resistor(Unused)
GPIO40	N/A	N/A	Not Implemented
GPIO41	N/A	N/A	Not Implemented
GPIO42	N/A	N/A	Not Implemented
GPIO43	N/A	N/A	Not Implemented
GPIO44	N/A	N/A	Not Implemented
GPIO45	N/A	N/A	Not Implemented
GPIO46	N/A	N/A	Not Implemented
GPIO47	N/A	N/A	Not Implemented
GPIO48	Vcc3_3	I/O	GNT_4#
GPIO49	V_CPU_IO	I/O	CPU_PWRGD

Super I/O GPIO Summary

Name	Power Plane	Type	Description
GPIO16	SUS	I/O	VID select
GPIO22	SUS	I/O	S1 LED
GPIO23	SUS	I/O	S3 LED
GPIO10	SUS	I/O	ICH THRM UP
GPIO36	SUS	I/O	Fan 3pin/4pin Det
GPIO37	MAIN	I/O	SIO BEEP
		I/O	
		I/O	
		I/O	

PCI Routing Summary

	PCI1	PCI2		LAN		
INTAJ	D		C	A		
INTBJ	A		D			
INTCJ	B		A			
INTDJ	C		B			
INTEJ		C				
INTFJ		B				
INTGJ		A				
INTHJ		D				
REG#/GNT#	2	1	0	3		
IDSEL	18	17	21	19		

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Title: GPIO / IRQ / IDSEL Map

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Modify list

1. Update clockgen PWRGD circuit(by connecting directly to VRM_PWRGD)
2. Delete TPM 33M CLK(delete C26,delete RN19 pin5,6 net)
3. Delete CPU PWRGD Pull high Resistor
4. Update ESD DIODE net(change D10,D11,D13,D12 Pin3 net)
5. Add level shift for HSYNC/VSYNC(change U10,U11,R252,R255 from dummy to reserved
   change R241,R242 from reserved to dummy)
6. GPIO update(change GPIO7 from 1D5V_CTL to Board_ID,change GPIO9 from 1D8V_CTL to SPI_WP
   change GPIO10/12 from 1D8V_CTL to unused,change GPIO16 from Board_ID to 1D5V_CTL,change
   GPIO27 from unused to 1D8V_CTL,change GPIO28 from SPI_WP to 1D8V_CTL,Change GPIO34 from
   Board_ID to 1D5V_CTL,change GPIO38 from 1D5V_CTL to Board_ID;delete R262,R264,R322,R329
7. Update RSMRST# circuit(delete R320,U23,U24,R332;change R380 from dummy to reserved)
8. Delete SPI_WP header(delete WP,WP_EN)
9. Delete TPM(detele total page,remove others to page30)
10. LAN IC change from PCI LAN(8110C) to PCIE LAN8101E)
11. Add 75ohm resistor(add R410,R413,R374,R404,change R367,R368 from 0ohm to 75ohm
12. Add 22K resistor(change RN25 from dummy to reserved)
13. Update Front audio auto detect
14. Delete 1D5V VIN(delete R410,CP7,C415,add R423)
15. Delete CIR(delete R321)
16. Delete CIR
17. Change C1075,C1082,C1077,C1074,C1078,C1080,C1081,C1083 footprint
    from 1206 to 0805
18. Delete dummy ECAP EC32
19. Change R308 from 0ohm to 1K
20. Delete C92
21. Delete R327 and add capcitors C109(Dummy) and C111(for 8111B)
22. change the value of EC2 and EC3 from 1500uF to 1800uF
23. Add FB17 for SIO pin 99
24. Add EMI CAP
25. Add R456,R446 for EMI
26. Add R244 ,R250
27. Delete C430,C319,C365,C367

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Title: Modify List		
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