Design and FPGA Implementation of Flexible and Efficiency Digital Down Converter

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Abstract—**Digital down converter (DDC) is the one of the key technologies in the field of software define radio (SDA). Compared with traditional ASIC DDC devices, DDCs implemented by FPGA have more flexible frequency and phase characteristics and higher precision computation. The paper designed and implemented DDC with above advantages on Xilinx FPGA Virtex-5. Through analyzing the key points of DDC theory and MATLAB simulation analysis, DDC with across clock region and FIFO interface characteristics is designed using Xilinx ISE. Some important and practical implementation details are given in this paper. And finally presents one application of DDC in communication systems by the portions given in this document.**

Keyword; FPGA;Digital Down Converter; Flexible;

I. INTRODUCTION

As the trend in Software Defined Radio(SDR)communications systems moving the digital part towards the antenna, more and more digital signal processing under FPGA or DSP devices are replacing the analogue components of the transmitter or receiver. DDCs, as the first stage of an all-digital intermediate frequency (IF) receiver, have become a cornerstone technology in communication systems. DDC is a technique that takes a band limited high sample rate digitized signal, mixes the signal to a lower frequency and reduces the sample rate while retaining all the information.[1][2]

Traditional ASIC-based DDC devices lack flexibility on right frequency and phases and have less performance in high precision computation. FPGAs can successfully solve these problems. With their inherent parallelism and the growing libraries of IP cores available, it is practical and efficient to design DDCs based on FPGAs, especially narrowband and high channel count DDCs. [3][4][5]

Taking advantage of design flexibility, high precision computing and system-level resource savings of FPGA, A high-efficiency DDC is designed in the paper. It shows, by means of a design example, which design parameters, influence the implementation results (resource consumption) of a DDC. Section 2 describes the theory of digital down converter. Section 3 details the design of the down converter and the results of MATLAB simulation. The implementation details on an FPGA device are given in Section 4. Its Application presents in Section 5 and, finally, the conclusions are summarized in Section 6.

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II. THEORY OF DDC

DDCs have become a cornerstone technology in communication systems. Similar to its analog receiver counterpart, the DDC provides the user with a means to tube and extract a frequency of interest from a broad radio spectrum. The DDC consists of a front end digital mixer, a digital filtering part and decimation section. Its block diagram is shown in Fig. 1.

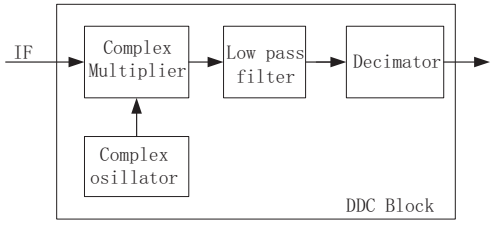

Figure 1. DDC block diagram

A. Digital Mixer

The first stage of the DDC is to mix, or multiply, this digitized stream of samples with a digitized cosine for the phase channel and a digitized sine for the quadrature channel and so generating the sum and difference frequency components. The amplitude spectrum of both phase and quadrature channels will be the same but the phase relationship of the spectral components is different. This phase relationship must be retained, which is why all the filters in the phase path must be identical to those in the quadrature path. Because we have quadrature signals the spectral components from both positive and negative frequencies can be overlaid, for non quadrature sampling the two frequency components would have o be kept separate and so requiring twice the bandwidth. A front end digital mixer performs a frequency translation to baseband. An Intermediate frequency A/D signal is moved to baseband after mixer. [6] Equation (1) and (2) describe such a process in frequency domain.

$$\cos(\omega_c t)\ x(t) \leftrightarrow 0.5\ \mathrm{X}\ X(\omega-\omega_c) + 0.5\ \mathrm{X}\ X(\omega+\omega_c) \quad (1)$$

$$sin(\omega_c t)\ x(t) \leftrightarrow 0.5\ \mathrm{X}\ X(\omega-\omega_c)j + 0.5\ \mathrm{X}\ X(\omega+\omega_c)j \quad (2)$$

B. Digital Filter

The function of digital filtering is to suppress both the image band signal due to frequency mixing and the noise residing in aliasing bands resulted from decimation and also to maximize the received signal-to-noise ratio (SNR). [7] The spectrum of both phase and quadrature signals can be filtered using identical digital filters, which with digital filters in an FPGA is not a problem. A digital filter frequency response is always symmetrical about 0.5Fs. The unwanted frequency components fall outside the pass bands of the filter.

C. Decimation

The sample frequency is now much higher than required for the maximum frequency in our frequency band and so the sample frequency can be reduced or decimated, without any loss of information.

Decimation is to reduce the sample rate. And its theory is expressed in (3) and (4).

$$y(n) = x(Mn) \quad n = -\infty \sim +\infty \tag{3}$$

$$Y(e^{j\omega}) = \frac{1}{M}\sum_{k=0}^{M-1} X(e^{j(\omega-2\pi k)/M}) \tag{4}$$

Where x(n) is input signal, M is decimator factor, y(n) is output signal after decimator.

The spectral of y(n) can be achieved through the following step conversion: (a) stretch $X(e^{j\omega})$ by a factor M to obtain$X(e^{j\omega/M})$, (b) create M-1 copies of this stretched version by shifting it uniformly in successive amounts of 2π, and (c) add all these shifted stretched versions to the unshifted stretched version $X(e^{j\omega/M})$, and divide by M and formed $Y(e^{j\omega})$. The stretched quantity $X(e^{j\omega/M})$ does not have period 2π, but after adding the shifted versions the result is periodic with period 2π. [8]

III. DEGIN OF DDC

The output from the DDC has retained all the information in our frequency band of interest but has moved it down to baseband and so allowed the sample frequency to be greatly reduced. This has the advantage of simplifying any further processing on the data, together with the gains of possibly time shared functions within the FPGA due to the lower clock frequency, so allowing more processing to be fitted into the FPGA, also the lower effective clock frequency will reduce the power requirement for the FPGA.

Here takes an example of a practical DDC design. Its main parameters are shown in table1. The key part of DDC design is to decide how many stages filters have and what their sampling rate factors are.

From table 1, we can see it is a narrowband DDC with decimation factor of 8. With the help of MATLAB analysis, it is impossible to design a required filter in such a narrowband system with 80Msps sample rate and 1MHz signal bandwidth, so multi-stage filter architecture is adopted. When there is a decimator or an interpolator with a large factor, it is usually wise to break up the filter into several multi-rate stages, each comprising a multiple of the total decimation/interpolation factor. Here the decimation factor is 8 less than 32; it is efficiently to design with a cascade of FIR filters instead of CIC filters. [9][10]

TABLE I. DDC MAIN PARAMETERS DESPCRIPTION

Main Parameters	**Description**
Input sample rate	80Msps
Decimation factor	8
Input /output data width	16
DDS output frequency	Programmable
DDS Frequency resolution	0.04Hz
Band Rejection	100dB
Output Clock	10MHz
Signal Bandwidth	1MHz
DDS Spurious Free Dynamic Range	100dB

To minimize resource utility in system level, here adopted 3-stage fir filter with 2 decimation factor of each stage. Such architecture is efficient verified in MATLAB. Fig. 2 shows individual magnitude response of 3-stage FIR. FIR1, FIR2 and FIR3 indicate the first-stage fir filter, the second-stage fir filter and the third-stage fir filter. The magnitude response after cascading is shown in Fig. 3. The main parameter comparison of 3-stage fir is shown in table2.It is easy to obtain the functional block diagram of DDC after fixing the architecture of digital filtering parts. It is show in Fig. 4.

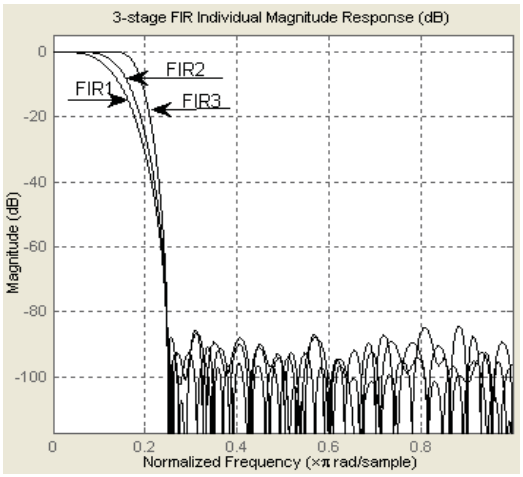

Figure 2. 3-stage FIR Individual Magnitude responses

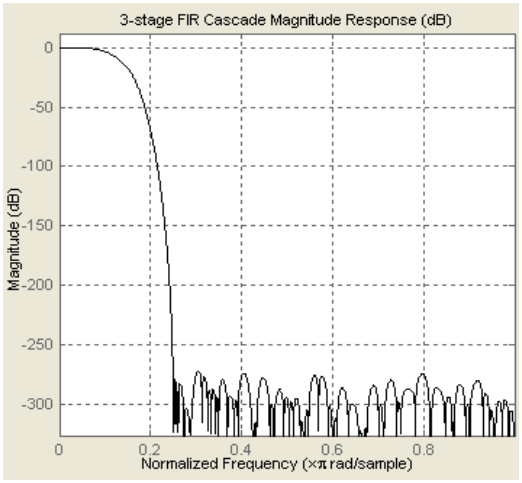

Figure 3. 3-stage FIR cascaded Magnitude responses

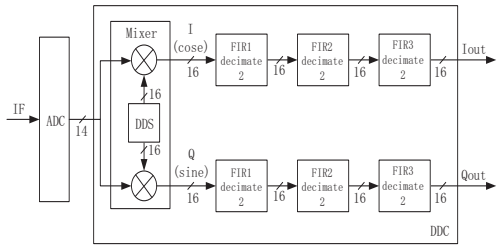

Figure 4. Single-channel DDC functional block diagram

TABLE II. 3-STAGE FIR INDIVIDUAL FILTER RESPONSES

Filter Parameter	FIR1	FIR2	FIR3
Fpass (MHz)	1.5	1.5	1.5
Fstop (MHz)	10	2.5	1.5
Frequency(MHz)	80	40	20
Taps	44	53	79

IV. IMPLEMENTATION BY FPGA

To understand how FPGAs play a key role in implementing DDCs and performing the function of a receiver, it's important to break the DDC down into its individual functional blocks. The DDC design is implemented on Xilinx FPGA SX95T with the software foundation series Xilinx ISE 11.2. [11]

A. DDS

DDS IP core is used to generate digitalized sine and cosine signal as local carrier. Here DDS we design has a programmable output frequency. Fig. 5 shows 9.76 KHz and 10 MHz frequency output respectively of DDS IP core with 80MHz of input clock. Please refer to reference [12] about DDS IP operation.

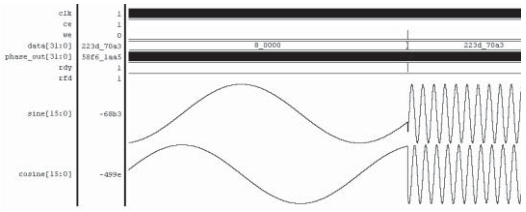

Figure 5. DDS different frequency output

B. Mutlistage FIR Filters

The 3-stage fir filters are realized by FIR IP core. [13] Multi rate and multistage filters realized in FPGA have two main advantages. The first advantage is that it can accelerate the computation rate because multistage filters can be easily pipelined. Fig. 6 shows the relationship of control signals in 3-stage FIR Filter. From it we can see the signal fir2_nd of the second fir filter is achieved by fir fir1_rdy & fir2_rfd; and the signal fir3_nd of the third fir filter is achieved by fir2_rdy & fir3_rfd. The pre-fix of fir1, fir2, fir3 delegate the first fir filter, the second filter and the third filter. The second advantage is that half of FPGA resources can be saved due to 3-stage fir filters have symmetry coefficients.

The filters here usually have linear phase characteristics. Linear phase filters are usually more complex than those with arbitrary phase characteristics, so once again, there is a good reason for this.

Communications systems often depend on the relationships between multiple carriers. These carriers may be the same frequency but with different phase; or they may be completely different frequencies. In either case, disturbing the phase relationships would be a bad thing.[2]

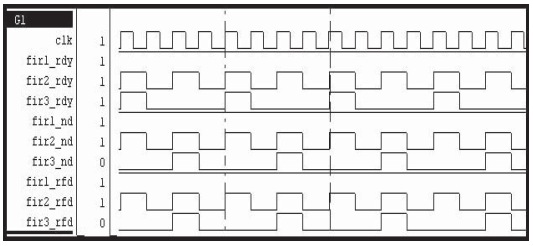

Figure 6. Relationship of control signals of 3-stage FIR Filter

C. Cross Clock Scope and FIFO Interface

The DDC design utilizes two clock scopes. FPGAs have global and regional clock resources. Regional clock works only in the scope of one bank. [14] The output clock of ADC is regional while one bank cannot place both ADC and DDC modules. So it is wise to design DDC across clock regions. For the convenience of users, the interface of DDC module is in FIFO form. That is, data from DDC module is transferred to a FIFO, which plays a role of forming the new data flow and sending them to the next processing unit.

D. Resource Consumption

Table 3 is DDC resource consumption on Virtex-5 SX95T FPGA device. Symmetry coefficients and the technique of pipeline of multistage fir filter have saved lot FPGA resources.

TABLE III. DDC RESOURCE CONSUMPTION ON VIRTEX-5

Slice logic Utilization	Quantity
Number of Used Slice Registers	10998
Number of Used Slice LUTs	5933
Number of Used Block RAM/FIFO	1
Number of Used DSP48Es	100

V. APPLICATION

This part describes an example of data flow in one DDC application. Figure7 shows it block diagram.

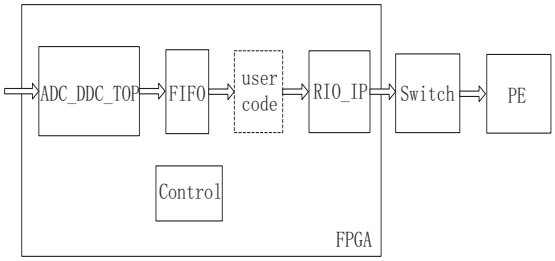

Figure 7. Data Flow of one DDC Application

In the application, DDC module and ADC module is packaged as the IP core name ADC_DDC_TOP in Figure7, that is, the ADC_DDC_TOP module is a black box. It is not necessary for further developers to know the internal architecture and implementation details of such a black box.

The module provides a FIFO interface for user to further develop their application in user code module shown in dashed box. The RIO_IP is short for RapidIO IP, whose function is packeting data and transferring to the next module. RapidIO is an open-standard, switched fabric designed by the leaders in embedded computing specifically for developers of wireless infrastructure, edge networking, storage, scientific, military and industrial equipment. It is out of the scope of the paper. People of interest please refer to reference [15]. Switch module is a kind of RapidIO Switch. Packets from SX95T are transferred to next PE (Processing Elements) through RapidIO Switch.

VI. CONCLUTION

The paper discusses the theory of DDC and the details of implementation on Xilinx FPGA. A flexible, programmable and high-efficiency architecture of DDC is implemented on Xilinx FPGA SX95T. The main feature of the DDC designed in the paper is that the DDC utilizes two clock scopes and has a FIFO interface. And the benefit of the DDC is efficiency in terms of resource consumption. It is practical for other developers to make use of the DDC module designed above. And finally the paper presents one application with the DDC module.

REFERENCES

[1] Reed, J.H. Software radio: a modern approach to radio engineering. Prentice Hall PTR, Upper Saddle River, NJ, 2002:1-21, 55-87.

[2]] Hollis T. Weir R. *The Theory of Digital Down Conversion*.26-06-2003. www.hunt-dsp.com/pdfs/tech/ddctheory.pdf

[3] Woods,R. McAllister J. Lightbody G. Yi Y. *FPGA-based Implementation of Signal Processing Systems*. John Wiley & Sons Ltd. U.K. 2008:111-125.

[4] Mitola J. The software radio architecture, IEEE Communications Magazine, 33/5, 1995.5,26-38.

[5] Pentek,Inc. *FPGAs for Software Radio.* http://www.pentek.com.

[6] Stephen Creaney, Igor Kostarnov. Designing Efficient Digital Up and Down Converters for Narrowband Systems. V1.0. Xilinx,Inc. November 21,2008.

[7] Mitra S.K. "Digital Signal Processing- A Computer-Based Approach". McGraw-Hill Inc. New York, 2001:359-510.

[8] Vaidyanathan P.P. Multirate Systems and Filter Banks. Prentice hall. N.J.1993:100-168.

[9] Tarn,H., et al, Design Efficient Wireless Digital Up and Down Converters Leveraging CORE Generator and System Generator, Xilinx® Application Note, XAPP1018.

[10] Altera, Inc. *Digital Down converter Reference Design*. Ver.2.0 Altera, Inc. April 2003.

[11] Xilinx ® Design Suite 11.2 Software Manuals, http://www.xilinx.com/support/software_manuals.htm

[12] Xilinx ® DDS Compiler, http://www.xilinx.com/products/ipcenter/DDS_Compiler.htm

[13] Xilinx ® FIR Compiler, http://www.xilinx.com/products/ipcenter/FIR_Compiler.htm

[14] Xilinx® Virtex-5 FPGA User Guide.

[15] www.xilinx.com/support/documentation/user_guides/ug190.pdf

[16] The RapidIO Trade Association web site: http://www.rapidio.org.