Design and FPGA Implementation of a Reconfigurable Digital Down Converter for Wideband Applications

Xue Liu, Xin-Xin Yan, Ze-Ke Wang, and Qing-Xu Deng

***Abstract*— This brief presents a field-programmable gate array-based implementation of a reconfigurable digital down converter (DDC) that can process input bandwidth of up to 3.6 GHz and provide a flexible down-converted output. The proposed DDC consists of a mixer and a resampling filter. The resampling filter can work at much higher clock rate. The reason is that all the single-cycle recursive loops in the resampling filter are pipelined by using either real/imaginary part-time multiplexing or parallel processing technique. With features like arbitrary sampling rate conversion, and dynamic configuration, the proposed design is highly flexible, so that it can generate a down-converted output with sampling rate, selectable within the range of 1 kS/s–225 MS/s. Moreover, the flexibility is further improved by being able to specify the output sampling rate and center frequency to a resolution of less than 1 S/s. The experimental results show that the proposed design can achieve the same functionality as the existing work but with fewer hardware resources.**

***Index Terms*— Digital down converter (DDC), field-programmable gate array (FPGA), resampling filter.**

I. Introduction

An important component in wideband digital receivers is a reconfigurable digital down converter (DDC), which is critical to the correct reception and resampling of radio signal. Limited by the process technology of devices, the design and implementation of wideband DDC must be optimized for both area and speed. In addition, DDC should be flexible enough to meet different application requirements, such as mix frequency resolution, output sampling rate, and antialiasing bandwidth. Therefore, how to optimize for the area, speed, and flexibility is an important issue for the design of DDC.

DDC usually consists of one mixer and one resampling filter. The mixer moves the target signal from its center frequency to the baseband, and the resampling filter is used to eliminate the signals outside the bandwidth, and reduce the sampling rate to avoid processing unnecessary bandwidth. The following filters or their combinations are often used as the resampling filter. They are half-band (HB) filter, cascaded-integrated comb (CIC) filter, polyphase filter, Farrow-based variable fractional delay (VFD) filter [1], and lookup table (LUT)-based variable digital filter (VDF) [2]. Among them, VFD filter and VDF can perform arbitrary sampling rate conversion (SRC). Compared with Farrow-based VFD filter, LUT-based VDF has lower hardware complexity and better filter performance. For filters with constant coefficients, the sum-of-power-of-two coefficient representation [3] and multiplier block (MB) technique [4] can be used to reduce the complexity.

Our contributions are as follows: 1) we propose a wideband-DDC architecture that can process the input data with sampling rate up to 7.2 GS/s; 2) an SRC factorization scheme is proposed to produce a down-converted output with sampling rate in the range from 1 kS/s to 225 MS/s; 3) the combinations of carry chain pipeline, MB, and real/imaginary part-time multiplexing techniques are applied to improve the speed and reduce the resources; and 4) a novel calculation method for fractional delay is proposed to relax the critical path of VDF. Compared with the VDF [2], the proposed LUT-based VDF has more flexibility due to real-time online configuration.

Finally, we realize the proposed DDC in a Xilinx Kintex-7 field-programmable gate array (FPGA). The experimental results show that the proposed design can achieve the same functionality as RF Engines Ltd.'s (RFEL's) DDC IP core [5], but it reduces the hardware resources and power consumption.

This brief is organized as follows. Section II presents the proposed DDC architecture. Section III illustrates the complete design details. Section IV presents specific implementations and experimental results. Section V concludes this brief.

II. Proposed Architecture

A. System Specifications

According to the sampling theorem, F_s should be greater than or equal to $2 \times B$, where F_s is the input sampling rate, and B is the bandwidth of the input signal. In our design, the maximum bandwidth is 3.6 GHz, so $F_s \geq 7.2$ GS/s.

No existing FPGA logic slices can reliably work at a clock rate over 1 GHz, so the clock rate of our design is limited to 450 MHz. For $F_s = R_1 \times 450$ MS/s with $R_1 \in \{4, 8, 16\}$, the sampling rate of the down-converted complex output is limited in the range of 1 kS/s–225 MS/s, so the SRC factor R ranges from $2 \times R_1$ to $2 \times R_1 \times 2^{18}$. Moreover, the resolution of the mixing and SRC is required to be less than 1 S/s.

The antialiasing bandwidth of complex output is $F_{\text{out}} \times 80\%$, where F_{out} is the output sampling rate. The filter magnitude specifications are as follows: less than 0.1-dB passband ripple and greater than 80-dB stopband attenuation.

B. Overall Architecture

A novel DDC architecture is proposed to meet the system specifications. The resampling filter consists of R_1-phase filter, HB filter, CIC filter, 2-times interpolation, LUT-based VDF, and polyphase filter (see Fig. 1). The main reason why we use these filters to construct the resampling filter and determine the order of these filters like that in Fig. 1 is to reduce the number of nonconstant coefficient multipliers and the RAM capacity.

A problem of LUT-based VDF is the asymmetrical property of the filter coefficients due to the nonzero fractional delay, so the number of multipliers for convolution calculation equals to the filter length. By placing one HB filter and one 2-times interpolation before LUT-based VDF, half of the input data are changed to zero. Thus, the number of nonconstant coefficient multipliers is reduced by half.

The SRC factor of polyphase filter directly determines the capacity of its data and coefficient RAMs. If we only use polyphase filter to perform SRC, the RAM resources may exceed the capacity of hardware devices, such as FPGA. Our solution is to place one

Manuscript received May 8, 2017; revised July 28, 2017; accepted August 30, 2017. Date of publication September 14, 2017; date of current version November 22, 2017. This work was supported by the National Natural Science Foundation of China under Grant 61501103 and Grant 61472072. *(Corresponding author: Xue Liu.)*

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Digital Object Identifier 10.1109/TVLSI.2017.2748603

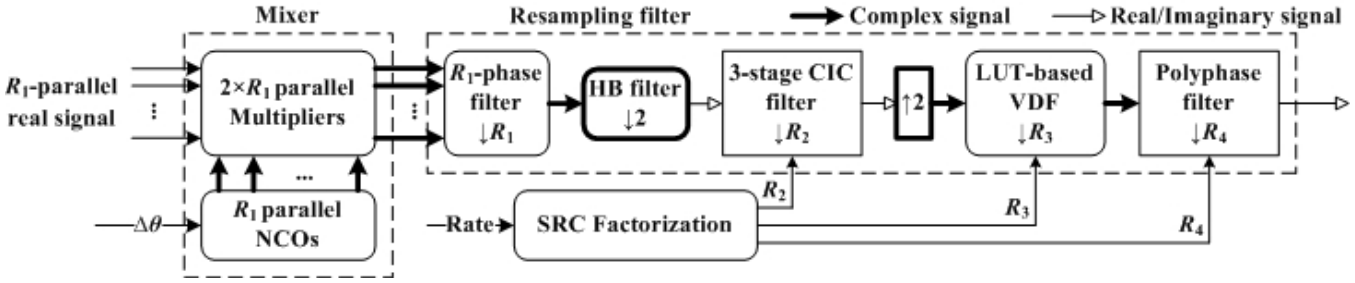

Fig. 1. Proposed DDC architecture.

TABLE I
SRC FACTORIZATION RESULTS

Rate	R_2	R_3	R_4
$(2^{27}, 2^{28}]$	↓**1**	$\downarrow 2^{28}$/Rate	↓2
$(2^{26}, 2^{27}]$	↓**1**	$\downarrow 2^{27}$/Rate	↓4
$(2^{25}, 2^{26}]$	↓**1**	$\downarrow 2^{26}$/Rate	↓8
$(2^{24}, 2^{25}]$	↓**1**	$\downarrow 2^{25}$/Rate	↓16
$(2^{23}, 2^{24}]$	↓**1**	$\downarrow 2^{24}$/Rate	↓32
$(2^{22}, 2^{23}]$	↓2	$\downarrow 2^{23}$/Rate	↓32
$(2^{21}, 2^{22}]$	↓4	$\downarrow 2^{22}$/Rate	↓32
$(2^{20}, 2^{21}]$	↓8	$\downarrow 2^{21}$/Rate	↓32
$(2^{19}, 2^{20}]$	↓16	$\downarrow 2^{20}$/Rate	↓32
$(2^{18}, 2^{19}]$	↓32	$\downarrow 2^{19}$/Rate	↓32
$(2^{17}, 2^{18}]$	↓64	$\downarrow 2^{18}$/Rate	↓32
$(2^{16}, 2^{17}]$	↓128	$\downarrow 2^{17}$/Rate	↓32
$(2^{15}, 2^{16}]$	↓256	$\downarrow 2^{16}$/Rate	↓32
$(2^{14}, 2^{15}]$	↓512	$\downarrow 2^{15}$/Rate	↓32
$(2^{13}, 2^{14}]$	↓1024	$\downarrow 2^{14}$/Rate	↓32
$(2^{12}, 2^{13}]$	↓2048	$\downarrow 2^{13}$/Rate	↓32
$(2^{11}, 2^{12}]$	↓4096	$\downarrow 2^{12}$/Rate	↓32
$(2^{10}, 2^{11}]$	↓8192	$\downarrow 2^{11}$/Rate	↓32

When R_2 is 1, CIC filter is bypassed.

CIC filter before polyphase filter. Although the CIC filter consumes some logic resources, the total resources are still reduced due to the reduction of RAMs.

C. SRC Factorization

Based on the proposed DDC, an SRC factorization scheme is presented to assign SRC factors to each component of the resampling filter. The SRC factor R is defined as follows:

$$R = F_s/F_{\text{out}} = R_1 \times R_2 \times R_3 \times R_4 \tag{1}$$

where R_1, R_2, R_3 ($1 \le R_3 < 2$), and R_4 are the decimation factors of R_1-phase filter, CIC filter, VDF, and polyphase filter.

The SRC control word Rate is defined as follows:

$$\text{Rate} = \text{Round}\left(\frac{2^{29} \times R_1 \times F_{\text{out}}}{F_s}\right) = \text{Round}\left(\frac{2^{29}}{R_2 \times R_3 \times R_4}\right) \tag{2}$$

where round function rounds a number to the nearest integer. According to (2), the resolution of the output sampling Rate is $F_s/(2^{29} \times R_1)$ (=0.8382 Hz). The SRC factorization results for R_1-parallel real input are listed in Table I. When rate has $2^{10} <$ Rate $\le 2^{28}$, R is in the range $(2 \times R_1, 2 \times R_1 \times 2^{18})$.

III. DESIGN DETAILS

A. Mixer

The mixer consists of R_1-parallel numerical control oscillators (NCOs) and $2 \times R_1$-parallel multipliers (see Figs. 1 and 2).

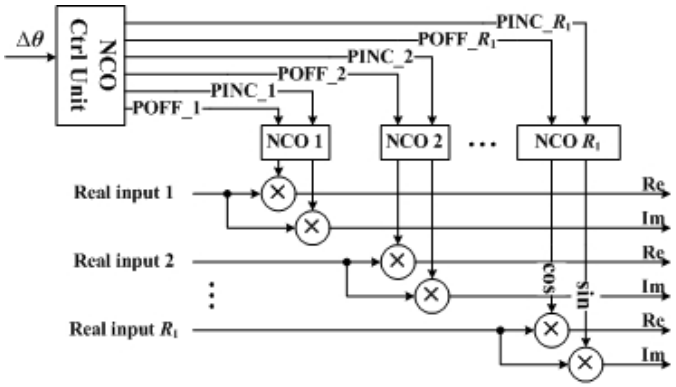

Fig. 2. Structure of mixer.

Let F_c be the center frequency of the target signal. F_{NCO}, which is the output frequency of NCO, is defined as follows:

$$\Delta\theta = \text{Round}(2^L \times F_{\text{NCO}}/F_s) = \text{Round}[2^L \times (-F_c)/F_s] \tag{3}$$

where L is the bit width of the phase accumulator of NCO, and $\Delta\theta$ is the phase increment value of NCO. For example, if the NCO parameters are: $F_s = 3.6$ GS/s, $\Delta\theta = 2^{28}$, and $L = 32$, F_{NCO} is 225 MHz, and the mixing resolution ΔF is 0.8382 Hz.

No existing FPGA logic slices can reliably work at a clock rate $F_s = R_1 \times 450$ MS/s ($R_1 \in \{4, 8, 16\}$), so the mix frequency signal is generated by using R_1-parallel NCO IP cores [6]. The phase increment value PINC(r) and phase offset value POFF(r) of NCO r ($r \in \{1, 2, \ldots, R_1\}$) correspond to $\Delta\theta$ as follows:

$$\text{PINC}(r) = R_1 \times \Delta\theta, \quad \text{POFF}(r) = (r-1) \times \Delta\theta. \tag{4}$$

B. R_1-Phase Filter

The maximum antialiasing bandwidth is $0.8 \times F_s/(2 \times R_1)$, so the normalized passband and stopband edges of R_1-phase filter are $0.2 \times 2\pi/R_1$ and $0.8 \times 2\pi/R_1$, respectively. The filter magnitude specifications require that the filter length is greater than or equal to 54 for $R_1 = 8$.

R_1-phase filter consists of two identical filters, which process the real and imaginary parts of the mixer output, respectively. Each filter consists of R_1 shift registers, one add–multiply array, and one adder tree [see Fig. 3(a)]. Considering the symmetry, the number of constant coefficient multipliers is reduced by half. In our design, we use the add and shift operations to realize the constant coefficient multiplier.

The highest clock rate of large bit-width adder is limited by the carry chain length. In order to remove this critical path, we pipeline the carry chain to improve the clock rate [see Fig. 3(b)], and place additional registers before the corresponding data bits of operands to ensure the timing requirement. This approach is used to design adders in the adder tree of R_1-phase filter and HB filter. It is also used to realize the constant coefficient multipliers in R_1-phase filter and HB filter. The following example illustrates this point.

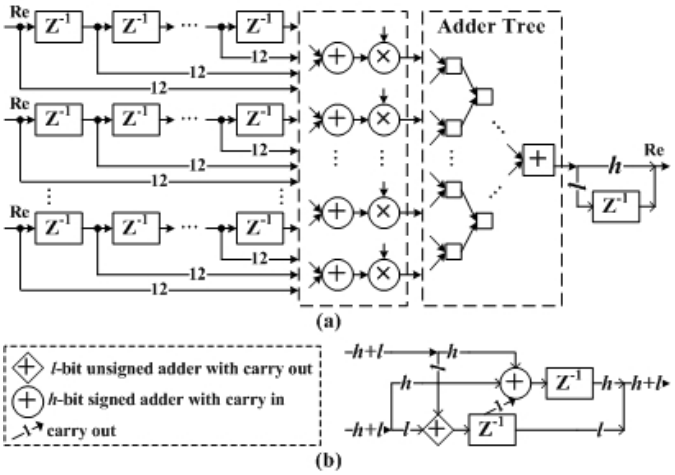

Fig. 3. (a) Structure of R_1-phase filter. (b) Structure of adder in adder tree.

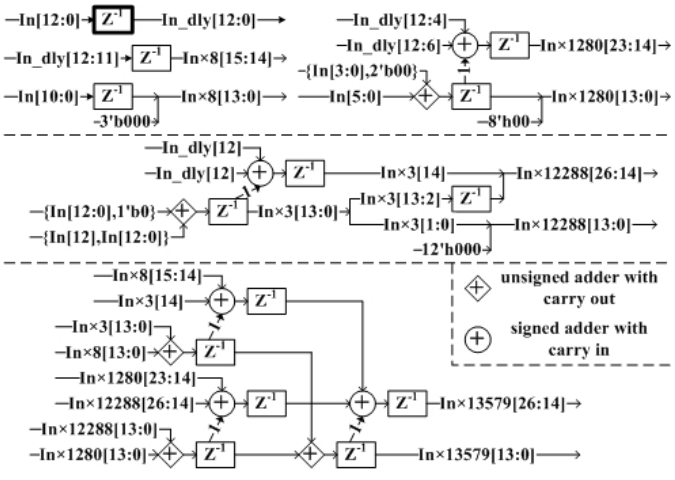

Fig. 4. Structure of multiplier for constant coefficient 13579.

One of the filter coefficients is 13579, so the multiplier can be expressed by $\text{In}\times 13579 = \text{In}\times 3\times 4096+\text{In}\times 5\times 256+\text{In}\times 8+\text{In}\times 3$. In × 5 × 256, and In × 3 are realized by adding, and In × 8 and In × 3 × 4096 are realized by shifting In and In × 3. The adder is built by connecting the carry out of l-bit unsigned adder with the carry in of h-bit signed adder (see Fig. 4). The upper limit value of l and h is determined by the specific FPGA device and required clock rate. The multiplier first exports the low l bit of $\text{In}\times 13\,579$, and then exports the high h bit. The interval between them is one cycle, so the output of the add–multiply array can be directly imported to the adder tree without additional registers.

C. HB Filter

The maximum antialiasing bandwidth and input sampling rate together determine that the passband and stopband edges of HB filter are 0.4π and 0.6π. The filter magnitude specifications require the filter length is greater than or equal to 47.

The number of constant coefficient multipliers is reduced to 1/4 of the original amount, because approximately half of the coefficients are zero, and nonzero coefficients are symmetrical. In this design, an MB technique, combined with the proposed carry chain pipeline technique, is used to reduce the complexity of constant coefficient multipliers.

HB filter is realized with two-phase structure because of decimation by 2 (see Fig. 5). Let $x_r(n)$ and $x_i(n)$ be the real and imaginary parts of HB filter input. From Fig. 5, we find that $x_r(2n)$ and $x_r(2n+1)$

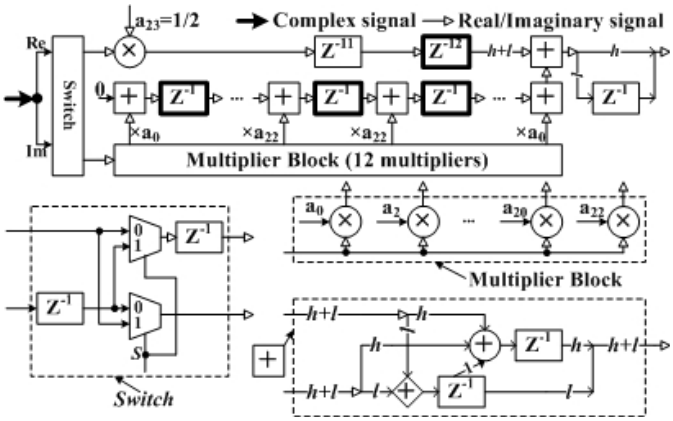

Fig. 5. Structure of HB filter.

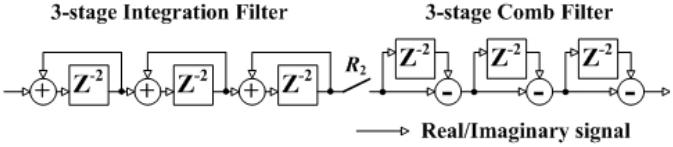

Fig. 6. Structure of CIC filter.

are first exported from switch, and then followed by $x_i(2n)$ and $x_i(2n+1)$. Additional registers should be added to the two branches of HB filter, because they are shared by the real and imaginary parts of the input data.

D. CIC Filter

For CIC filter with a decimation factor R_2, the bands centered at the integer multiple of $2\pi/R_2$ will produce the aliasing to the baseband. The worst severe aliasing lies in $(2\pi/R_2-\omega_{\text{pass}})$, where ω_{pass} is the passband edge of CIC filter. The bandwidth scaling factor b, which is defined by $b=\omega_{\text{pass}}\times R_2/2\pi$, is used to evaluate the antialiasing performance of CIC filter. The input sampling rate is $F_s/(2\times R_1)$, and the final antialiasing output bandwidth is $0.8\times F_s/R$, so $b\le 1/40$. After calculation, the passband droop of single-stage CIC filter is less than 0.009 dB, and the stopband attenuation is greater than 28.1 dB. Thus, the filter performance of three-stage cascaded CIC filter can meet the filter magnitude specifications.

The highest clock rate of CIC filter is limited by the single-cycle recursive structure of the integrator. In order to remove this critical path, we add one additional register to this recursive structure (see Fig. 6). The reason why this change can be successful is that CIC filter is time multiplexed by the real and imaginary parts of the output of HB filter.

E. LUT-Based VDF

The passband edge of VDF prototype is $\max[0.8\pi/(R_3\times R_4)]=0.4\pi$, and the stopband edge is $\min(2\pi/R_3-0.4\pi)\approx 0.6\pi$. The filter magnitude specifications require that the filter length is greater than or equal to 36.

In order to better approximate the continuous time version of the impulse response, the prototype is interpolated by 1024 to generate the VDF coefficients, which are quantized to 18 bit and stored in 36 RAMs. Considering the symmetry, the number of RAMs can be reduced by half. VDF is implemented by using the direct-form finite-impulse response structure. Before entering into VDF, the input data are interpolated by 2. Thus, the number of multipliers for convolution calculation can be reduced by half.

The core unit of VDF is the RAM address generator. When calculating a new output, it must precisely produce the address for

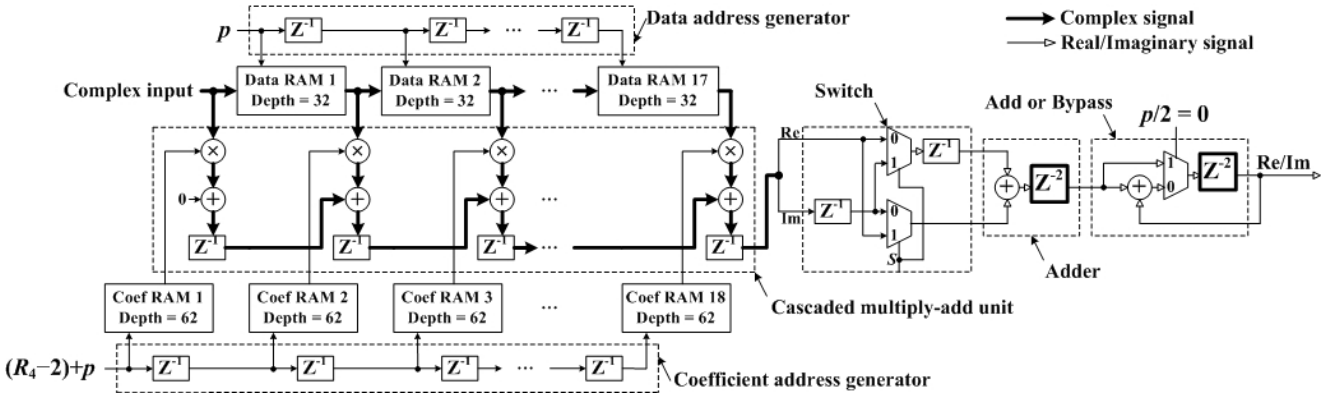

Fig. 7. Structure of polyphase filter.

all the coefficient RAMs. The fractional delay ϕ is the time interval between an output sample and the input sample preceding it [2]. There is a one-to-one correspondence between the coefficient address and ϕ. In our design, ϕ is

$$\phi_{n+1} = \begin{cases} \phi_n + \Delta\phi = \phi_n + (2^r - \text{Rate})/\text{Rate}, & \phi_n < 1 \\ \phi_n - 1, & \phi_n \geq 1 \end{cases} \tag{5}$$

where ϕ_0 is 0, and $2^{r-1} < \text{Rate} \leq 2^r$ with $r \in \{11, 12, \ldots 27, 28\}$. When $\phi_n \geq 1$, the output result of VDF is discarded.

The highest clock rate of VDF is limited by the single-cycle recursive calculation in (5). In order to remove this critical path, we recalculate ϕ as follows:

$$\phi_n = \begin{cases} \phi_{2m}, & n = 2m \\ \phi_{2m} - 1, & (n = 2m+1)\,\&\,(\phi_{2m} \geq 1) \\ \phi_{2m+1}, & (n = 2m+1)\,\&\,(\phi_{2m} < 1) \end{cases} \tag{6}$$

$$\phi_{2m} = \begin{cases} 2 \times \Delta\phi + \phi_{2m-2}, & (\phi_{2m-2} < 1)\,\&\,(\phi_{2m-1} < 1) \\ \Delta\phi + \phi_{2m-2}, & \phi_{2m-2} \geq 1 \\ \phi_{2m-1} - 1, & (\phi_{2m-2} < 1)\,\&\,(\phi_{2m-1} \geq 1) \end{cases} \tag{7}$$

$$\phi_{2m+1} = \begin{cases} 2 \times \Delta\phi + \phi_{2m-1}, & \phi_{2m-1} < 1 \\ \Delta\phi + \phi_{2m-1}, & \phi_{2m-1} \geq 1 \end{cases} \tag{8}$$

where $m \geq 1$, $\phi_0 = 0$, and $\phi_1 = \Delta\phi$. Note that ϕ_{2m} and ϕ_{2m+1} can be calculated simultaneously, so the calculation time of (7) and (8) can double that of (5). Compared with the recursive structure in (5), one additional register can be added to the recursive structures in (7) and (8). Rate is configurable at run time, so the division for calculating $\Delta\phi$ is unavoidable. In our design, the division is realized by using the subtraction and shift approach.

F. Polyphase Filter

The passband and stopband frequencies of polyphase filter are $0.4 \times 2\pi/R_4$ and $0.6 \times 2\pi/R_4$, where R_4 is its decimation factor. The filter magnitude specifications require that the filter length is greater than or equal to $18 \times R_4$, so each filter branch contains at least 18 coefficients.

As shown in Fig. 7, the polyphase filter is composed of one cascaded multiply–add unit, one data address generator, one coefficient address generator, 17 data RAMs, 18 coefficient RAMs, one switch, one adder, and one add or bypass unit. Shift registers are used to realize the addresses generators because of pipeline registers in the cascaded multiply–add unit. LUT-based distributed RAMs are used as data and coefficient RAMs. The depth of each data RAM is 32, i.e., $\max(R_4)$, and the depth of each coefficient RAM is 62, which is the sum of all possible values of R_4. The previous data of filter branch p are stored in address p of data RAMs, and the corresponding coefficients are stored in address $(R_4 - 2) + p$ of coefficient RAMs, where $p \in \{0, 1, \ldots, R_4 - 1\}$.

TABLE II
DATA PROCESSING ORDER OF POLYPHASE FILTER FOR $R_4 = 4$

Cycle	Switch input	Switch output	Adder output	Add or bypass output
1	0_r, 0_i	-	-	-
2	1_r, 1_i	0_r, 1_r	-	-
3	2_r, 2_i	0_i, 1_i	-	-
4	3_r, 3_i	2_r, 3_r	0_r+1_r	-
5	0_r, 0_i	2_i, 3_i	0_i+1_i	-
6	1_r, 1_i	0_r, 1_r	2_r+3_r	0_r+1_r
7	2_r, 2_i	0_i, 1_i	2_i+3_i	0_i+1_i
8	3_r, 3_i	2_r, 3_r	0_r+1_r	0_r+1_r+2_r+3_r
9	…	2_i, 3_i	0_i+1_i	0_i+1_i+2_i+3_i

The highest clock rate of the polyphase filter is limited by the single-cycle recursive accumulation of the convolution results of all filter branches, i.e., the recursive loop in the add or bypass unit. In our design, this critical path is removed by using the real/imaginary part-time multiplexing method, whose principle is explained by using the following example. Let p_r and p_i be the real and imaginary convolution results of filter branch p. Table II lists the processing order of the switch, adder, and add or bypass unit for $R_4 = 4$. We can add one additional register to the recursive loop in the add or bypass unit, because it is shared by the real and imaginary parts of the adder output.

IV. VALIDATION AND COMPARISON

A. Functionality Test

The proposed DDC architecture is implemented in the Xilinx FPGA XC7K70T-2FBG676. The real-input bit width is 12 bit, and the complex-output bit width is 24 bit. The development tool is Xilinx ISE 14.7. After place and route, we can obtain the hardware resources of each component (see Table III). After timing and power analyses, we can obtain the maximum clock rate and power consumption of the proposed design (see Table IV). The maximum clock rate $F_{\max}$ indicates that our solution can reliably work at the input sampling rate $F_s = R_1 \times 450$ MS/s.

In order to verify functionality, we realize the proposed DDC in the Xilinx Zynq-7000 FPGA XC7Z045, and test it in the Xilinx ZC706 evaluation board. The signal source consists of four carriers whose frequencies are 105.3, 112.8, 120.5, and 123.2 MHz, respectively. It is sampled by 3.6-GHz clock and quantized to 12 bits, and then fed into the DDC realization. By using the ChipScope tool, the output results are fed back to MATLAB software for analysis. As shown in Fig. 8,

TABLE III
HARDWARE RESOURCES OF EACH COMPONENT OF THE PROPOSED DDC ARCHITECTURE

Hardware Resources	Mixer			R_1-phase filter			HB filter	CIC filter	VDF	Polyphase filter
	$R_1 = 4$	$R_1 = 8$	$R_1 = 16$	$R_1 = 4$	$R_1 = 8$	$R_1 = 16$				
Registers	1340	2778	6071	3950	7262	14662	1994	697	4030	1541
6-input LUTs	787	1774	3488	2279	5679	10325	1437	524	1343	899
18kb Block RAMs	4	8	16	0	0	0	0	0	18	0
DSP48Es	8	16	32	0	0	0	0	0	38	37

TABLE IV
COMPARISONS OF RFEL'S SOLUTION AND OUR SOLUTION

	RFEL's solution for $R_1 = 8$ [5]	Our solution		
		$R_1 = 8$	$R_1 = 4$	$R_1 = 16$
Registers	19426	18302	13552	28995
6-input LUTs	12238	11656	7269	18016
18kb Block RAMs	38	26	22	34
DSP48Es	106	91	83	107
F_{max} (MHz)	450	454.3	454.5	452.4
Power (W)	Not available	1.626	1.446	2.293

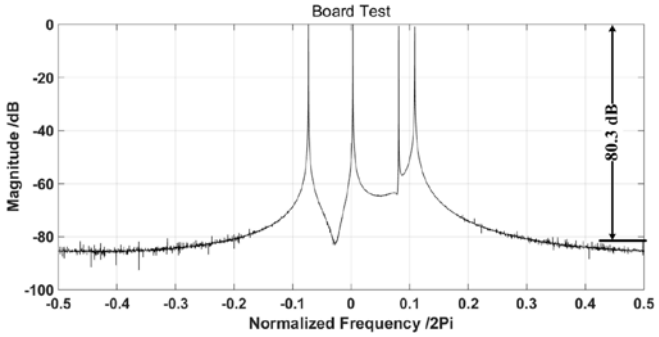

Fig. 8. Channel output with $R_1 = 8$, $R_2 = 1$, $R_3 = 8/7$, and $R_4 = 4$.

our solution can extract the signal source from the wideband input and perform SRC by setting $\Delta\theta$ and Rate.

B. Comparisons

Indeed, there are several references about the design of DDC. However, they can hardly have the same features as our design in terms of input sampling rate and output channel parameters. In addition, some of these references are commercial IP cores, which often do not publish their design details and relative information, such as power and resource counts.

Table IV presents the hardware resources of RFEL's solution [5] and our solution. Compared with wideband-DDC IP core [5], our design uses less hardware. Reduced resources also mean a reduction in power consumption. Note that the saved DSP48Es can be used to realize the constant coefficient multipliers in R_1-phase filter. As a result, the number of both six-input LUTs and registers of our solution for $R_1 = 8$ can be further reduced by at least 1500. Our DDC solution can achieve the same functionality as [5]. Therefore, it is a better choice for wideband applications because of the area and power saving.

V. CONCLUSION

An FPGA-based reconfigurable DDC architecture, that can process input bandwidth of up to 3.6 GHz (7.2-GS/s sampling rate) and provide a multistandard down-converted channel output with bandwidth of up to 180 MHz, was presented in this brief. Channel parameters, including the center frequency and output sampling rate, are configurable at run time. Compared with the existing work, the proposed solution represents an efficient tradeoff between the resource and performance. The wideband capability, combined with the reconfiguration ability, makes the proposed solution a better choice for surveillance, electronic warfare, and RF sampling applications.

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