Design and Simulation of Digital down Converter Based on System Generator

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***Abstract*—In this paper, the general structure of digital IF receiver is analyzed, based on the platform of system generator, the author design the digital controlled oscillator and a decimation filter model in the MATLAB/Simulink.**

Keywords-digital receiver; numerical controlled Oscillator; decimation filters

I. INTRODUCTION

With the rapid development of modern communications technology and communications needs, the wireless network communication system has a variety of different systems, such as satellite communications systems, cellular mobile communication systems, wireless paging communication systems etc. According to the characteristics of each communication system, they have different purposes, using different modulation methods, different encoding methods, and hardware-based communications systems and traditional systems can not meet people's needs. The Digital receiver technology is an important part of the software radio system, the analog signal convert into digital signal using the A/D converter, and then the system process a series of digital signal[1]. System Generator is a design tool which can make use of Mathworks Simulink to design platform FPGA .It can realize the high level, based on the model of the development environment to complete the hardware design. Developers can use the Generator System tool to reduce the workload of the designer to write hardware description language code[2]. In this paper, the digital down conversion model is designed in the Simulink environment, and its effectiveness is verified by simulation.

II. STRUCTURAL ANALYSIS OF DIGITAL IF RECEIVER

In analog down conversion, non-linearityof the mixer and frequency stability side-band, phase noise, temperature drift and conversion rate of the local oscillator are very difficult to solve. However, the analog down conversion have no these problems, but its operation speed is limited because of processing capability of hardware circuitry. Therefore, the designer need to consider the occupation of hardware resources, to optimize the system as far as possible[3]. Digital IF receiver block diagram is shown in Figure I. The receiver converts the received signal from the radio frequency conversion to the intermediate frequency using A/D converter, so that the analog to digital conversion is completed. The digital down conversion converts the IF signal into a baseband signal by special processing chip or FPGA. In the end, the baseband signal is processed such as demodulation. So, this paper focuses on the design of digital down converter[4].

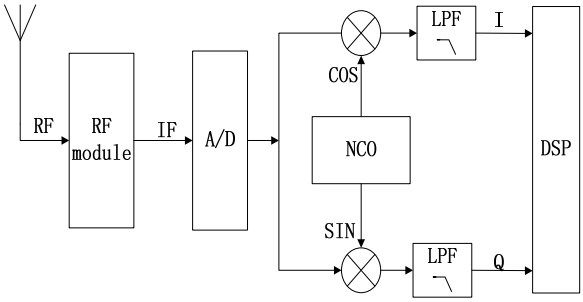

FIGURE I. BLOCK DIAGRAM OF DIGITAL IF RECEIVER

III. DESIGN OF DIGITAL DOWN CONVERTER BASED ON GENERATOR SYSTEM

A. Numerical Control Oscillator Designed

The digital controlled oscillator is the key part of the digital frequency synthesizer. It can produce a step pulse by the accumulator and map the amplitude, then it will output synthesized frequency. With the development of digital communication technology, the precision and speed of the data transmission is also higher and higher, the digital controlled and precision of a high-frequency carrier signalis also crucial to digital communication systems. In DDC system, the accuracy of the digital up conversion will be impacted by the accuracy of NCO digital signals. After digital mixing, the calculation will have a certain error because of accuracy of the mixer[5]. So, the hardware resources must be considered in the implementation process of NCO. Meanwhile, the designer have to consider and the operation precision of the upper frequency conversion system should be considered.

The NCO module consists of the following parts: the phase accumulator module, shift module, phase-amplitude mapping table. The phase accumulator need cycle phase accumulation by inputting step control signal, the shift operation removed up to 14 bits as the phase and amplitude of the mapping table look-up table address lines, so as to obtain the sine, cosine signal the phase corresponding to the amplitude value. NCO model is built in Simulink environment as shown in Figure II.

System sampling rate f_s =12.8MHz, the step control signal is 32 bit unsigned fixed-point number 1.11065e9,the 32 bits are all small bits; Shift module will move data to the right 18, take the high 14 as the ROM lookup table lookup table address lines. The depth of ROM lookup table (amplitude interval) is 2^{14} ==16384, the initial value of the sine table is

$\sin(pi*(0:16383)/8192)$.

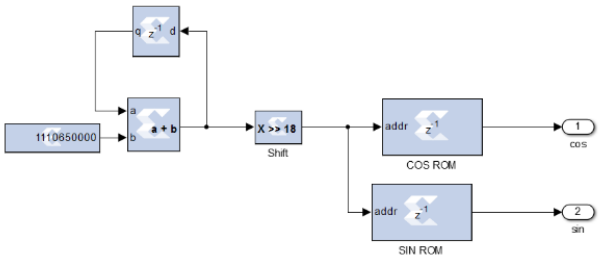

FIGURE II. THE MODEL OF NCO

B. Decimation Filter Designed

The core of digital down conversion technology is to build a set of efficient decimation filter, so that the rate of data flow rate is significantly reduced, to meet the requirements of FPGA, DSP and other parts of the processor. The cascaded integrator-comb filter (CIC) can achieve the extraction of the function. It does not require the multiplier and the filter coefficients of the memory cell and reduce the amount of storage in the middle of the process using integral links[6]. Therefore, CIC filter is often used in the design of high sampling rate and extraction.

Although the multi-stage cascade structure can increase attenuation of stop-band and reduce the effects of aliasing, but it will increase tolerance of in-band. So, in this paper, the design of CIC decimation filter adopt a cascade of 5 CIC decimation structure. Decimation filter of model is built in Simulink environment as shown in Figure III.

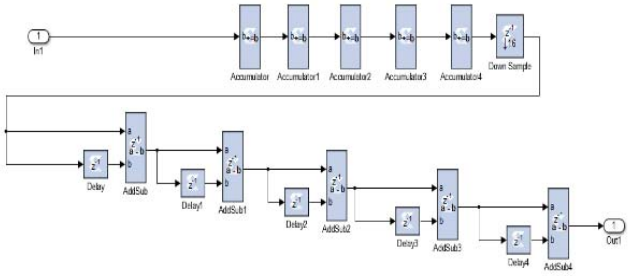

FIGURE III. THE MODEL OF DECIMATION FILTER

The model of digital down converter system is shown in Figure IV. The modulated model has been encapsulated forexpedient simulation. Modulation signal of baseband signal rate: 0.033316MHz; Carrier signal of frequency is 3.3MHz; The sampling rate of t the down conversion system is 12.8MHz, down converter output0.8MHz.

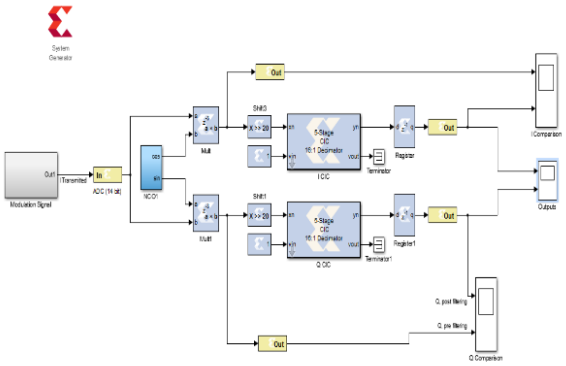

FIGURE IV. THE MODEL OF DIGITAL DOWN CONVERTER SYSTEM

IV. SIMULATION ANALYSIS

The model of digital down converter system are operated, The road of data waveform are showed. The simulation results are shown in Figure V. From the simulation results, we can see that the waveform is smooth and complete after the signal is mixed with CIC, and the model is correct. Spectrum of NCO, as shown in Figure VI. NCO generate sine cosine signal that the frequency is 3.3MHz.It reaches the design requirements, and it also meets the required frequency of the system. Spectrum of received signal, as shown in Figure VII.

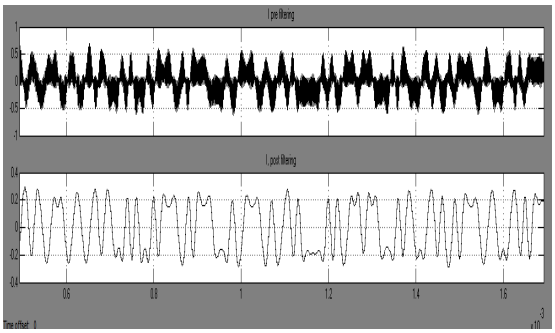

FIGURE V. COMPARED THE I ROAD OF WAVEFORM BEFORE AND AFTER FILTERING

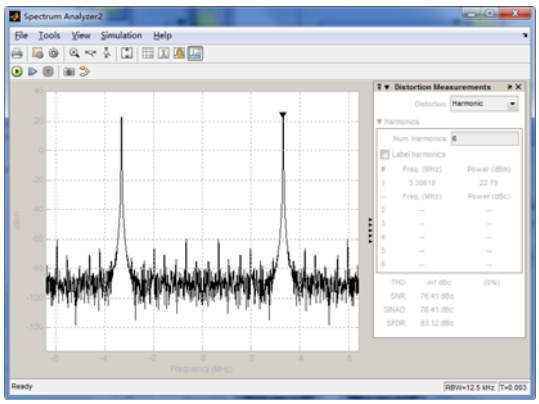

FIGURE VI. SPECTRUM OF NCO

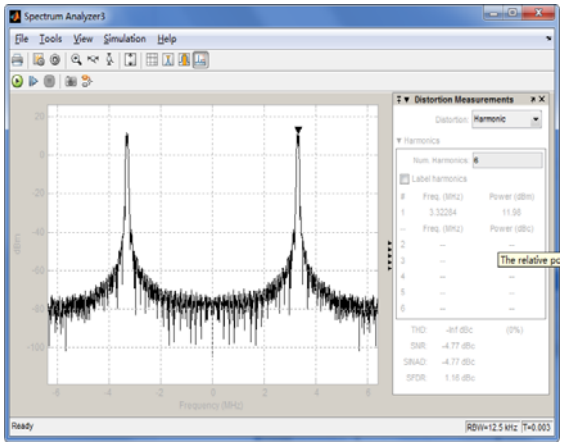

FIGURE VII. SPECTRUM OF RECEIVED SIGNAL

V. CONCLUSION

Generator for DSP System is a digital signal processing system development tool that is so easy and profound. This paper analyzes the basic structure of digital down conversion system. According to the functional characteristics of Generator System, the numerical control oscillator module and the decimation filter module are designed. And the en-tire digital down conversion system is cascaded, the design of the module and the system is simulated and verified. The design of this paper, it makes the whole design work more simple and efficient and shortens the development cycle of the system.

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