Analog Integr Circ Sig Process (2012) 73:531–543
DOI 10.1007/s10470-012-9905-9

Cascade linear phase recursive half-band filters implement the most efficient digital down converter

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Received: 29 February 2012 / Revised: 17 June 2012 / Accepted: 19 June 2012 / Published online: 10 July 2012

Abstract The digital down converter (DDC) is a fundamental component in modern DSP based receivers. The basic architecture is the DSP implementation of the Edwin Armstrong heterodyne circuit. It is formed by three processes, a quadrature heterodyne, a pair of low-pass filters, and an M-to-1 down sampler. The index M is the ratio of input to output bandwidth of the filtering process. When M is large, the filtering is often performed in two sub-filters: a cascade integrator comb (CIC) filter that performs most of the down sampling followed by a pair of half-band filters that perform spectral correction, some final bandwidth reduction, and the remainder of the down-sampling. The attraction of the CIC filter is that it performs the filtering without multiplies. In this paper we present two alternate filter structures that offer significant computational advantages over the conventional CIC based DDC. These architectures offer the minimum power implementation of a DDC and likely will find great value in battery operated radio receivers.

Keywords Digital down converter · Cascade-half-band FIR filter · Cascade-half-band IIR filter · CIC filter

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1 Introduction

There are many ways of performing the task of a digital down converter. The digital down converter (DDC) converts a real sampled data signal centered at an arbitrary intermediate frequency to a complex base band signal centered at zero frequency. The most common form of the DDC is based on Edwin Armstrong's heterodyne receiver. It contains three processes: a quadrature direct digital synthesizer (DDS) feeding a pair of multipliers that perform the desired spectral translation, a pair of sampled data low-pass filters that reduce the signal bandwidth, and a down sampling process that reduces the output sample rate in proportion to the filter bandwidth reduction. In modern receivers the filter is implemented in a multirate architecture that embeds the re-sampling process in the filtering process.

The ubiquitous resampling filter present in many systems is the K-stage cascade integrator comb (CIC) or Hogenauer filter [1]. This filter consists of K-digital integrator stages, an M-to-1 down sampler, and K-derivative stages. Figure 1 shows the evolution of the M-to-1 resampled K-stage box-car integrator transfer function to separate numerator and denominator filters and their reordering by the noble identity [2] to the Hogenauer partition with the comb filters at the input rate becoming derivative filters at the output rate.

The attraction of this filter is that it performs the filtering and resampling without multipliers. In many systems the CIC performs an M/4-to-1 bandwidth and sample rate reduction followed by a pair of half-band filters that correct for the CIC's main lobe spectral distortion and a final house cleaning filter to obtain a 4-to-1 bandwidth reduction and 4-to-1 down sampling. This is seen in Fig. 2 which shows the form of the CIC based DDC as often seen in the Graychip family.

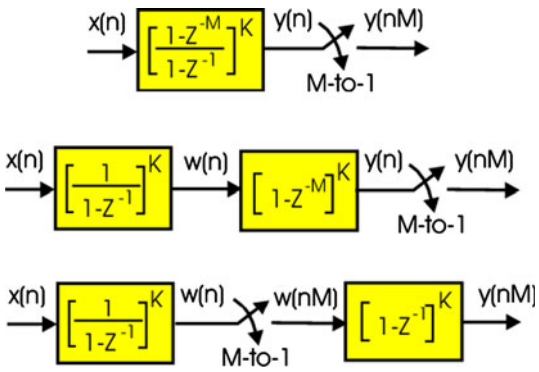

Fig. 1 Successive transformations of M-to-1 down sampling K-stage boxcar integrator to cascade integrator comb and then to Hogenauer partition

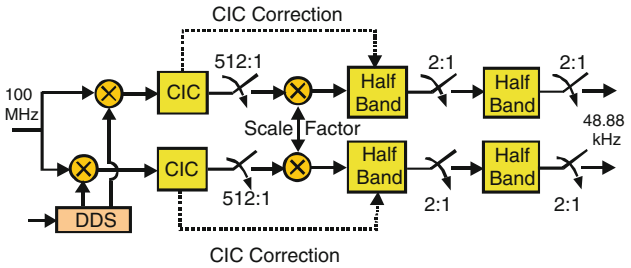

Fig. 2 Digital down converter containing direct digital down converter, M/4-to-1 resampling CIC filter, one-half-band compensating filter and one-half-band clean-up FIR filter

Figure 3 shows the frequency response of 4, 5, and 6 stages of CIC filtering. We see here the pass band spectral curvature which requires the post CIC correction stage. We also see how the increase in number of stages increases the attenuation of the alias stop band spectral span.

An important consideration often overlooked when comparing the CIC filter to other filtering options is the bit width of the registers in the CIC Integrators. The prototype M-to-1 resampling boxcar filter has a gain of M and of course a K-stage version of the boxcar filter has a gain of M^{K}. The registers in the integrators of the CIC, as well as the registers of the derivatives, must accommodate this gain. The number of bits required for the integrator registers is shown in (1) as the sum of the number of bits representing the input signal and the number of bits to accommodate the K stages of gain.

$$b_{\mathrm{ACCUM}} = b_{\mathrm{DATA}} + \mathrm{ceil}[\log_2(M^{\mathrm{K}})] \tag{1}$$

Specifically say we require 16 bit input samples processed by a 6-stage filter performing 2048-to-1 down sampling. For this example, the CIC filter would perform 512-to-1 down sampling and the following half-band filters would perform the remaining 4-to-1 down sampling. Inserting the 512 for M in (1) we find that $b_{\mathrm{ACCUM}} = 16 + 54$ or 70 bits. There would be 6 integrators on each of the I and Q legs of the DDC for a total of twelve 70 bit registers operating at the input sample rate. The total number of bits circulating in the CIC integrators would be 840 bits which is the equivalent to 52 16-bit words. Alternate DDC architectures that use less than 52 16-bit words at the input sample rate offer a more energy efficient choice for the DDC than the CIC based version. The original Hogenauer paper describes a mechanism to prune the word widths in the accumulator chain as a way to reduce implementation resources and energy use. For options in which the input ADC bit width and the resampling ratio are fixed and it makes sense to tune the accumulator bit widths to the specific processing task. In other applications for which the resampling ratio is controlled by reconfigurable software the option to optimally tune the accumulator width may not be applicable. In many SDR [3] applications the hardware may be fixed and the accumulator width cannot be changed for applications requiring different resampling ratios. DSP chip sets do not offer the flexibility of selecting arbitrary width accumulators as do designs embedded in an application specific integrated circuit (ASIC) or field programmable gate arrays (FPGA). The more standard procedure, as implemented for instance in the Grey chip set, is to fix the bit width in the hardware design and caution the DSP designer that while the fixed wide width accumulators have been designed to accommodate a wide range of resampling ratios, the fixed width does limit the allowable filter gain.

2 Alternate architecture I

The first design we present here replaces the resampling CIC filters with a cascade of 2-to-1 down sampling half-band filters. The half-band filters are implemented as a two-path polyphase partition often called a quadrature mirror filter. In this configuration the 2-to-1 down sampling is performed prior to the filtering process so that the filtering is performed at the reduced output sample rate rather than at the input rate. A cascade of traditional true half-band filters is very efficient because half the coefficients are zero and each successive filter in the chain operates at half the speed of the previous stage. We have two options to implement the half-band filters; these are the linear phase non-recursive or finite duration impulse response (FIR) and the linear phase recursive or infinite duration impulse response (IIR) filter.

We first consider the linear phase half-band FIR filter partitioned into two-paths [4] as shown in (2) and resampled in the block diagrams of Fig. 4. Here the 2-to-1 resampler is brought through the filter partitions $H_0(Z^2)$ and $H_1(Z^2)$ which now operate at the reduced output rate. Noting that 2 units of delay at the input rate is the same as

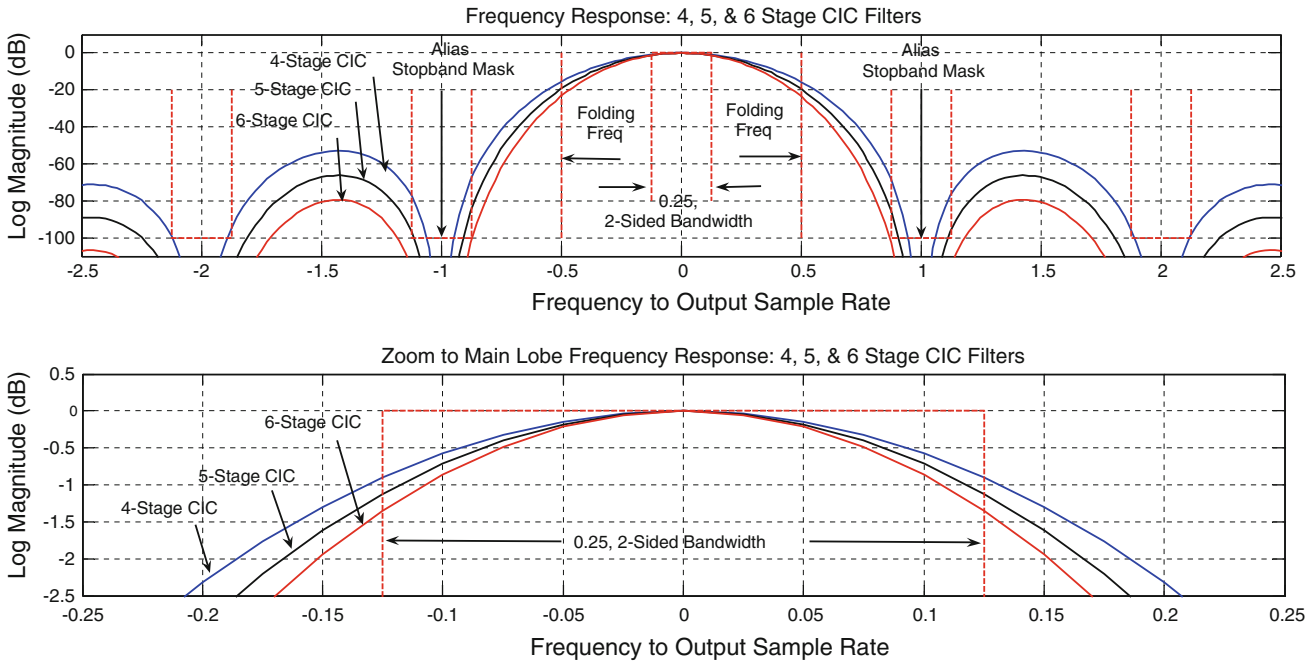

Fig. 3 Frequency response of 4, 5, and 6 stages of CIC filter showing stop band intervals and pass band spectral curvature

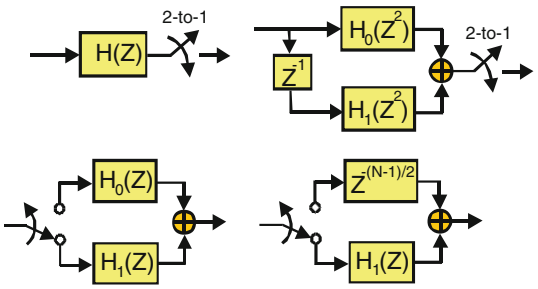

Fig. 4 Down-sampled half-band filter, poly-phase partition, with reordering of filter and down sampler

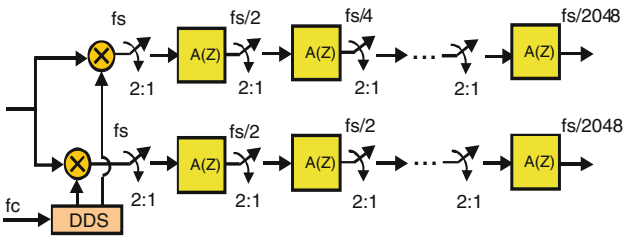

Fig. 5 Cascade of 10 2-to-1 down sampled half-band filters

1 unit of delay at the output rate we invoke the noble identity to interchange the order of filtering and sample rate change. We alter the filter notation to $H_0(Z)$ and $H_1(Z)$ and keep in mind the change in clock rate.

As shown in Fig. 5 we replace the CIC filter with a cascade of 11 half-band FIR filters to accomplish the same 2048-to-1 bandwidth reduction and sample rate change.

$$\begin{aligned} H(Z) &= \sum_{n=0}^{N-1} h(n)Z^{-n} \\ &= \sum_{n=0}^{(N/2)-1} h(2n)Z^{-2n} + \sum_{n=0}^{(N/2)-1} h(2n+1)Z^{-(2n+1)} \\ &= H_0(Z^2) + Z^{-1}H_1(Z^2). \end{aligned} \tag{2}$$

Each 2-to-1 down sample aliases the spectral span bracketing the half sample rate to baseband. The stop band attenuation of this aliased band is designed to be 100 dB as was the level we had selected for the CIC we are replacing. For this design example we selected the in-band ripple for each stage to be 0.01 dB to assure the composite ripple would be less than 0.1 dB. As was the criterion for the CIC and half-band correction filter, the final output bandwidth is one-half of the output sample rate. Then the two-sided stop band widths in successive half-band filters are seen to be 1, 2, 4,…., 2048 parts in 4,096. Figure 6 shows the impulse and frequency response of filters h_8 and h_9 of the FIR filter version of this cascade.

Labeling the successive filters in this cascade as h_1, h_2, …, h_{11} we find that 4 different filters are required for the cascade. Table 1 lists their lengths and arithmetic workload.

These filters are operated at successively reduced sample rates in the 11-stage cascade. Table 2 presents the number of additions and multiplies of each filter in, say the I-path, referenced to the input sample rate of the cascade. Since the filter chain must be repeated for the second path, we must double the workload shown in Table 2 to account for the total workload for the DDC. We then note that the

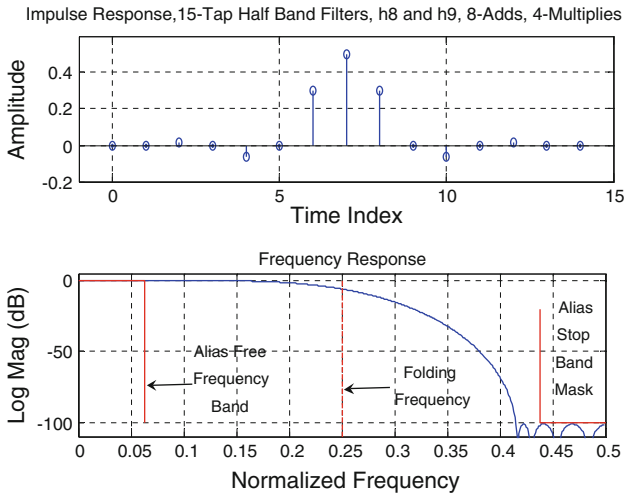

Fig. 6 Impulse and frequency response of filters h_{10} and h_{11} in 11-stage cascade of FIR half-band filters

Table 1 Linear phase half-band FIR filters in DDC cascade

Filter numbers	Number of taps	Operations
h1-to-h4	3	2-A, 0-M, 1-Shft
h5-to-h8	7	4-A, 2-M, 0-Shft
h9-to-h10	15	8-A, 4-M, 0-Shft
h11	23	12-A, 6-M, 0-Shft

number of adds referenced to the input rate is less than 2.14 and the total number of multiplies referenced to the input rate is 0.13 per path. Doubling these numbers, we find the total workload for the DDC is 4.28 adds and 0.26 multiplies. Remember that these are 20 bit adds and multiplies (for the 5 dB/bit arithmetic rule) rather than the 6 70 bit adds per path of the six stage CIC. The ratio of add bits $(4.28 \times 20)/(6 \times 70)$ is approximately 1-to-4.9 and when we include the 0.26 multiply (5×20) the ratio drops to approximately 1-to-2.54. A potential 2.54-to-1 improvement over the CIC cannot be ignored.

Figure 7 shows the spectra of the composite cascade of half-band filters starting at filter h_{11} and moving back through the FIR cascade till the equivalent filter h_7 to h_{11}.

3 Alternate architecture II

We now consider a variant of the half-band filter cascade that replaces the FIR filters with recursive two-path all-pass linear phase filters. The form of this filter is shown in Fig. 8. The core stages of this filter are shown in Fig. 9. The transfer functions of these cores are first and second order polynomials in Z^2. Note the upper path is a pure delay line with linear phase. The lower path is designed to match the phase of the upper path in the pass band region and to differ from the upper path by 180° in the stop band region. Since the upper path is linear phase, the composite filter is also linear phase up to the pass band edge (as shown later in Fig. 17). Since the polynomials forming the filter stages are polynomials in Z^2 we can invoke the noble identity and pull the 2-to-1 down sampler through the filter and perform the 2-to-1 down sampling at the input to the filter. When we do this, the polynomials in Z^2 become polynomials in Z. This transformation is shown in Fig. 10 which started as an eleventh order two-path filter. In this form the filter has only 5 coefficients for which the down sampling workload is remarkably only 2.5-multiplies per input sample.

We will shortly have need for four versions of this half-band filter that are centered on the four cardinal directions that are multiples of $\pi/2$. But for now we insert these half-band filters in the structure of Fig. 5. Figure 11 shows the impulse, frequency, and group delay response of filters h_7, h_8 and h_9 of the IIR filter version of this cascade.

Labeling the successive filters in this cascade as h_1, h_2, …, h_{11} we find that 3 different filters are required for the cascade. Table 3 lists their lengths and arithmetic workload.

Figure 12 shows the spectra of the composite cascade of half-band IIR filters starting at filter h_{11} and moving back through the cascade till the equivalent filter h_7 to h_{11}. These IIR filter spectra are remarkably similar to the FIR filter spectra of Fig. 7.

These filters are operated at successively reduced sample rates in the 11-stage cascade. Table 4 presents the number of additions and multiplies of each filter in one path referenced to the input sample rate of the cascade. Note that after accounting for both paths by doubling, the total and the total number of multiplies referenced to the

Table 2 Filter number in FIR cascade, number of taps in filter, and number of arithmetic operations referenced to input

Filter number	1	2	3	4	5	6	7	8	9	10	11	Total
Number of taps	1	3	3	3	7	7	7	7	15	15	22	–
Adds	2	2	2	2	4	4	4	4	8	8	12	–
Multiplies	0	0	0	0	2	2	2	2	4	4	6	
Adds referenced to input	2/2	2/4	2/8	2/16	4/32	4/64	4/128	4/256	8/512	8/1024	12/2048	2.14
Multiplies referenced to input	0/2	0/4	0/8	0/16	2/32	2/64	2/128	2/256	4/512	4/1024	6/2048	0.13

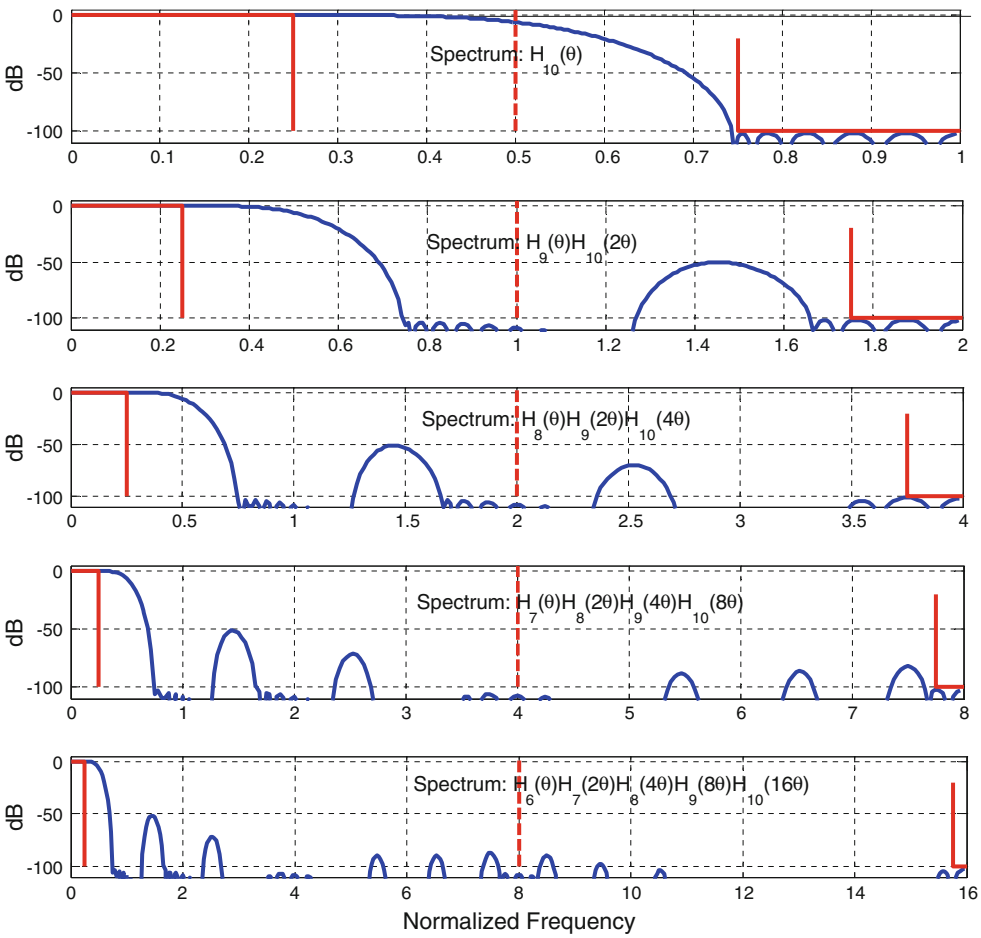

Fig. 7 Spectra: composite FIR filters, $H_{11}(\theta)$, $H_{10}(\theta)H_{11}(2\theta)$, $H_9(\theta)H_{10}(2\theta)H_{11}(4\theta)$, $H_8(\theta)H_9(2\theta)H_{10}(4\theta)H_{11}(8\theta)$, and $H_7(\theta)H_8(2\theta)H_9(4\theta)$ $H_{10}(8\theta)H_{11}(16\theta)$

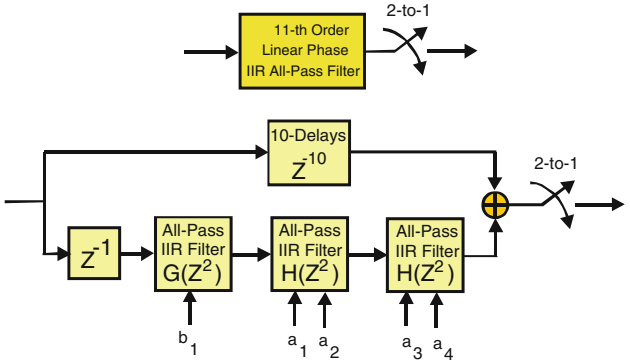

Fig. 8 Two-path, half-band linear phase IIR filter

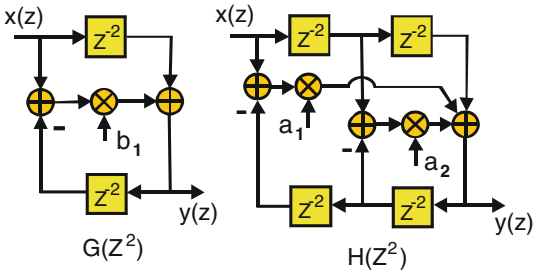

Fig. 9 Recursive all-pass first order and second order filters formed by polynomials in Z^2

input rate is approximately 3.0 and the number of adds referenced to the input rate is approximately 1.0 per path. These numbers represent an improvement over the CIC's 6-stages of wide band accumulators. Comparing Tables 2 and 4 we see that these numbers are slightly greater than the FIR half-band filter cascade.

Studying the two tables we recognize that at the start of cascades the FIR filters are more efficient than the IIR

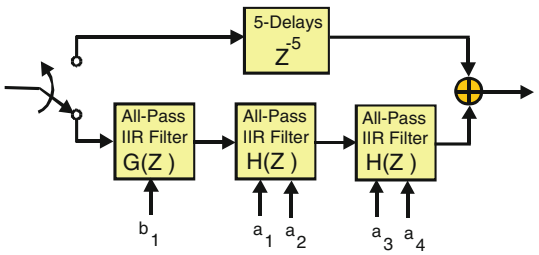

Fig. 10 2-to-1 Down sampled two-path, linear phase IIR half-band filter

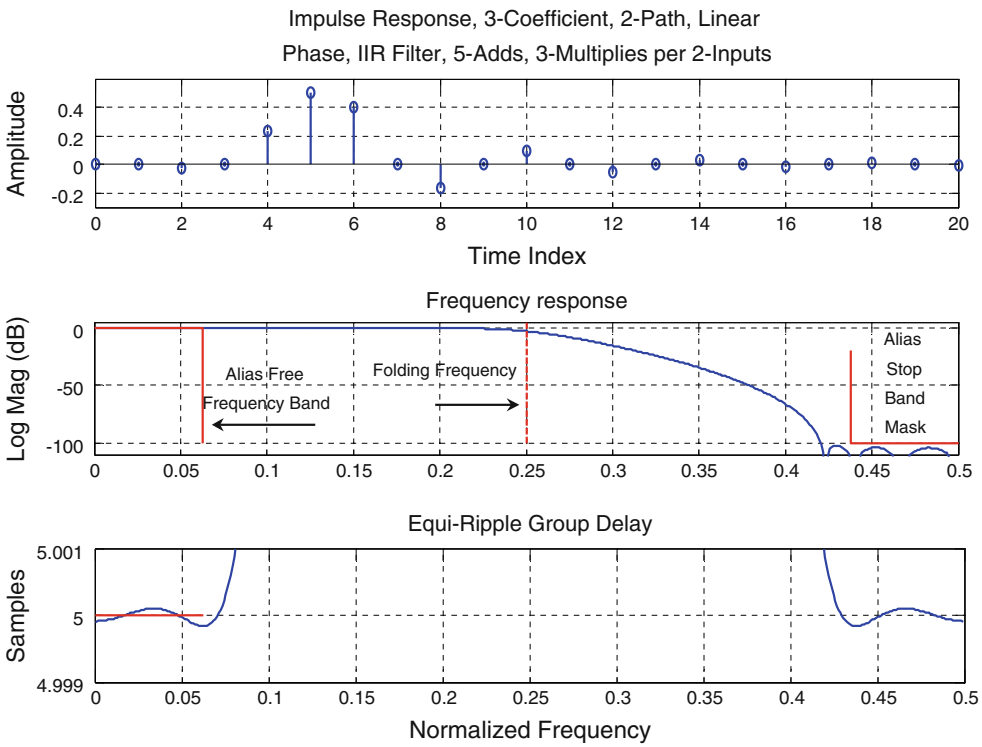

Fig. 11 Impulse, frequency and group delay of IIR filter

Table 3 Linear phase half-band IIR filters in DDC cascade

Filter numbers	Number of coefficients	Operations
h1-to-h7	1	3-A, 1-M
h8-to-h10	3	7-A, 3-M
h11	5	11-A, 5-M

filters and that at end of the cascades the IIR filters are more efficient than the FIR filters. This suggests a hybrid cascade comprising FIR filters at the start of the cascade and IIR filters at the end of the cascade may be the most efficient application of the cascade-half-band filters. Table 5 presents the number of multiplications and additions in a hybrid realization of the half-band cascade per path. Here the first four filters in the chain are the multiply free 3-tap fir filter while the remaining eight filters are the corresponding filters of the IIR cascade. We see that for this hybrid cascade the number of additions referenced to the input, after doubling is 4.2 while the number of multiplications referenced to the input, after doubling, is 0.16. These numbers represent the smallest workload for the cascade of half-band filters. The ratio of add bits $(4.2 \times 20)/(6 \times 70)$ is approximately 1-to-5.0 and when we include the 0.16 multiply (3.3×20) the ratio drops to approximately 1-to-2.8. A potential 2.8-to-1 improvement over the CIC cannot be ignored.

4 Alternate architecture III

We now propose a variant of the half-band filter cascade. In this variant, the DDS and the quadrature down conversion are transferred from the input of the half-band cascade to its output. In doing so the workload for the heterodyne becomes insignificant because it occurs at the very low output rate rather than at the high input rate. As part of this architectural transformation, the low-pass half-band filters in the cascade are replaced with modified half-band filters. The modified filters are selected from one of four versions of the same bandwidth filter with the versions only differing by their center frequencies which are aligned with the four cardinal directions or center frequencies of DC, fs/4, fs/2, and –fs/4. The filter pair at DC and fs/2 corresponds to the center frequencies of a conventional quadrature mirror filter with their selection performed by a sign change at the sum of the two-path partition. The two additional filters at ±fs/4 are seen to be the half-band Hilbert transform filters which are similarly formed with the same weights as the low-pass prototype filter by weighted sums with the "j" operator.

Using the notation of a 4-point DFT we will refer to these four filters by their bin numbers, 0, 1, 2, and 3. The transfer function for the upper and lower arms of Fig. 13, denoted TP and BT, are shown in (3). We can perform the low-pass to band-pass transformation that converts the low-pass Bin-0 filter to the Hilbert transform Bin-1 filter by the

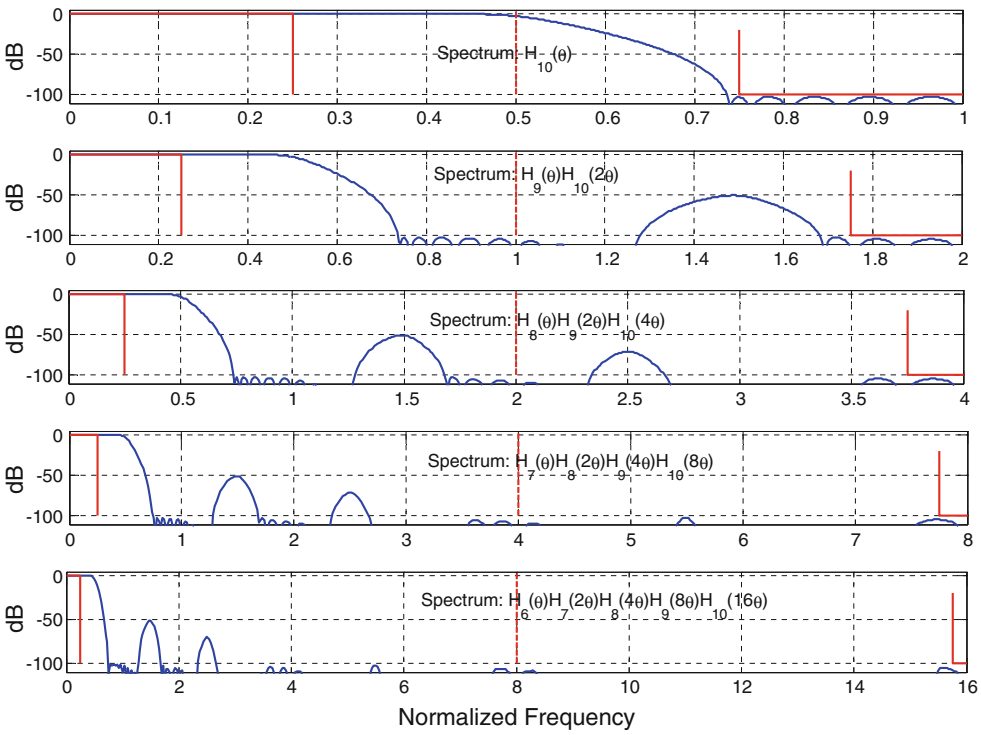

Fig. 12 Spectra: composite IIR filters, $H_{11}(\theta)$, $H_{10}(\theta)H_{11}(2\theta)$, $H_9(\theta)H_{10}(2\theta)H_{11}(4\theta)$, $H_8(\theta)H_9(2\theta)H_{10}(4\theta)H_{11}(8\theta)$, and $H_7(\theta)H_8(2\theta)H_9(4\theta)$ $H_{10}(8\theta)H_{11}(16\theta)$

Table 4 Filter number in IIR cascade, number of taps in filter, and number of arithmetic operations referenced to input

Filter number	1	2	3	4	5	6	7	8	9	10	11	Total
Number of coefficients	1	1	1	1	1	1	1	3	3	3	5	–
Adds	3	3	3	3	3	3	3	7	7	7	11	–
Multiplies	1	1	1	1	1	1	1	3	3	3	5	
Adds referenced to input	3/2	3/4	3/8	3/16	3/32	3/64	3/128	7/256	7/512	7/1024	11/2048	3.02
Multiplies referenced to input	1/2	1/4	1/8	1/16	1/32	1/64	1/128	3/256	3/512	3/1024	5/2048	1.01

Table 5 Filter number in hybrid FIR-IIR cascade, number of taps in filter, and number of arithmetic operations referenced to input sample rate

Filter type	FIR	FIR	FIR	FIR	IIR	IIR	IIR	IIR	IIR	IIR	IIR	
Filter number	1	2	3	4	5	6	7	8	9	10	11	Total
Number of taps	3	3	3	3	1	1	1	3	3	3	5	–
Adds	2	2	2	2	3	3	3	7	7	7	11	–
Multiplies	0	0	0	0	1	1	1	3	3	3	5	
Adds referenced to input	2/2	2/4	2/8	2/16	3/32	3/64	3/128	7/256	7/512	7/1024	11/2048	2.09
Multiplies referenced to input	0/2	0/4	0/8	0/16	1/32	1/64	1/128	3/256	3/512	3/1024	5/2048	0.077

substitution shown in (4). When this substitution is made in (3) we obtain (5) where we see the effect of the transformation is to reverse the polarity of the odd indexed coefficients in the second order polynomials and to declare the bottom path to be the imaginary part of the complex impulse response. This is precisely the coupling of a Hilbert transform filter with the upper path delay line that forms the analytic signal filter.

$$TP_1(Z) = \frac{1}{Z^6}$$
$$BT_1(Z) = \frac{1}{Z}\frac{1+b_1Z^2}{Z^2+b_1}\frac{1+a_1Z^2+a_2Z^4}{Z^4+a_1Z^2+a_2} \quad (3)$$

$$Z^{-1} \Rightarrow jZ^{-1}$$
$$Z^{-2} \Rightarrow -Z^{-2} \quad (4)$$

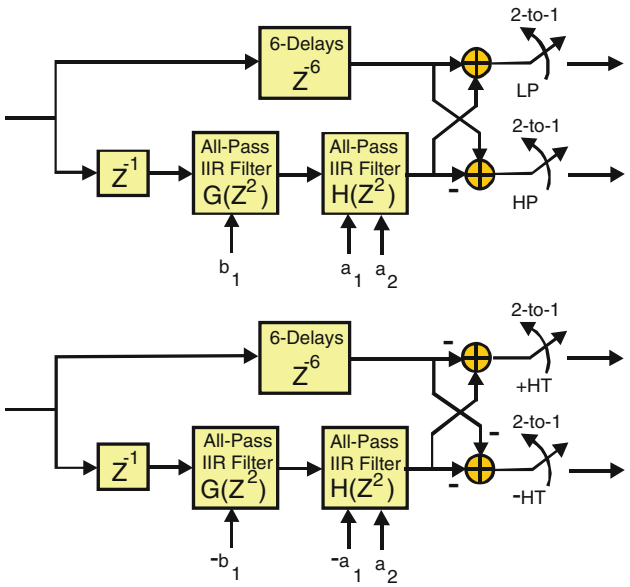

Fig. 13 Resampled 7th order low-pass and high-pass quadrature mirror and for positive and negative frequency hilbert transform filters

$$TP_2(Z) = -\frac{1}{Z^6}$$
$$BT_2(Z) = -j\frac{1}{Z}\frac{1-b_1Z^2}{Z^2-b_1}\frac{1-a_1Z^2+a_2Z^4}{Z^4-a_1Z^2+a_2} \quad (5)$$

As shown in Fig. 14 the 2-to-1 resamplers can be brought through the filter to the filter input. This transposition has the filters operating at output rate rather than input rate and the two sample delays at the input clock rate are replaced by one sample delay at the output clock rate which changes the polynomials from polynomials in Z^2 to polynomials in Z.

The pole zero diagrams of the Bins 0-to-4 filters are shown in Fig. 15. The stop bands of the four configurations are easily identified by the cluster of zeros on the unit circle opposite the pass band interval identified by the non-minimum phase zeros characteristic of linear phase filters. Note the very high efficiency of the two-path IIR filter. The filter exhibits 7 poles and 7 zeros for the computational cost of 3 multiplies and 7-additions for every output sample or for every pair of input samples when the resampling is performed by the input 2-port commutator. In addition we can operate the filter in any of the four configurations with simple sign changes.

Note that since any stage is capable of operating with a non-hermitian symmetric spectrum with a complex impulse response then every stage past the first must also be prepared to accept complex samples from its previous stage. In this architecture the I and Q paths are coupled in the filters which now have ordered pair registers and we no longer have a pair of matching I and Q filter paths.

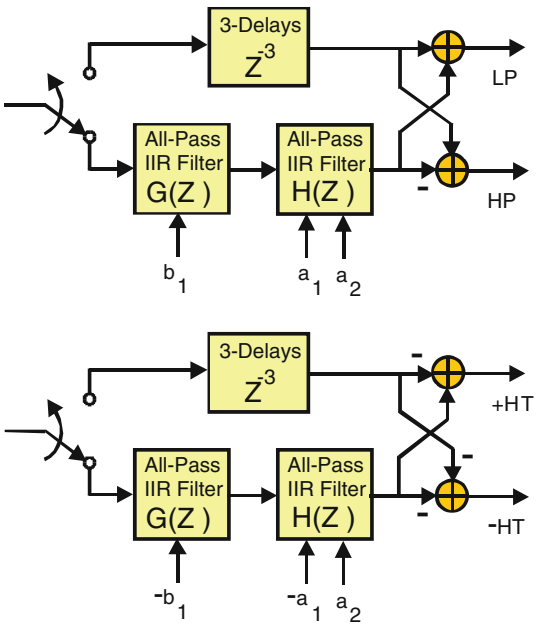

Fig. 14 Interchanging order of resamplers and filters for 7th order low-pass and high-pass quadrature mirror and for positive and negative frequency hilbert transform filters

Figure 16 illustrates the pass band intervals and the transition band intervals for the four center frequency configurations. Also shown are the aliasing of the transition bands resulting from 2-to-1 down sampling. What is not shown is the shift in center frequency for three of the four bands that also occurs due to the 2-to-1 down sampling.

Figure 17 shows the group delay and frequency response of this simple half-band filter. From the two upper subplots we note that the filter exhibits linear phase in its pass band interval and its complementary stop band interval. For this design, these intervals are 26.56 % of the normalized frequency axis. The pass band of the filters extends 1.56 % beyond the 25 % point where adjacent filters overlap. This 1.56 % overlap is required to have a signal located at the crossover boundary be in one of the four filters.

As the sample rate is lowered by the succession of half-band filters, the overlap region must increase as the signal bandwidth of interest occupies a larger fraction of the sample rate. The DDC system for which this design was performed extracted a single 50 kHz bandwidth signal from a 100 MHz sample rate. This bandwidth is one part in 2,000 and at the end of 11 half-band filter chain. The filters required to accomplish this task use 5-coefficients for filters 1-through 6, use 6-coefficients for filter 7, use 7-coefficients for filter 8 and finally 10 coefficients for filter 9. Figure 18 shows the spectra of filters 7, 8, and 9 as well as the overlap interval between adjacent filters positioned on the cardinal direction frequencies. All the filters shown here achieve 100 dB out-of-band alias rejection.

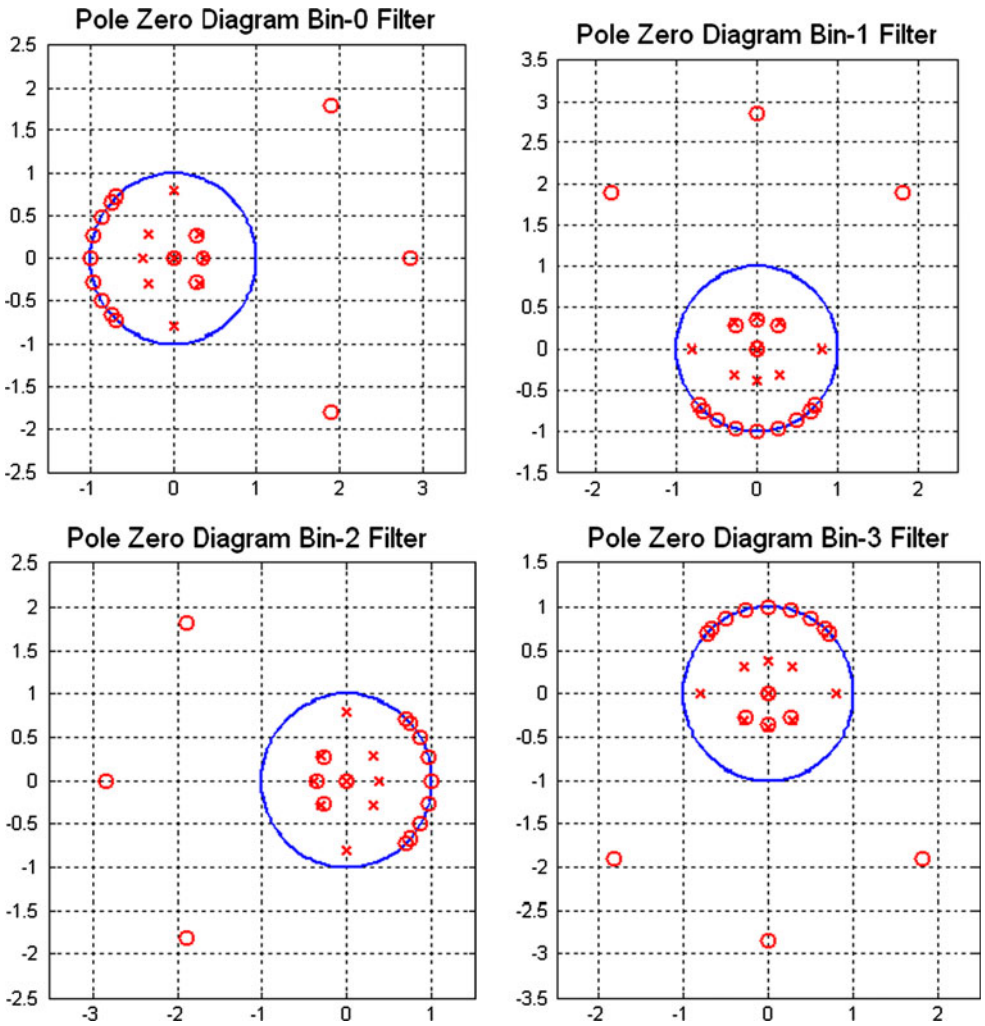

Fig. 15 Pole-zero diagrams for IIR half-band bin-0 low-pass and bin-1 positive frequency, hilbert transform filters

After the 9th filter, the overlap of adjacent filters becomes too large a fraction of the sample rate to continue with the four cardinal direction filters. Thus at the output of the 9th filter the center frequency is heterodyned to baseband and the two remaining half-band filters are standard baseband half-band filters. An arbitrary interpolator [5, 6] can be applied to the data stream after the heterodyne to obtain a final output sample rate that differs from a power of 2 sample rate reduction.

In this alternate architecture option for the DDC we have rearranged the order of filtering and heterodyne and perform the filtering with a cascaded of linear phase recursive filters. Each filter has four possible center frequencies and we select one of the four options to track the aliasing center frequency of the selected center frequency channel being down converted. This structure is shown in Fig. 19.

At each location in the half-band chain, the half-band filter has to be selected from one of 4-possible half-band filter options. As commented upon earlier, the four filters are centered at the four cardinal directions or phases, 0, $\pi/2$, $2\pi/2$, and $3\pi/2$ which we labeled as bins 0, 1, 2, and 3 successively. In the architecture of Fig. 19, every possible input center frequency is associated with a unique succession of nine sets of phase selections presented to each stage by the channel selector. The selection process proceeds in the following manner. We note that due to the effect of the sample rate halving, at each stage the relative position of the selected signal center frequency is aliased or doubled when normalized to the new output sample rate. As an example, we track the four successive locations of a signal initially located at normalized input frequency of 0.1 which places it in the bin-0 filter (-0.125 to $+0.125$) of the four possible filters. The effect of the upcoming successive alias shifts due 2-to-1 resampling is illustrated in Fig. 20.

After the first half-band filter and 2-to-1 down sample it has aliased to the normalized frequency 0.2 which places it in the Bin-1 filter ($+0.125$ to $+0.375$). Following the second half-band filter and 2-to-1 down sample it has aliased to 0.4 which is in the Bin-2 filter ($+0.375$ to $+0.625$).

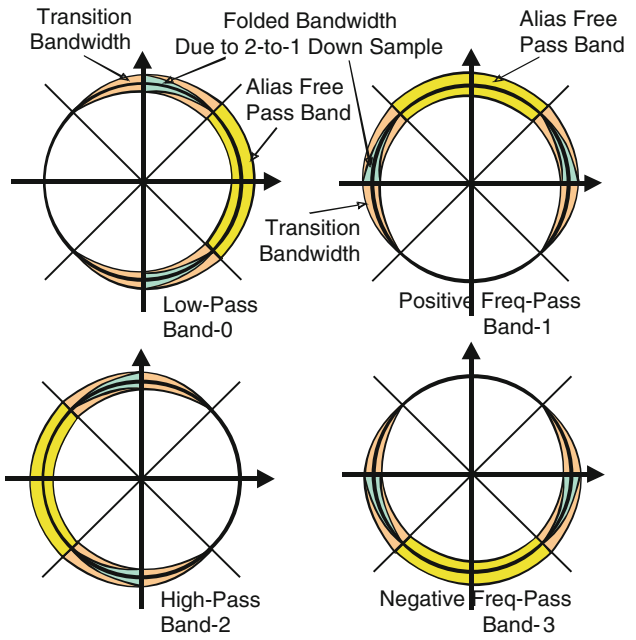

Fig. 16 Pass band and transition bands for the half-band filter at each of its four possible configurations

The third half-band filter and 2-to-1 down sample places it at 0.8 or at −0.2 which is in Bin-3 (+0.6255 to +0.875). A fourth half-band filter and 2-to-1 down sample places it at 1.6 or 0.6 or −0.4 modulo(1) which is back to Bin-2 (+0.375 to +0.625). At the end of the sequence of 2-to-1 down sample aliasing and half-band filter the signal of interest will reside at some offset centered location. In the example just cited, the final center frequency is −0.4 at sample rate $f_S/512$. A final heterodyne at this output rate, as show in Fig. 19, shifts the center of the final aliased band back to zero frequency.

We now estimate the workload for this architecture option. We first note that the first stage processes real input samples while the remaining stages up to the heterodyne process complex samples. Since the coefficients are real the workload of filters 2-through-9 is doubled as the multiplies and adds are applied to the real and imaginary parts of their input series. When 2-input samples are delivered to each filter to compute 1-output sample, the workload per input sample is half the workload per output sample. Thus the first filter with 5 coefficients requires 2.5 multiplies per input sample and the workload per input sample to the next filter is 2 times 2.5 multiplies per input but occurs at half the rate which cancels doubling due to complex input samples so that the workload for the next stage referenced to the input stage is also 2.5 multiplies per input sample. Following this reasoning, the workload for the cascade chain per path is shown in Table 6.

Here we see that, for an eleven stage cascade, the workload per path is approximately 15.1 additions per input sample and 7.5 multiplies per input sample. This workload proves to be significantly greater than the workload of the half-band filter cascade of Tables 5, and 4.2 adds and 0.16 multiplies. The reason for the disparity is that in the previous cascade, the filters had very wide transition bandwidths which required much fewer multiplies and adds in the early stages. Here, in order to overlap

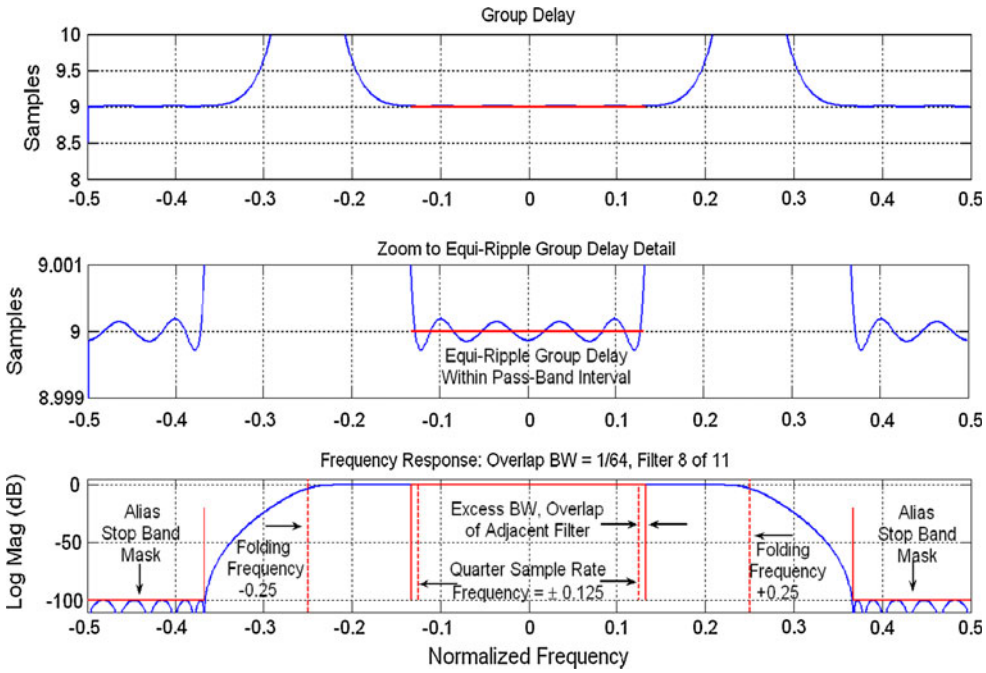

Fig. 17 Group delay, zoom to group delay detail and frequency response of half-band filter

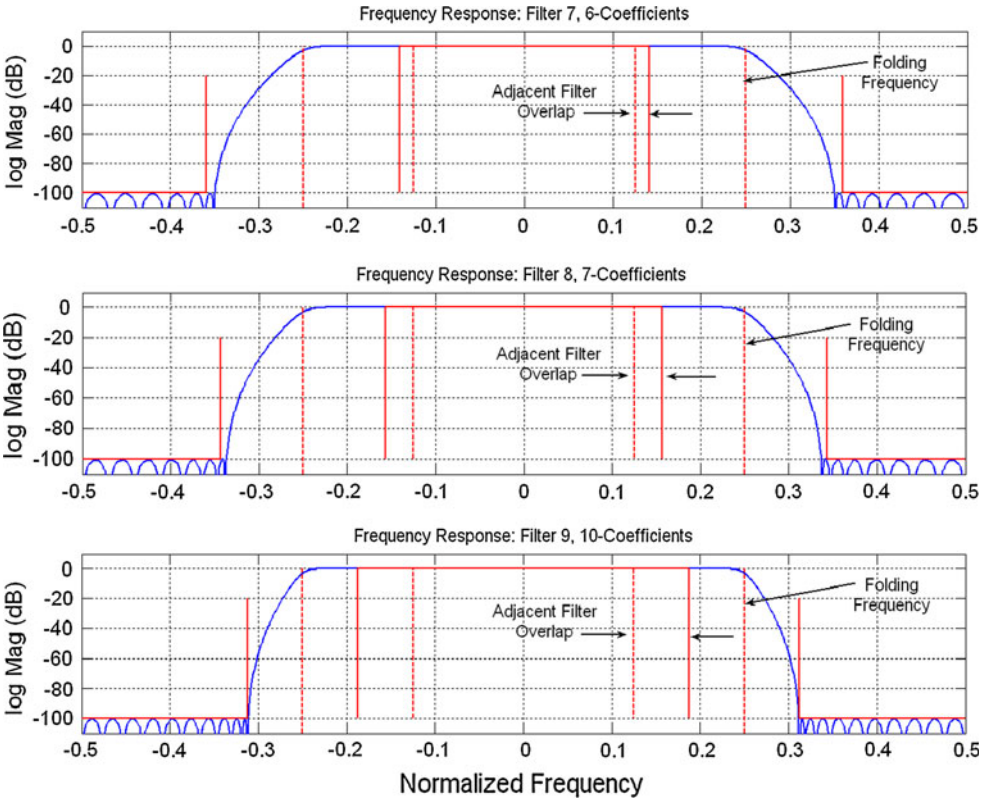

Fig. 18 Spectra of filters 7, 8, and 9 showing their wider pass band overlap with their adjacent filters

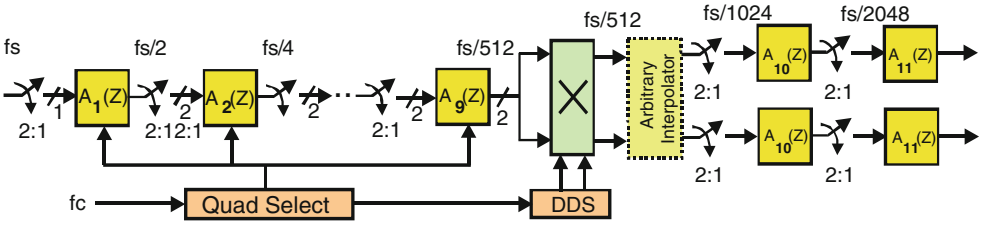

Fig. 19 Block diagram of the DDC option with cascade-half-band linear phase IIR filters and heterodyne applied near output

the pass band frequency responses of adjacent quarter band filters, they were required to have narrower transition bands which required more arithmetic to implement.

While the workload per input sample is larger than the half-band cascade of the earlier options the workload still represents an improvement over the twelve 70 bit accumulators of the 6-stage CIC filter we identified as our reference processing chain of this paper. The 12 CIC accumulators are circulating 840 bits at the input rate while the 15 20-bit additions of this last cascade is only circulating an equivalent 300 bits at the input rate. The increase in the number of multiplications is disappointing since we were looking for architectures that would reduce the multiply rate by moving the input heterodyne to the output port of the processing chain. We exchanged 2-DDC heterodyne multiplies at the input for 7.5 multiplies in the filter chain. This is not what we expected but we are still examining other architectures [7, 8] that can make this trade with a net reduction in workload.

5 Conclusion

The DDC filter structure shown in Fig. 5 is a very efficient technique to reduce bandwidth and sample rate. It performs a base banding operation and 2048-to-1 down sampling with approximately 2 arithmetic operations per real input sample. In addition to the filtering operations are the quadrature heterodyne at the input to the filter chain. In the DDC filter structure shown in Fig. 19 the quadrature mixing is moved to the output of the filter chain where its contribution to the workload is insignificant. In performing for the relocation we found that the filter workload rose to approximately 8 arithmetic operations per real input sample. These workload numbers still compare quite favorably with the CIC work load of nearly 52 real arithmetic operations per input sample distributed over the quadrature heterodyne and the very wide bit width of the many input integrators. We have not performed detailed examination of finite arithmetic effects on the alternate architectures but have used the conservative bound that

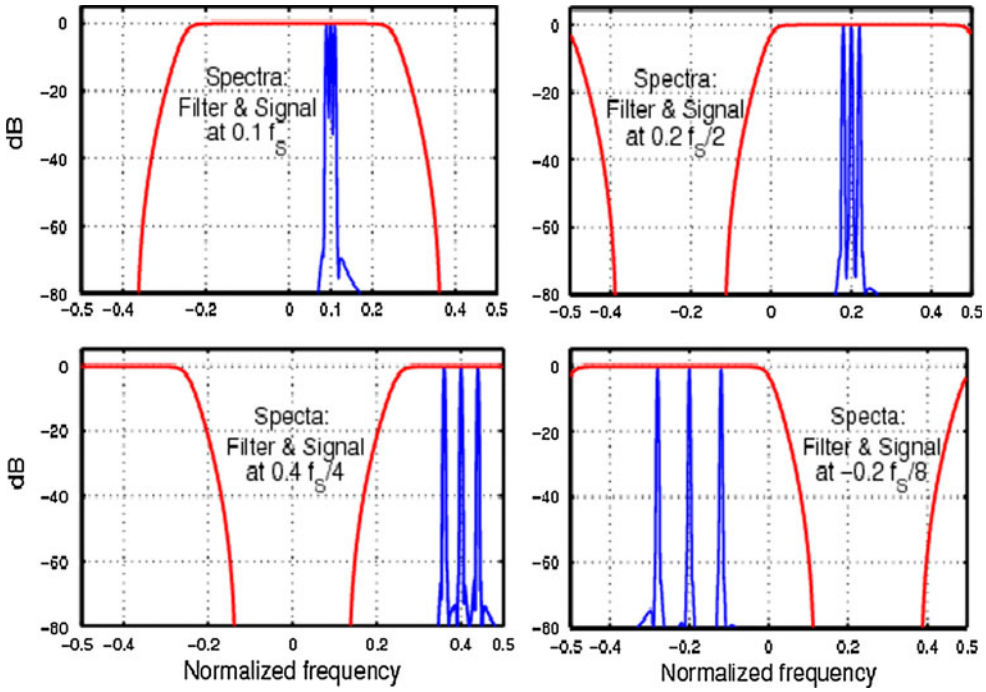

Fig. 20 Spectra of signal aliased to different sampled data frequencies in successive 2-to-1 sample rate reductions

Table 6 Filter number in IIR cascade, number of taps in filter, and number of arithmetic operations referenced to input

Filter number	1	2	3	4	5	6	7	8	9	10	11	Total
Number of coefficients	5	5	5	5	5	5	6	7	10	3	3	–
Adds	10	10	10	10	10	10	12	14	20	6	6	–
Multiplies	5	5	5	5	5	5	6	7	10	3	3	
Adds referenced to input	10/2	10/2	10/4	10/8	10/16	10/32	12/64	14/128	20/256	6/512	6/1024	15.1
Multiplies referenced to input	5/2	5/2	5/4	5/8	5/16	5/32	6/64	7/128	10/256	3/512	3/1024	7.54

the specified 100 dB filtering requirements could assuredly be satisfied with 20 bit coefficients. We also acknowledge a reviewer's comment that a thorough comparison of the proposed architectures with the CIC would require careful comparison of data flow, data memory access and bandwidth. After some consideration, the authors decided that this level of detail may be more appropriate in a follow on paper.

We finally note that the dual of the two process presented here will form a digital up converter (DUC) with the same computationally efficient work load, a work load nearly an order of magnitude smaller than the traditional CIC based DUC.

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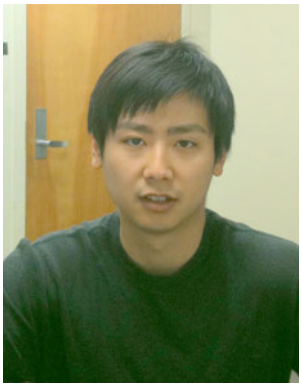

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