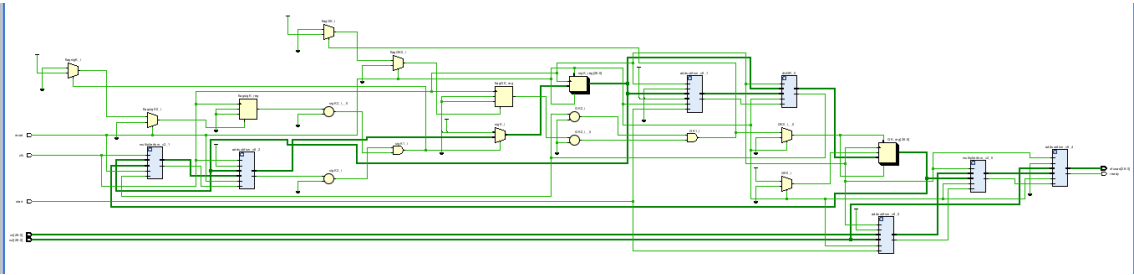


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Matrícula: 16/0031621

Prova de PCR

Questão 1)



Questão 2)

Foi observado que mesmo utilizando a arquitetura de máquinas de estados o erro MSE se manteve na escala de 0.0043, isso se deve principalmente ao truncamento feito na conversão de float 64bits para binário em ponto flutuante. (arquivos na pasta matlab).

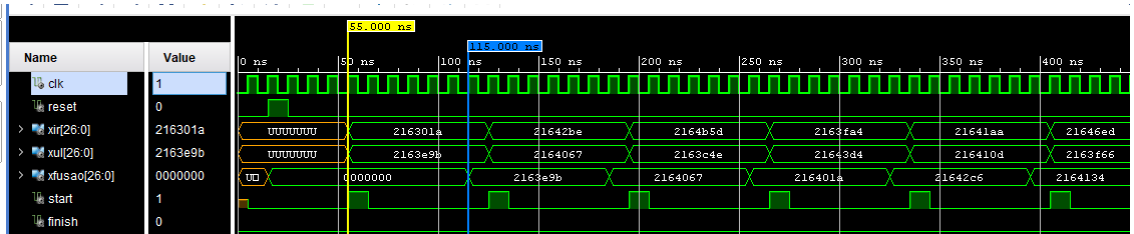
MSE =

0.00430595879255749

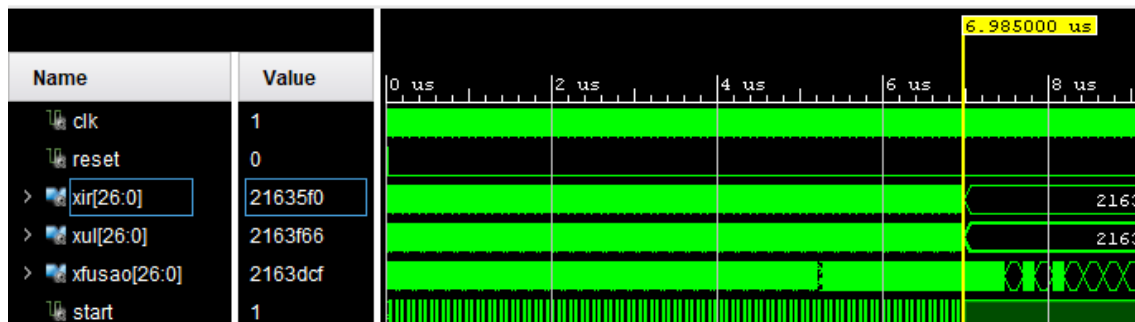
Questão 3)

De acordo com a figura abaixo a latência é $115 - 55 = 60\text{ns}$

E o throughput igual a latência de 60ns



Levou 7 us para que todos os 100 valores fossem processados.



Questão 5)

Analisando o circuito e aumentando a frequência até uma folga negativa setando os outputs_delays e os inputs_delays percebe-se que a frequência máxima é 100Mhz limitada principalmente pelos Ip_cores das RAMs

Design Timing Summary		
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.677 ns	Worst Hold Slack (WHS): 0.151 ns	Worst Pulse Width Slack (WPWS): 3.750 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 771	Total Number of Endpoints: 771	Total Number of Endpoints: 537
All user specified timing constraints are met.		

```

1 create_clock -period 10.000 -waveform {0.000 5.000} -name clk [get_ports clk]
2 set_input_delay -clock clk -max 3.00 [get_ports reset]
3 set_input_delay -clock clk -min 1.00 [get_ports reset]
4 set_input_delay -clock clk -max 3.00 [get_ports sw]
5 set_input_delay -clock clk -min 0.50 [get_ports sw]
6 set_input_delay -clock clk -max 3.00 [get_ports start]
7 set_input_delay -clock clk -min 0.50 [get_ports start]
8 set_input_delay -clock clk -max 3.00 [get_ports address[0]]
9 set_input_delay -clock clk -min 0.50 [get_ports address[0]]
10 set_input_delay -clock clk -max 3.00 [get_ports address[1]]
11 set_input_delay -clock clk -min 0.50 [get_ports address[1]]
12 set_input_delay -clock clk -max 3.00 [get_ports address[2]]
13 set_input_delay -clock clk -min 0.50 [get_ports address[2]]
14 set_input_delay -clock clk -max 3.00 [get_ports address[3]]
15 set_input_delay -clock clk -min 0.50 [get_ports address[3]]
16 set_input_delay -clock clk -max 3.00 [get_ports address[4]]
17 set_input_delay -clock clk -min 0.50 [get_ports address[4]]
18 set_input_delay -clock clk -max 3.00 [get_ports address[5]]
19 set_input_delay -clock clk -min 0.50 [get_ports address[5]]
20 set_input_delay -clock clk -max 3.00 [get_ports address[6]]
21 set_input_delay -clock clk -min 0.50 [get_ports address[6]]
22 set_input_delay -clock clk -max 3.00 [get_ports address[7]]
23 set_input_delay -clock clk -min 0.50 [get_ports address[7]]
24 set_output_delay -clock clk 8 [get_ports led[0]]
25 set_output_delay -clock clk 8 [get_ports led[1]]
26 set_output_delay -clock clk 8 [get_ports led[2]]

```

```

--!
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

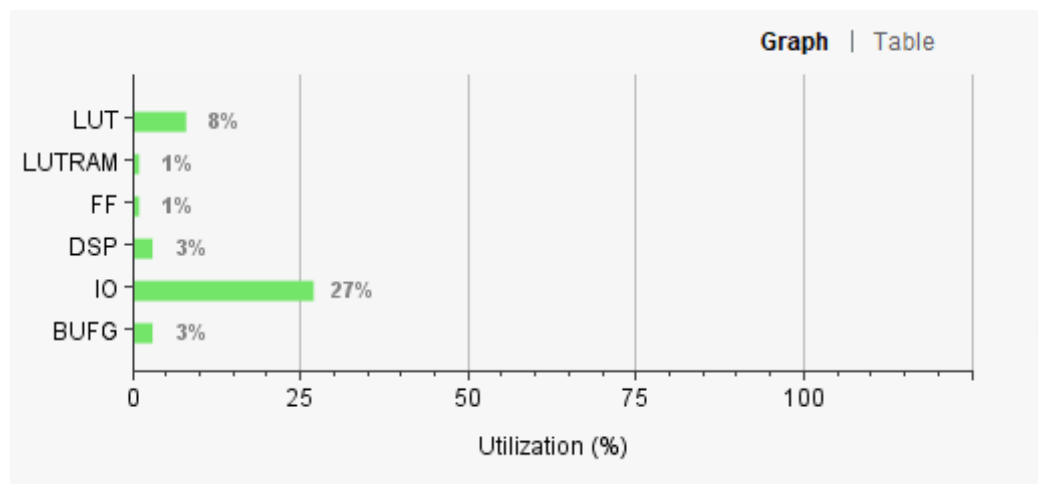
entity top_level is
    Port ( clk : in STD_LOGIC; -- clock do circuito
          reset : in STD_LOGIC; -- reset
          start : in STD_LOGIC; -- start para o inicio dos calculos
          sw : in STD_LOGIC; -- botão para multiplexar os leds entre o MSBs e os LSBs do sinal resultante
          address: in STD_LOGIC_VECTOR(6 DOWNTO 0); -- endereçamento da ROM
          led : out STD_LOGIC_VECTOR(15 DOWNTO 0); -- Leds para mostrar o sinal Xfusao
          dp : out STD_LOGIC; -- flag para informar que os calculos estão prontos
          an : out STD_LOGIC -- para ligar o dp
        );
end top_level;

architecture Behavioral of top_level is

    COMPONENT ROMxir
    PORT (
        a : IN STD_LOGIC_VECTOR(6 DOWNTO 0);
        d : IN STD_LOGIC_VECTOR(26 DOWNTO 0);
        clk : IN STD_LOGIC;
        we : IN STD_LOGIC;
        spo : OUT STD_LOGIC_VECTOR(26 DOWNTO 0)
    )

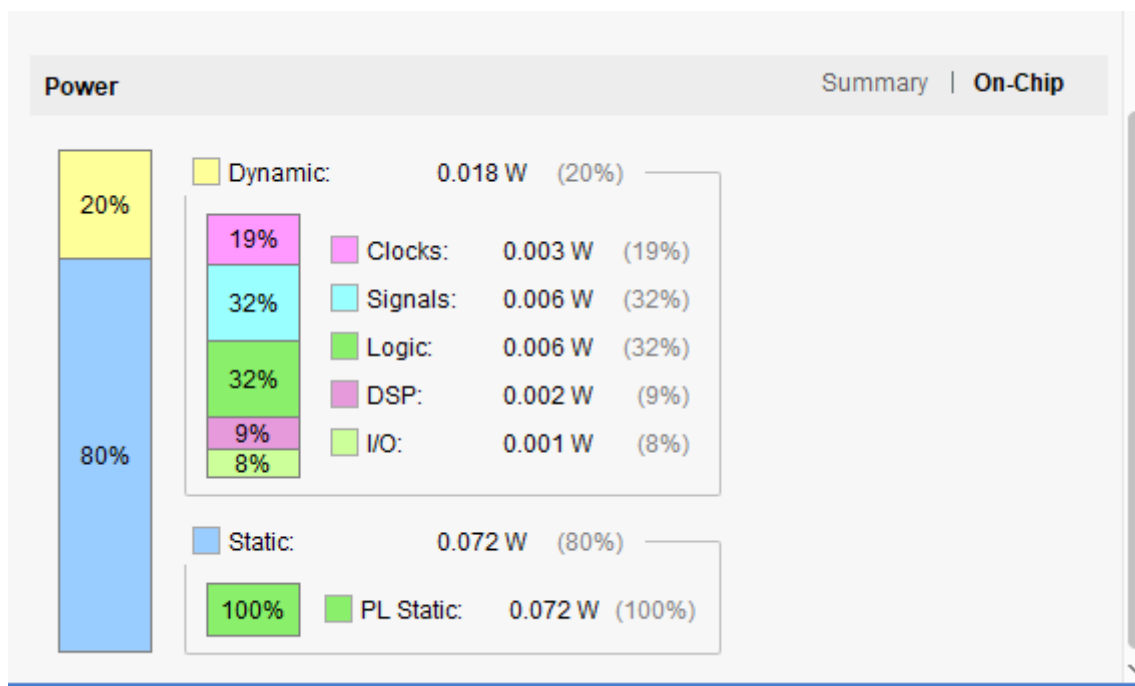
```

Questão 6)



Utilization		Post-Synthesis Post-Implementation	
		Graph Table	
Resource	Utilization	Available	Utilization %
LUT	1713	20800	8.24
LUTRAM	108	9600	1.13
FF	428	41600	1.03
DSP	3	90	3.33
IO	29	106	27.36
BUFG	1	32	3.13

Questão 7)



Dinâmica: 0.018 W

Estática: 0.072W

Total: 0.09W

