Curriculum Vitae

Yangdong Deng

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Institute of Microelectronics
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Research Interests

Machine learning for industry equipment prognostics, High performance computer architecture, Parallel algorithms

Education

Ph.D.	Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, USA, December 2006
Master of Engineering	Department of Electronic Engineering, Tsinghua University, Beijing, April 1998
Bachelor of Engineering	Department of Electronic Engineering, Tsinghua University, Beijing, July 1995

Work Experience

Associate Professor	Institute of Microelectronics, Tsinghua University, Beijing	*Mar'08 – present*
Software Architect	Magma Design Automation	*Mar'05- Mar'08*
Senior Software Engineer	Incentia Design Automation	*May'04 - Mar'05*

Awards and Honors

- Best paper award, International Conference on Computer Design, 2013
- NVIDIA Partner Professor Award, 2010, 2009
- Foundation for Key Faculty Members, Tsinghua University, 2008
- Deng Feng Foundation, 2008
- NEC Project Technical Achievement Award, Magma Design Automation, 2006
- Innovation Award, Incentia Design Automation, 2005

Ongoing Research Projects

- **Multi-Physics Signal Analysis and Health Management for Railway Vehicles** sponsored by Special Fund for Basic Research on Scientific Instruments of the National Natural Science Foundation of China (**Co-PI**)
  - Developing machine learning based technologies for detection, diagnosis, and prediction of machine failures on modern railway vehicles

- **Railway Equipment Fault Prediction and Health Management** sponsored by Major Project of CRRC Corporation Limited (**Co-PI**)
  - Developing next generation big-data driven prognostics technologies for railway vehicles
- **Computer Architecture for Bayesian Cognition** sponsored by Xilinx (**PI**)
  - Developing computer architectures supporting native stochastic sampling for human-level cognition computations

Finished Projects

- **Key Technologies for Multi-functional Vehicle Bus Controller** sponsored by China CNR Corporation, 2012 – 2014, (**PI**)
  - Designed an IEC61375 compatible Multi-functional Vehicle Bus (MVB) controller (Already deployed in high-speed trains, locomotives and subway trains operating in China, Egypt, and Argentina railways)
- **Parallel Computer Architecture for Ray-Tracing** sponsored by China National Science Foundation, 2013 – 2016, (**PI**)
  - Developed microarchitectural technologies to enable real-time ray-tracing (World's first FPGA based GPU microarchitecture simulator, ICCD'13 best paper award)
- **Essential Algorithmic Techniques for Ray-Tracing** sponsored by Tsinghua Independent Research Project, 2012 – 2015, (**PI**)
  - Developed highly efficient ray-tracing algorithms including a fully parallel construction algorithm for spatial acceleration structures
- **CUDA Excellence Center at Tsinghua University** sponsored by NVIDIA, 2010 – 2014, (**PI**)
- **Parallel RTL Simulation with Graphics Processing Units** sponsored by Intel, 2012 – 2013, (**PI**)
- **Massively Parallel Logic Simulation with Graphics Processing Units** sponsored by Intel, 2011 – 2012, (**PI**)
- **System-Level Simulation for System-on-Chips** sponsored by Intel, 2009 – 2011, (**PI**)

Invited Talks and Lectures

- Towards Human Level Cognition with Stochastic Bayesian Computing, Tsinghua-Xilinx Workshop on FPGA based Machine Leaning, 2017.
- Toward Ray-Tracing on Mobile Platforms, GPU Technology Conference, 2015.
- Mining Effective Parallelism from Hidden Coherence for GPU based Path Tracing, GPU Technology Conference, 2014.
- Massively Parallel Logic Simulation on Modern GPUs, Synopsys, Shanghai, 2012
- Hardware/Software Co-Design for System-on-Chips, China Computer Federation CCF Advanced Disciplines Lectures, 2011.
- Massively Parallel Logic Simulation, GPU Technology Conference, 2012
- Morphing GPU into a Network Processor, GPU Technology Conference. 2011.
- Parallel Simulation on Heterogeneous Processors, 1st GPU Computing Workshop,

2011.

- Parallel Processing on Modern Many-Core Processors, Tilera Workshop, 2011
- Into a Parallel New World, Keynote Speech, GPU Technology Conference at Taiwan, 2011
- General Purpose Computing with Modern GPUs, NVIDIA CUDA Technology Lecture Series at 10 top China Universities, 2009-2010

Media Interview

- Live video interview, IT168 (China's largest IT Internet media), 2013, 2012, 2011
- Interview by CSDN.NET (China's largest online community for programmers), 2012, 2010

Teaching

● Embedded System Architecture	School of Software, Tsinghua University, 2013 -
● Advances in Microelectronics	Institute of Microelectronics, Tsinghua University, 2008, 2009, 2010, 2011
● Computer Organization	Institute of Microelectronics, Tsinghua University, 2014
● General Purpose Programming with GPUs	One-week tutorial on GPU computing, 2009, 2010

Professional Activities

● Invited course expert and editor	Parallel Programing for Many-Core Processors, China Excellent Course Center, 2010 – present
● NVIDIA Partner Professor	http://www.nvidia.com/object/professor_partners_bios_yangdong.html
● Co-chair	Int'l Workshop on Frontier of GPU Computing, 2010, 2011, 2012
● Guest editor	VLSI Design Journal, Jan. 2012
● Technical program committee	IEEE Computer Society Annual Symposium on VLSI (2009-present), HPC China (2013), ASP-DAC(2012), ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (2010), IEEE/ACM Great Lakes Symposium on VLSI (2010)

Publications

Books

1. Y. Deng and J. Huang, "GPU Machine Learning," China Machine press and

Elsevier Publishing Company, in press.
2. Y. Deng, M. Zhu and C. Liu, "Introduction to OpenCL Programming for Heterogeneous Processors," China Machine press, 2016.
3. Y. Deng and W. Maly, "3-D VLSI – A 2.5-D Integration Scheme," Springer Verlag/Tsinghua University Publishing House, 2010.
4. Z. Wang and Y. Deng, "Structural VLSI Design and High Level Synthesis," Tsinghua Publishing House, 1998.

Invited Surveys and Book Chapters

1. Yangdong Deng, Shuai Mu, "A Survey on GPU Based Electronic Design Automation Computing," Foundation and Trends in Electronics Design Automation, Now Publishers, 2013, pp. 1-180.
2. Y. Deng, D. Wang, and Y. Zhu, "Asynchronous Parallel Logic Simulation on Modern Graphics Processors," Why Scientists and Engineers Need GPUs, Springer, 2012.
3. Y. Deng, "Hardware/Software Co-Design for System-on-Chips," Communications of China Computer Federation, Feb. 2012.

Representative Conference Papers

1. Z. Li, L. Liu, Y. Deng, S. Yin, Y. Wang, and S. Wei, Aggressive Parallelization of Irregular Applications on Reconfigurable Architectures, 44th International Symposium on Computer Architecture (ISCA), Toronto, Canada, 2017.
2. Z. Li, Y. Deng, and M. Gu: Path compression kd-trees with multi-layer parallel construction a case study on ray tracing. ACM SIGGRAPH Symposium on Interactive 3D Graphics and Games (I3D), 2017.
3. X. Wang, Y. Deng, G. Zhang, and Z. Wang, Apparent resolution enhancement for near-eye light field display, SIGGRAPH Asia Mobile Graphics and Interactive Applications, 2015.
4. X. Liu, Y. Deng, Y. Ni, and Z. Li, FastTree: a hardware KD-tree construction acceleration engine for real-time ray tracing. DATE 2015.
5. Y. Wang, C. Liu, and Y. Deng, A feasibility study of ray tracing on mobile GPUs, SIGGRAPH Asia 2014 Mobile Graphics and Interactive Applications, 2014.
6. T. Wang and Y. Deng, Mining Effective Parallelism from Hidden Coherence for GPU Based Path Tracing, SIGGRAPH Asia, 2013.
7. K. Fang, Y. Ni, J. He, Z. Li, S. Mu, and Y. Deng, FastLane: An FPGA Accelerated GPU Microarchitecture Simulator, IEEE International Conference on Computer Design, 2013. (**Best paper award**)
8. H. Qian and Y. Deng, Accelerating RTL Simulation with GPUs, IEEE/ACM International Conference on Computer-Aided Design, Nov. 2011.
9. Y. Zhu, Y. Deng, and Y. Chen, Hermes: An Integrated CPU/GPU Microarchitecture for IP Routing, Design Automation Conference, 2011.
10. S. Mu, C. Wang, M. Liu, D. Li, M. Zhu, X. Chen, X. Xie, and Y. Deng, Evaluating the Potential of Graphics Processors for High Performance Embedded Computing" Design Automation and Test Europe, 2011.

11. K. Kang, and Y. Deng, Scalable Packet Classification via GPU Meta-programming, Design Automation and Test Europe, 2011.
12. J. Zhao, X. Zhang, X. Wang, Y. Deng, and X. Fu, Exploiting Graphics Processors for High-performance IP Lookup in Software Routers, INFOCOM, 2011.
13. B. Wang, Y. Zhu, and Y. Deng, Distributed Time, Conservative Parallel Logic Simulation on GPUs, Design Automation Conference, Jun. 2010.
14. J. Xue, X. Jiao, Y. Deng, H. Qian, D. Zeng, G. Li, and Z. Yu, Massively Parallel Finite Element Simulator for Full-Chip STI Stress Analysis, First International Workshop on Frontier of GPU Computing, Jun. 2010.
15. S. Mu, J. Lu, N. Zhang, X. Zhang, Y. Deng, and S. Zhang, IP Routing Processing with Graphic Processors, Design Automation and Test Europe, Apr. 2010.
16. Y. Deng, B. Wang, and S. Mu, Taming Irregular EDA Applications on GPUs, IEEE/ACM International Conference on Computer-Aided Design, Nov. 2009.
17. J. Xue, L. Yang, Y. Deng, Z. Ye, and Z. Yu, Layout-Dependent STI Stress Analysis and Stress-Aware RF/Analog Circuit Design Optimization, IEEE/ACM International Conference on Computer-Aided Design, Nov. 2009.

Representative Journal Papers

1. Y. Deng, Y. Ni, Z. Li, S. Mu S. and W. Zhang, Toward Real-Time Ray Tracing: A Survey on Hardware Acceleration and Microarchitecture Techniques, ACM Computing Surveys. Accepted.
2. Jin Huang, Qingmin Huang, Yangdong Deng, and Ye-Hwa Chen. "Toward Robust Vehicle Platooning With Bounded Spacing Error." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 36, no. 4 (2017): 562-572.
3. Jin Huang, Yangdong Deng, Qinwen Yang, Jiaguang Sun, An Energy- Efficient Train Control Framework for Smart Railway Transportation: IEEE Transactions on Computers 65, no. 5 (2016): 1407-1417.
4. Y. Jiang, H. Zhang, Z. Li, Y. Deng, X. Song, M. Gu, and J.-G. Sun: Design and Optimization of Multiclocked Embedded Systems Using Formal Techniques. IEEE Trans. Industrial Electronics 62(2): 1270-1278 (2015)
5. S. Mu, Y. Deng, et. al. “Orchestrating Cache Management and Memory Scheduling for GPGPU Applications”, IEEE Transaction on Very Large Scale Integration, 2014.
6. H. Qian, Y. Deng, B. Wang, and S. Mu, “Towards Accelerating Irregular EDA Applications with GPUs,” Integration, the VLSI Journal, 2012.
7. J. Xue, Y. Deng, Z. Ye, et al. “A Framework for Layout-Dependent STI Stress Analysis and Stress-Aware Circuit Optimization,” IEEE Transaction on Very Large Scale Integration, Mar. 2012.
8. G. Sun, S. Xu, X. Wang, D. Wang, E. Tang. Y. Deng, and S. Chen, “A High-throughput, High-Accuracy System-Level Simulation Framework for System-on-Chips,” VLSI Design Journal, Jan. 2012.
9. Y. Zhu, B. Wang, and Y. Deng, “Massively Parallel Logic Simulation with GPUs,” ACM Transaction on Design Automation of Electronics Systems, Vol.16, No.3,

June, 2011.
10. X. Chen, Y. Deng, X. Chen, X. Li, and J. Tian, “GPU Based High Speed FIR Digital Filtering,” Journal on Computer Aided Design and Graphics, Sep. 2010.
11. J. Xue, T. Li, Y. Deng, and Z. Yu, “Full-Chip Leakage Verification for 65nm CMOS Node and Beyond,” Integration, the VLSI Journal, Sep., 2010.
12. Y. Deng and W. Maly, “2.5-Dimensional VLSI System Integration,” IEEE Transaction on VLSI, Aug., 2005.