Layout-Dependent STI Stress Analysis and Stress-Aware RF/Analog Circuit Design Optimization

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Abstract

With the continuous shrinking of feature size, various effects due to shallow-trench-isolation (STI) stress are becoming more and more significant. The resulting nonuniform distribution of stress affects the MOSFET characteristics and hence changes the circuit behavior. This paper proposes a complete flow to characterize the influence of STI stress on performance of RF/analog circuits based on layout design and process information. An accurate and efficient FEM-based stress simulator has been developed to handle the layout dependence. A comprehensive MOSFET model is also proposed to capture the effects of STI stress on mobility, threshold voltage, and leakage current. The influence of layout-dependent STI stress on the circuit performance is further studied, and the corresponding optimization strategies to circuit design are discussed. A realistic PLL design realized using 90nm CMOS technology is used as a test case for the proposed approach.

Ⅰ. Introduction

As CMOS technology is moving to sub-90nm nodes, the mechanical stress, which is used to be the secondary concern of the circuit design, now becomes one of the major factors determining circuit performance. Different from other intentional mechanical stresses, STI stress, which is exerted by STI wells on active region of the device, is inevitably formed and has increasingly significant impact on device behavior, especially in aggressively scaled-down CMOS technology.

A few papers [1-5] have reported the influence of STI stress on device characteristics. In [6-8], some empirical models have been proposed, which mainly focus on relatively simple cases. Moreover, these studies are all conducted at device level, and thus do not consider the effects on MOSFET characteristics due to complex STI stress distribution on a real die. It is desirable to develop an accurate and efficient method to analyze the influence of the STI stress on device/circuit performance comprehensively at a full-chip level.

ICCAD'09, November 2–5, 2009, San Jose, California, USA.

Mobility change, which is responsible for the driving current and many other device behaviors, is one of the most important factors induced by STI stress. The most widely used Berkeley Short-channel IGFET Model (BSIM) SPICE model (revision 4.6 and higher) does not fully consider the influence of two-dimensional (2-D) STI stress. Recently, Kahng proposed a model that relates the transistor mobility to stress induced by the width of STI regions [9-10]. However, this model focuses only on simplistic situations, so it cannot be applied to complex layout analysis.

Leakage current grows significantly with the ever-shrunk gate length, and it is also affected significantly by STI stress. In [11-12], the effects of the STI stress on leakage current at 130nm and 65nm nodes have been discussed. However, to our knowledge, quantitative analysis and models on these effects are not available.

Besides, the circuit performance will change under the influence of STI stress. The delay of digital circuits under the influence of the width change of STI is studied in [10] and [13]. However, [9, 10, 13] only focus on simplistic 1-D layout models for standard-cell circuits. It is known that STI stress is closely dependent on the layout geometry. For RF/analog circuits, in which the layout geometry is much more complicated and cannot be described with 1-D models, no literature has been found to address STI stress issue.

In order to analyze STI stress accurately, numerical TCAD tools, such as Taurus, are needed to perform the simulation for STI stress analysis. Due to their excessive requirements for computing resources, such TCAD tools can only be applied to very simple layouts. To perform numerical simulations to get the stress profile for large cells, certain simplification together with appropriate methodology must be introduced to accelerate the simulation process.

In this paper, a complete flow of the methodology to analyze MOS characteristics and the circuit performance under the effects of STI stress is proposed. We also present corresponding optimization strategies for RF/analog circuit design. The contribution of our work is as follows:

- An efficient stress simulator is developed. It facilitates characterizing the layout-dependent STI stress accurately.
- Accurate physics-based MOSFET models including mobility, threshold voltage and leakage current are proposed. The models make it possible to accurately and efficiently characterize performance of devices and circuits under the impact of STI stress.
- The influence of STI stress on the performance of RF/analog circuits is quantitatively analyzed by considering the effects of such factors as the

number of fingers and mismatch. The corresponding optimization strategies are also proposed.

The rest of this paper is organized as follows. Section Ⅱ introduces some basic knowledge related to STI stress analysis. Section Ⅲ discusses the developed simulation tool, which provides STI stress distribution according to different layouts. Considering the layout-dependent parameters, Section Ⅳ presents the physics-based models including mobility and threshold voltage as well as leakage current. In section Ⅴ we discuss the performance change of RF/analog circuits under the effects of STI stress and propose some optimization strategies. Section Ⅵ presents experimental results for model verification and the influence of STI stress on circuit performance. Finally, conclusions are drawn in section VII.

Ⅱ. Preliminaries

A. Process of STI

The process for STI formation starts with the growth of a thermal pad oxide on silicon substrate, followed by the deposition of a silicon nitride layer. A pattern is applied and trenches are etched through the nitride and oxide layers. A corner-rounding oxidation is then performed in order to reduce the electric field at corners. Next, the trenches are filled with a deposited silicon dioxide film and the oxide is then planarized using masked reactive ion etch followed by chemical mechanical polishing. After the exposed nitride is removed in a hot-phosphoric bath, well implants are performed, followed by gate oxidation and gate electrode formation. In this process, STI stress builds up during subsequent temperature-ramps due to the mismatch between thermal expansion coefficients of silicon and oxide [14].

B. Description of STI Stress and Relationship between Stress and Strain

STI stress tensor is defined by the three stress vectors [15] as follows:

$$\hat{T} = \begin{bmatrix} \sigma_x & \tau_{xy} & \tau_{xz} \\ \tau_{yx} & \sigma_y & \tau_{yz} \\ \tau_{zx} & \tau_{zy} & \sigma_z \end{bmatrix} \quad (1)$$

where σ_i (i=x,y,z) is stress component normal to the unit cube face and τ_{ij} (i,j=x,y,z) is shear component directed toward j on the orthogonal face to i. The impact of stress is mostly attributed to σ. since $\hat{T}$ is symmetric，There are altogether six independent variables.

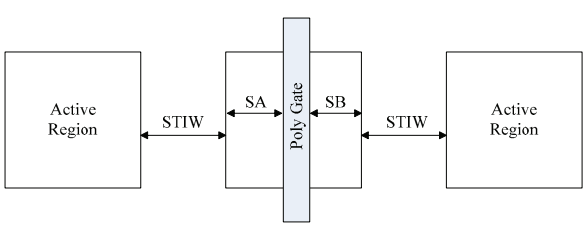

Fig.1. some layout parameters related to STI stress

Since strain is the direct cause of the change of MOSFET characteristics, we need to change the value of stress to strain through equation (2) [16] when the STI stress of a MOSFET is obtained.

$$\begin{pmatrix} \varepsilon_x \\ \varepsilon_y \\ \varepsilon_z \\ \gamma_{yz} \\ \gamma_{zx} \\ \gamma_{xy} \end{pmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{12} & 0 & 0 & 0 \\ C_{12} & C_{11} & C_{12} & 0 & 0 & 0 \\ C_{12} & C_{12} & C_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{44} \end{bmatrix} \begin{pmatrix} \sigma_x \\ \sigma_y \\ \sigma_z \\ \tau_{yz} \\ \tau_{zx} \\ \tau_{xy} \end{pmatrix} \quad (2)$$

In equation (2)，the transformation matrix is the tensor of elastic stiffness constants for silicon, and tensile stress is used with a positive sign and compressive stress with a negative sign.

C. Existing Models

The influence of STI stress has been investigated in many papers, some of which show the layout dependence of MOS parameters and the necessity of new models to cover this change. Their uniform recognition of the effects of STI stress is that the NMOS current decreases and the PMOS current increases under the compressive stress of STI [2].

Currently, the widely used BSIM4 model only contains the distance from the MOS channel to the STI boundary (*SA* and *SB*) when considering the STI effects (Fig.1). It shows that with the decrease of SA and SB, STI stress will increase, which increases the driving current of PMOS and decreases that of NMOS. Other parameters such as the width of STI (*STIW*) are not included in the BSIM4 model.

Tsuno in [17] introduced the parameters related to STI effects through measurement, and concluded that *STIW* could influence driving current by up to 10%. This result shows that the device model without the consideration of the *STIW* effects could not describe the characteristics of MOSFET accurately. Unfortunately, Tsuno did not conduct the model building work in this paper.

Recently, Kahng et al. [9-10] studied the *STIW* effects in detail and proposed a corresponding mobility model. Nevertheless, this model is not physics-based. In addition, this mobility model contains only two parameters and lacks the 2-D analysis, thus its application is limited to a great degree. For the accurate description of the characteristics of MOSFET with the actual layout, a more efficient model should be developed.

Tan [11] for the first time proposed the effect of STI stress on leakage current in 0.13um technology. The conclusion is that when *SA* decreases, or equivalently when STI stress increases, the NMOS leakage current decreases and the PMOS leakage current increases. Joshi [12] observed the obvious influence of STI stress in 65nm technology. However, in both [11] and [12] the analysis and modeling of the effects of STI on leakage current are not fully performed.

Ⅲ. STI Stress Simulation

Our STI stress simulation tool is based on the finite element method (FEM). During the simulation process, as the direct solution of the entire system is not feasible due to the large size of the mesh, the problem can be partitioned into smaller sub-regions and be solved iteratively.

Based on the STI process described in Section II, our simulation tool takes into account such factors as thermal expansion mismatch, intrinsic stress, growth of materials, and viscoelasticity. The stress due to the thermal expansion mismatch is the major stress source resulted from the difference of thermal expansion properties between different materials. It can be calculated from the temperature change and thermal expansion coefficients. Thin films such as nitride film are generally highly stressed and also have an important effect on the overall stress distribution. Volume expansions during the oxidation process for oxide liner in the STI process and mechanical stress is accumulated, which also influences the initial strain of the liner layer. In our simulator, the viscoelasticity at higher temperature due to nitride and silicon dioxide is also considered.

Fig.2 shows a small layout region taken from a real circuit. This non-rectangular active shape is typical in real circuits. Such a shape, although it is not the most complex one we have identified from layouts, already could not be analyzed with existing models. On the other hand, no matter how complex the layout shape is, the device characteristics can be analyzed after the STI stress is obtained with our simulation tool. As an actual gate level simulation case, Fig.3 and Fig.4 show the layout of an SR flip-flop standard cell and the corresponding STI stress simulation results using our TCAD simulator [18].

Ⅳ. Model of MOSFET Characteristics Related to STI Stress

With the simulation tool developed, we could get the accurate channel stress tensor for each transistor on the die. Then we need to develop the corresponding model including mobility, threshold voltage and leakage current to accurately describe the relationship between STI stress and the characteristics of MOSFET.

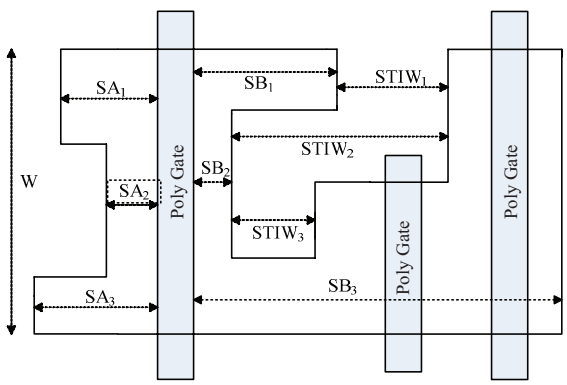

Fig.2. non-rectangular active region

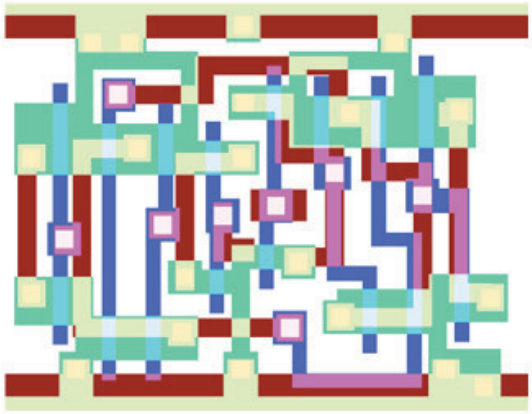

Fig.3. The layout of an SR flip-flop

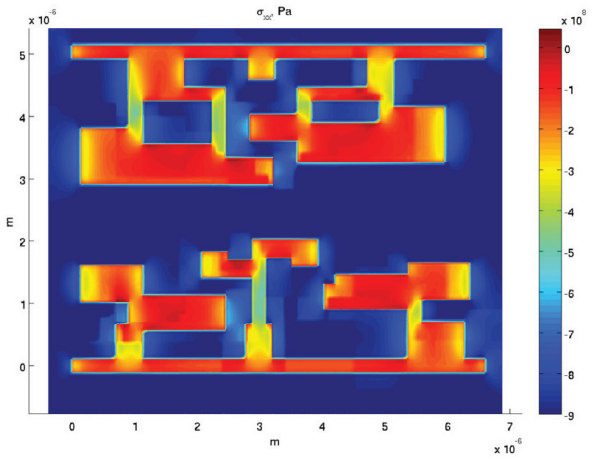

Fig.4. Simulation result of in-plane stress profile corresponding to the layout near the silicon surface using our simulator

Through quantum mechanical calculation [19] and experiments [20], it has been recognized that stress could induce shifts and splits in the energy bands of silicon. The change of energy bands of carriers leads to the change of mobility of carriers.

For electrons, the conduction-band change in silicon induced by STI strain can be calculated as follows:

$$\Delta E_c^{(i)} = \Xi_d \cdot (\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) + \Xi_u \varepsilon_{ii}, \qquad i = x, y, z \tag{3}$$

where $\Xi_d = 7.3eV$, $\Xi_u = 1.13eV$ [18] and ε_i (i=x,y,z) is the strain caused by STI stress.

The split in the conduction bands causes the change of the probability of energy band occupation, which further influences the mobility of electrons. By taking the weighted average of mobility tensors of each valley in E~k space, the mobility change could be obtained as follows [21]:

$$\mu_{STI} = \sum_{i=1}^{3} p^{(i)} \cdot \hat{\mu}_0^{(i)} \tag{4}$$

where $\hat{\mu}_0^{(i)}$ is the original mobility tensor of the i th valley. $p^{(i)}$ is the probability of the i th valley. Its expression is as follows [21]:

$$p^{(i)} = \frac{n^{(i)}}{\sum_{i=1}^{3} n^{(i)}} \tag{5}$$

$$n^{(i)} = N_c^{(i)} \cdot \exp[\frac{\Delta E_c^{(i)}}{k_B T}] \quad (6)$$

where N_c is the effective density of conduction band. k_B and T denote the Boltzmann's constant and ambient temperature, respectively.

For holes, the STI stress causes the splitting of degenerate valence bands at the Γ point [22], which can be calculated as follows:

$$\Delta E_v = \Xi_h \cdot (\varepsilon_x + \varepsilon_y + \varepsilon_z) \quad (7)$$

where $\Xi_h = 2.21\text{eV}$ and ε_i (i=x,y,z) is the strain caused by STI stress.

This band splitting reduces the occupation of holes in the lowered sub-valleys and therefore changes the effective mass of holes, which can be calculated as follows:

$$(m_{eff})^{3/2} = m_{hh}^{3/2} + m_{hl}^{3/2} \exp(-\frac{\Delta E_V}{k_B T}) \quad (8)$$

where m_{hh} and m_{hl} are the effective hole masses of the heavy and light bands, respectively.

Then the mobility under the influence of STI stress can be obtained as follows:

$$\mu_{STI} = \mu_0 \cdot \left(m_{eff}^{3/2}\right) / \left(m_{hh}^{3/2} + m_{hl}^{3/2}\right) \quad (9)$$

where μ_0 is the original mobility without considering the effects of the STI stress.

The shifts and splits of the conduction band and the valence band induced by STI stress naturally influences the work function, and thus the flat-band voltage, further influences the threshold voltage. Therefore, we modify the threshold voltage model [23] by adding the impact of STI stress on the energy bands of carriers as follows:

$$\begin{aligned} V_{th} = {} & \phi_{ms0} - \frac{Q_{ss}}{C_{ox}} + \frac{Q_B}{C_{ox}} + \left(\phi_{s0} - \Delta\phi_s\right) \\ & + \gamma\left(\phi_{s0} - V_{bs}\right)\left(1 - \lambda\frac{X_d}{L_{eff}}\right) + \Delta V_{NWE} + \Delta E_{C,V} \end{aligned} \quad (10)$$

where, ϕ_{ms0} is the original metal-semiconductor work function difference without considering STI stress effects. Q_{SS} is the fixed oxide charge, Q_B is the depletion region charge, ϕ_{s0} is the zero bias surface potential, $\Delta\phi_s$ is the reduction of the surface potential of short channel device from its zero bias value due to short channel effect (SCE) like drain induced barrier lowering (DIBL), γ is the body effect factor, $C_{ox} = \varepsilon_{S_iO_2} / t_{ox}$ is the oxide capacitance per unit gate area. X_d represents the depletion thickness, λ is a fitting parameter and ΔV_{NWE} is the narrow width correction factor [23]. $\Delta E_{C,V}$ is the conduction band shift of electrons or the valence band shift of holes, which is calculated through equation (4) and equation (9). Now the accurate threshold voltage under the influence of the STI stress can be obtained through Eq.11.

Because the subthreshold leakage has an exponential dependence on V_{th}, the variation of V_{th} has a significant effects on leakage current. Equation (11) is the modified model based on [24]. Here we remove the fitting term of layout parameters SA and SB and use the mobility model and threshold voltage model proposed above to reflect STI stress.

$$\begin{aligned} I_{\text{sub}} = {} & \frac{\alpha_{\text{sub}}\mu\sqrt{q\varepsilon_{\text{Si}}N_{\text{cheff}}\left(W^2 + \alpha_W W\right)/\Phi_s}}{\left(V_{\text{ds}}^2 + \alpha_{V1}V_{\text{ds}} + \alpha_{V2}\right)\exp\left(\alpha_{L1}L_{\text{eff}}^2 + \alpha_{L2}L_{\text{eff}}\right)} \\ & \left(1 - \exp\left(-\frac{V_{\text{ds}}}{V_T}\right)\right)\exp\left(\frac{V_{\text{gs}} - V_{\text{th}}}{nV_T}\right) \end{aligned} \quad (11)$$

where Φ_s is the surface potential, n is the subthreshold swing, $V_T = k_B T / q$ and N_{cheff} is the doping density of the channel.

Ⅴ. Analysis and Optimization of RF/Analog Circuits Considering STI Stress effects

The change of device characteristics due to STI stress effects naturally causes the change of circuit performance. Existing works have focused on the delay of digital circuits [9-10]. The influence of STI-induced stress on RF/analog circuits is studied in this paper. Corresponding optimization strategies are also proposed.

The process of the circuit performance analysis is as follows: first, the STI stress of each MOSFET is obtained using our simulator. Then the change of mobility under the impact of the STI stress is calculated through the model proposed in section Ⅳ. We then add a so-called influence factor of mobility into the MOSFET model and modify the original circuit netlist by setting the influence factor for every MOS transistor. In this way, the effects of layout-dependent STI stress on the circuit performance can be obtained through circuit simulation.

A. The Effects of Circuit Placement

Because different placement of a design will lead to varying STI stress distribution, the effects of layout placement on STI stress is discussed in this part. Simultaneously, according to the result of this study, some adjustment to the layout placement could be made to improve the circuit performance.

Kahng [9-10] presented a method to optimize the delay of digital circuits. During the design of the digital circuits, the layout of standard cell is fixed and thus the *SA* and *SB* are constant. In this way, the only means with respects to STI stress to improve the circuit performance is to adjust the *STIW* of the cell. Because such improvement could only influence the MOSFET on the edge of the cell, the degree of the improvement is limited. During the design of RF/analog circuits, however, the layout of each MOSFET can be arbitrary, and so many methods such as changing the *SA/SB* and *STIW* could be used to optimize the circuit performance.

As we know, the driving current of PMOS increases and that of NMOS decreases due to STI stress. Consequently, in most cases, we can increase the *STIW* and decrease the *SA/SB* of PMOS to enhance the positive effect of STI stress on PMOS while decrease the *STIW* and increase the *SA/SB* of NMOS to decrease the negative effect of STI stress on

NMOS. Furthermore, when there exists blank space in the layout, the dummy active region, which has no function but changing the STI stress environment of MOSFET, could be filled if necessary to improve the circuit performance. In most cases, if the surrounding of the blank region are mainly NMOS, the dummy active region could be filled in the vacant space to suppress the impact of the STI stress. Conversely, if the surrounding of the blank region are mainly PMOS, then there is no need to fill the blank space with the dummy active region.

B. The Choice of Number of Fingers

In analog circuits, MOSFETs are usually designed with mutiple fingers. The number of fingers has impact on the value of STI stress. In this paper, the STI stress of a MOSFET is studied when the number of fingers varies from 1 to 16. All fingers in this device are the same in shape with L=90nm. The spacing among fingers, as well as the distance betweem the egde finger and the boundary of STI are all 0.2um. The equavalent STI stress of the MOSFET verus the number of fingers is shown in Fig.5. We can see from Fig.5 that with the increase of the number of fingers, more fingers are far away from the STI, then the value of the STI stress on the MOSFET will decrease. Meanwhile, we exhibit the normalized driving current which is obtained by using our model with regard to STI stress in Fig.5. So from Fig.5 we can see the relationship of MOSFET characteristics with the number of fingers.

As we know, the performance of PMOS is enhanced by STI stress, thus the number of fingers should be set as small as possible to enlarge STI stress effects. Conversely, because the performance of NMOS is degraded by STI stress, the number of fingers should be set as large as possible to diminish STI stress effects.

We investigate the effect of STI stress on a ring oscillator designed in 90nm technology by varying the number of fingers of the device. The initial number of the figures of the device is 5. When we increase the finger number of NMOS to 10, and decrease the finger number of PMOS to 2, Fig.6 shows the different waveforms before and after adjustment. The corresponding frequencies are exhibited in Table 1. It can be seen that the oscillation frequency increases by 8%.

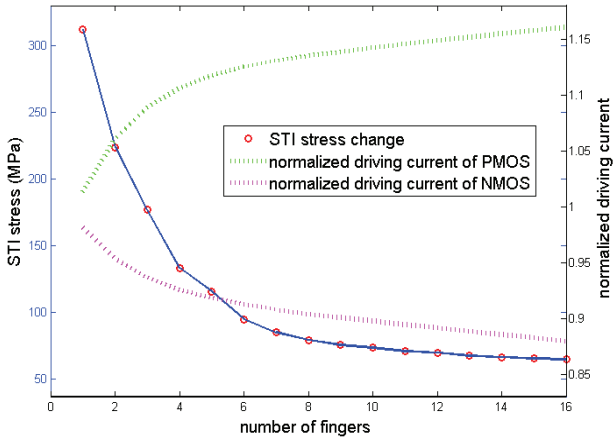

Fig.5. The dependence of STI stress and normalized driving current on the number of fingers

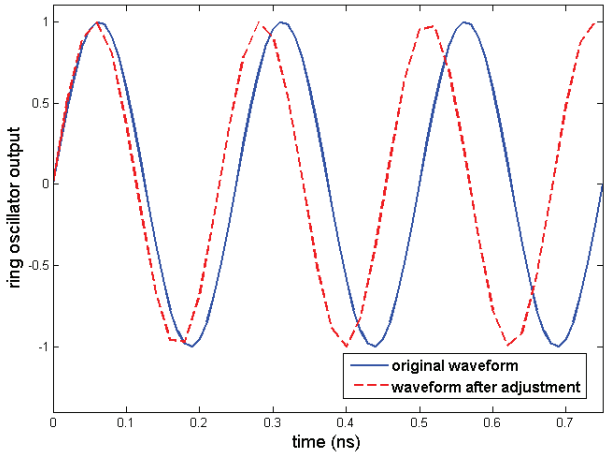

Fig.6. The waveform change of ring oscillator based on the adjustment of the number of fingers under the effects of STI stress

Generally, the number of fingers of MOSFET should be as large as possible to reduce the area cost and to decrease the gate resistance. However, this conclusion is no longer reasonable when the influence of STI stress is considered, especially in the circuits which consist mainly of PMOS transistors. Under this circusmastance, the number of fingers of the MOSFET should be as small as possible to improve the circuit performance. Consequently, there is a trade off when choosing the number of fingers.

Table 1 The frequency before and after adjustment

	original	after adjustment
oscillation frequency	4GHz	4.33GHz

C. The Effect of Mismatch

Since the influence of STI stress on PMOS and NMOS is in opposite directions, the two effects may be neutralized to some degree in certain circuits. For example, the delay of the PMOS increases and that of the NMOS decreases under the effects of STI stress, therefore the total delay appears only a little variation. However, the result is different in other cases. For example, in bias circuits, due to the effects of STI stress, the current in PMOS is higher than the reference current, while the current in NMOS is lower. Then the mismatch between the current of PMOS and that of NMOS is the sum of their difference from the reference current, which is an unexpected phenomenon. Under such situation, the importance of symmetric design, which can suppress the current deviation due to STI stress, grows significant. Nevertheless, it is very difficult to realize the exactly symmetrical design in reality, especially when considering the effects of STI stress. By using our method, we could obtain the exact influence of the asymmetrical design due to STI stress, and then decide whether it is necessary to redesign the layout or not.

VI. Experimental Results

In this paper we employ the commercial technology to verify our models and realistic circuits to discuss the

change of the circuit performance and optimization when considering STI stress.

First we use the measured data obtained from 65nm CMOS technology to verify the developed model based on STI stress simulation. And then the analysis results and optimization strategies presented in previous section are applied in the performance analysis of several RF/analog circuits designed in 90nm CMOS technology.

A. Verification of Model based on STI stress simulation

We have fabricated MOSFETs in commercial 65nm CMOS low-leakage standard technology on the wafer with (100) orientation. The leakage current is measured at $V_g=V_d=V_{DD}$ and $V_s=V_b=GND$. The V_{DD} used is 1.2V.

The process parameters for 65nm technology in our stress simulation tool are as follows:

1. Depth of STI: 0.32μm
2. Thickness of liner-oxide: 100Å
3. Thickness of silicon substrate: 600~800μm
4. Density of silicon dioxide inside STI: 2.32g/cm^3
5. Steepness of STI: 85~87 degree

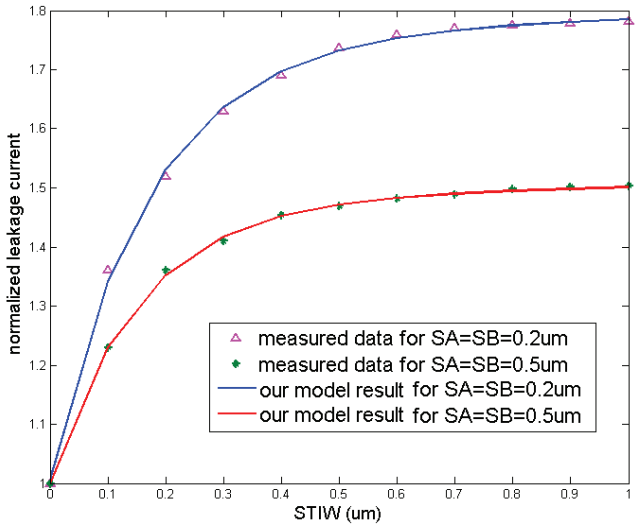

Fig.7. Comparison of our leakage model with our measured data

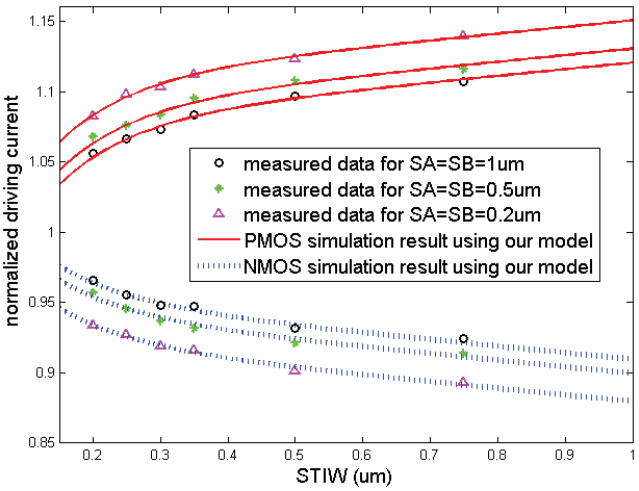

Fig.8. Comparison of our mobility model with measured data [9]

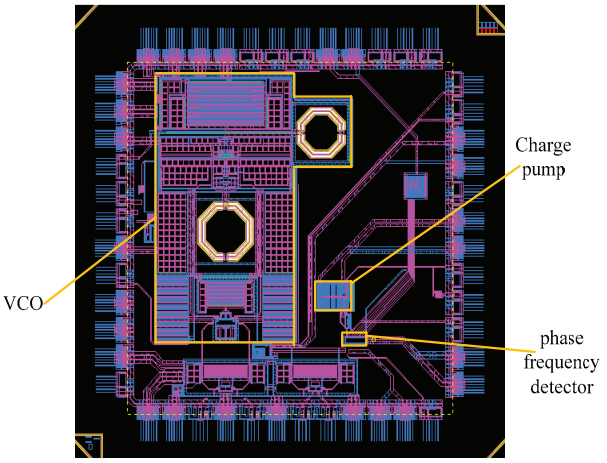

Fig.9. The layout of PLL in 90nm technology

Fig.7 shows the normalized leakage current with respect to *STIW* whose change leads to the difference of STI stress, and it also exhibits the comparison of our model prediction with the measured data. It can be seen from Fig.7 that the leakage model, which is a reflection of our mobility model and threshold voltage model, are able to describe the MOSFET characteristics accurately.

We modify the BISM4 model by using our mobility model to replace its original one and obtain the driving current of MOSFETs due to the effects of the STI stress. The simulation results obtained using the modified model are compared with the measured data in 65nm technology [9] (Fig. 8). It can be seen from Fig.8 that our model based on STI stress simulation is in good agreement with the actual data.

B. RF/Analog Circuit performance Analysis

In this part, the performance of several RF/analog circuits considering STI stress is discussed. We use a realistic PLL designed in 90nm CMOS technology [25] to conduct the experiment. Its operating frequency is 4GHZ and the transient settling time is 68μs. The layout of the PLL is shown in Fig.9. Our discussion is focused on the impact of the STI stress on three crucial components of the PLL, that is, charge pump, phase frequency detector and VCO.

In the charge pump design, the mirror current circuits should be designed with the symmetric structure, which is hardly completely met in the actual layout design, so the effect of STI stress on the pull-up current and pull-down current could not be avoided. The result is that because of STI stress, the pull-up current will increase and the pull-down current will decrease, making the circuit performance deteriorate.

The degree of the mismatch between pull-up current and the pull-down current using our model based on STI stress calculation is shown in Fig.10. It can be seen from Fig.10 that the pull-up current and the pull-down current are mismatched to certain extent($\approx$12%) when considering complex STI stress distribution. Therefore, STI stress must be paid much attention to in the layout design of charge pump. The layout of the mirror current circuits should be

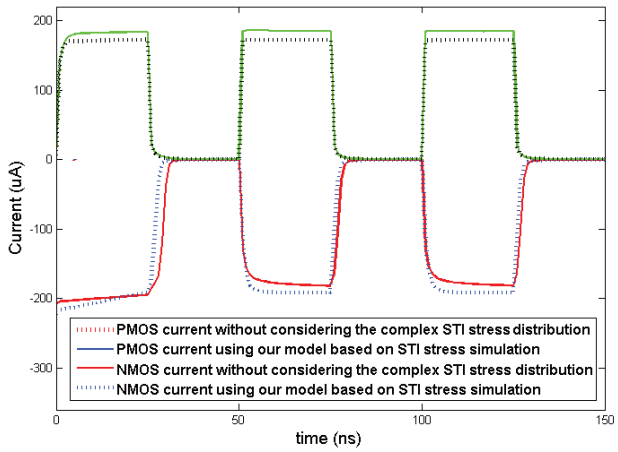

Fig.10. Comparison of the result of pull-up and pull-down current of charge pump with and without considering the complex STI stress distribution

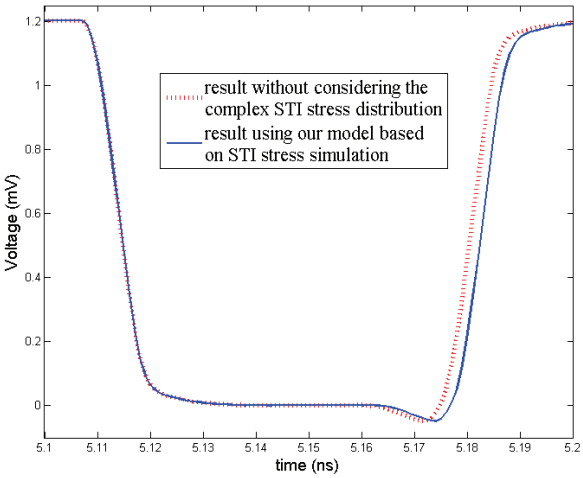

Fig.11. Comparison of the reset delay of phase frequency detector with and without considering the complex STI stress distribution

designed very carefully to guarantee their symmetrical structure. Some layout optimization methods such as using as many fingers as possible in devices could be adopted when considering the impact of STI stress.

Fortunately, the effects of STI stress are not so severe in all situations. Next, by using the proposed simulator and models, the change of the delay of another important circuit, phase frequency detector, is analyzed with considering the effects of the STI stress. The reset delay with and without considering the complex STI stress distribution is given in Fig.11. It can be seen from Fig.11 that the influence of the STI stress is not very obvious. Because the delay caused by PMOS decreases and the delay caused by NMOS increases due to STI stress, which means that the two effects are neutralized to some extent, the change of circuit delay is not very significant (≈3%). The tiny change comes from the fact that the impact of the STI stress on PMOS is more evident than that on NMOS. Consequently, in actual layout design, the finger number of NMOS should be made smaller and that of PMOS should be made larger to reduce the difference between the delay obtained before and after considering the complex STI stress distribution on a die.

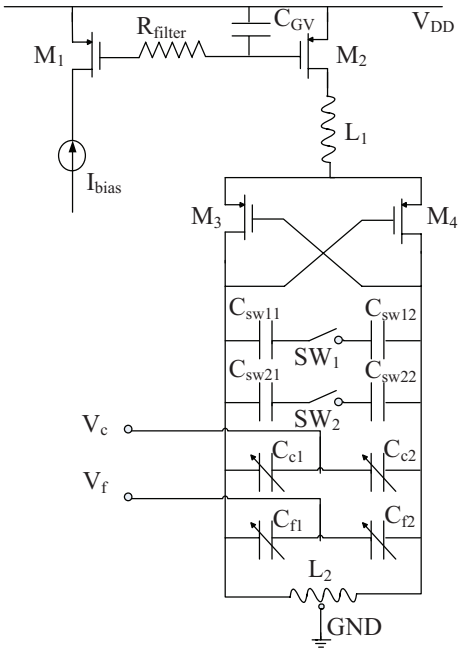

Fig.12. the schematic of the LC VCO

Fig.12 shows the schematic of the single-input dual-path LC VCO design in 90nm technology [25]. Its tuning frequency is 3.44 - 4.10GHz. Since this is a PMOS LC VCO, the presence of STI stress improves the circuit performance, namely reduces the phase noise of the circuit, which is one of the most important performance indicators of VCO. To accomplish this, the finger number of PMOS in this circuit should be made as small as possible under the permission of the area cost for the improvement of circuit performance. Table 2 gives the variation of phase noise of the circuit with the change of the finger number of PMOS to verify our theoretical analysis. Here we test the phase noise at three points which deviate from the center frequency by 10kHz, 100kHz and 1MHz respectively. It can be seen from Table 2 that with the decrease of the finger number, the performance of phase noise is indeed improved.

It can be derived from our experimental results that with the presence of STI stress, special care must be taken to determine the number of fingers of MOSFETs in certain analog circuits. The traditional way of using large number of fingers in devices is no longer absolutely reasonable, especially for PMOS transistors. Sometimes, the number of fingers of the MOSFETs should be set as small as possible to enhance the impact of STI stress.

Table 2 The phase noise with respect to the number of fingers at different frequency offsets

Finger number	Phase Noise (dBc/Hz) @10kHz	@ 100kHz	@1MHz
16	-60.7	-93.2	-126.2
8	-64.5	-94.8	-126.6
4	-69.8	-96.9	-126.9
2	-73.1	-98.2	-127.1
1	-75.4	-99.5	-127.3

VII. Conclusions

In this paper, a complete flow for analyzing circuit performance under the impact of STI stress is proposed. This flow is composed of three key components, an efficient stress simulator, a comprehensive MOS model considering STI stress, and a standard circuit simulator. Taking the layout information, the stress simulator can provide an accurate stress profile for a circuit. Then with the compact model we can obtain the MOSFET characteristics with considering STI stress. Together with the modified standard circuit simulator, the actual circuit performance can be determined. Optimization methods for the performance of RF/analog circuits considering STI stress are also presented. Case studies are done with commercial technology, which show the validity and effectiveness of our model and our optimizations.

Acknowledgement

This work is funded by National Program on Key Basic Research Project (973 Program) of China (2006CB302700). The collaboration with Cadence Design Systems is greatly appreciated.

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