

Editorial

CAD for Gigascale SoC Design and Verification Solutions

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As VLSI technology enters the nanometer regime, the design complexity is rapidly increasing with timing, power, routability, and reliability. Salient design automation techniques for scalable SoC design and verification solutions that could greatly improve the design quality are highly desired. This special issue is dedicated to the research problems in all aspects of System-on-Chip (SoC) implementation and verification. The papers selected for this special issue address new optimization, simulation, and verification techniques containing theoretical and/or applied contributions that emphasize the scalability to future large designs. They represent a good panel on the state-of-the-art development in scalable VLSI design and verification algorithms and methodologies.

This special issue contains ten papers. Six papers focus on the physical design optimizations including routing, buffer insertion, gate sizing, partitioning, floorplanning, and leakage analysis. Other three papers address the low-power test and resource sharing issue from different perspectives. Another paper discusses the emerging security issue in SoC design and presents some interesting new challenges.

In the paper entitled “*Efficient congestion mitigation using congestion-aware steiner trees and network coding topologies*,” the authors present a new Steiner tree construction technique for reducing congestion and minimizing overflow. With the integration of network coding, their technique can achieve significant improvements in routability.

In the paper entitled “*Shedding physical synthesis area bloat*,” the authors present a novel physical synthesis flow addressing the area bloat issue. To mitigate the significant area increase due to buffer insertion and gate sizing, a set of practical physical synthesis tools are designed which perform much better than existing algorithms in industrial designs.

In the paper entitled “*Buffer planning for IP placement using sliced-LFE*,” the authors present a buffer planning technique during floorplanning. Given a fixed-outline constraint, buffer insertion can be performed using a sliced less flexibility first algorithm which allows to distinguish geometric difference between floorplan candidates with the same topological structure. The proposed two-stage technique can significantly improve the success rate of buffer insertion and run faster than existing algorithms.

In the paper entitled “*Finding the energy efficient curve: gate sizing for minimum power under delay constraints*,” the authors present a gate sizing technique which targets to satisfy the timing constraint with minimal dynamic and leakage power consumption. Based on a new metric called energy delay gain to quantify the timing and power tradeoff, geometric programming technique is applied to optimize the circuits in the approach.

In the paper entitled “*The impact of statistical leakage models on design yield estimation*,” the authors review a set of closed form approximations on leakage power and present the study on the impact of different sums of lognormal approximation to the leakage of multiple leaky devices. Through comparing with CDF matching technique, they show that modeling the tail probability in CDF matching is critical.

In the paper entitled “*Wirelength minimization in partitioning and floorplanning using evolutionary algorithms*,” the authors present a memetic algorithm for partitioning and floorplanning. The algorithm uses multiple local search phases to reduce delay in partitioning and area in floorplanning.

In the paper entitled “*Weighted transition based reordering, columnwise bit filling, and difference vector: a power*

aware test data compression method,” the authors improve the existing hamming distance-based reordering technique for test data compression. The new technique can achieve high compression rate while reducing test power with little on-chip area overhead.

In the paper entitled “*Suitability of various low-power testing techniques for IP core-based SoC: a survey*,” the authors present a survey in the area of low-power testing for IP core-based SoC. Various existing techniques including external testing, BIST techniques, and DFT techniques are reviewed.

In the paper entitled “*Efficient resource sharing architecture for multistandard communication system*,” the authors present a dedicated hardware module which can be reconfigured for the OFDM wireless LAN standard and MCDMA standard. The new hardware can efficiently share resources for the two standards.

In the paper entitled “*SoC: a real platform for IP reuse, IP infringement, and IP protection*,” the authors address the security issue due to the IP reuse in SoC. They discuss how to locate attacks, categorize the infringement, apply strategic analysis in IP-based SoC design flow, and highlight several new research opportunities in this emerging area.

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