2024 Digital IC Design
Homework 3: matrix multiplier

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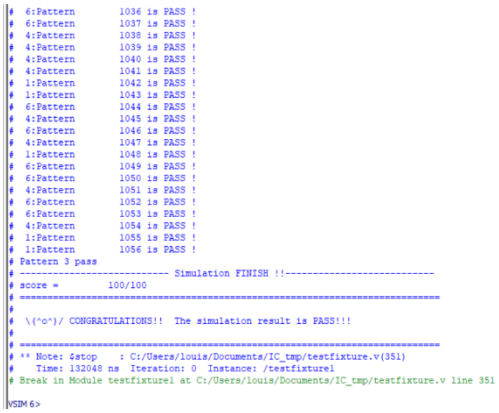
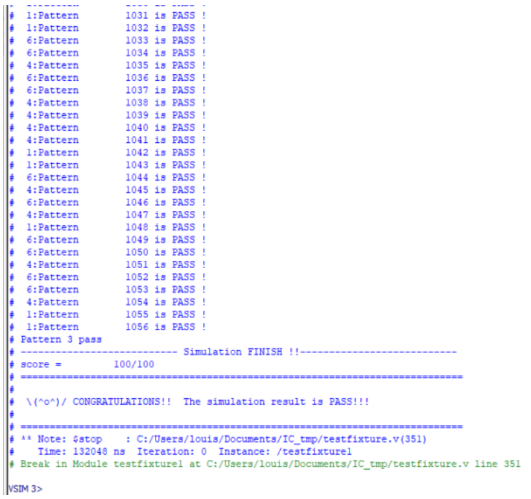
Simulation Result

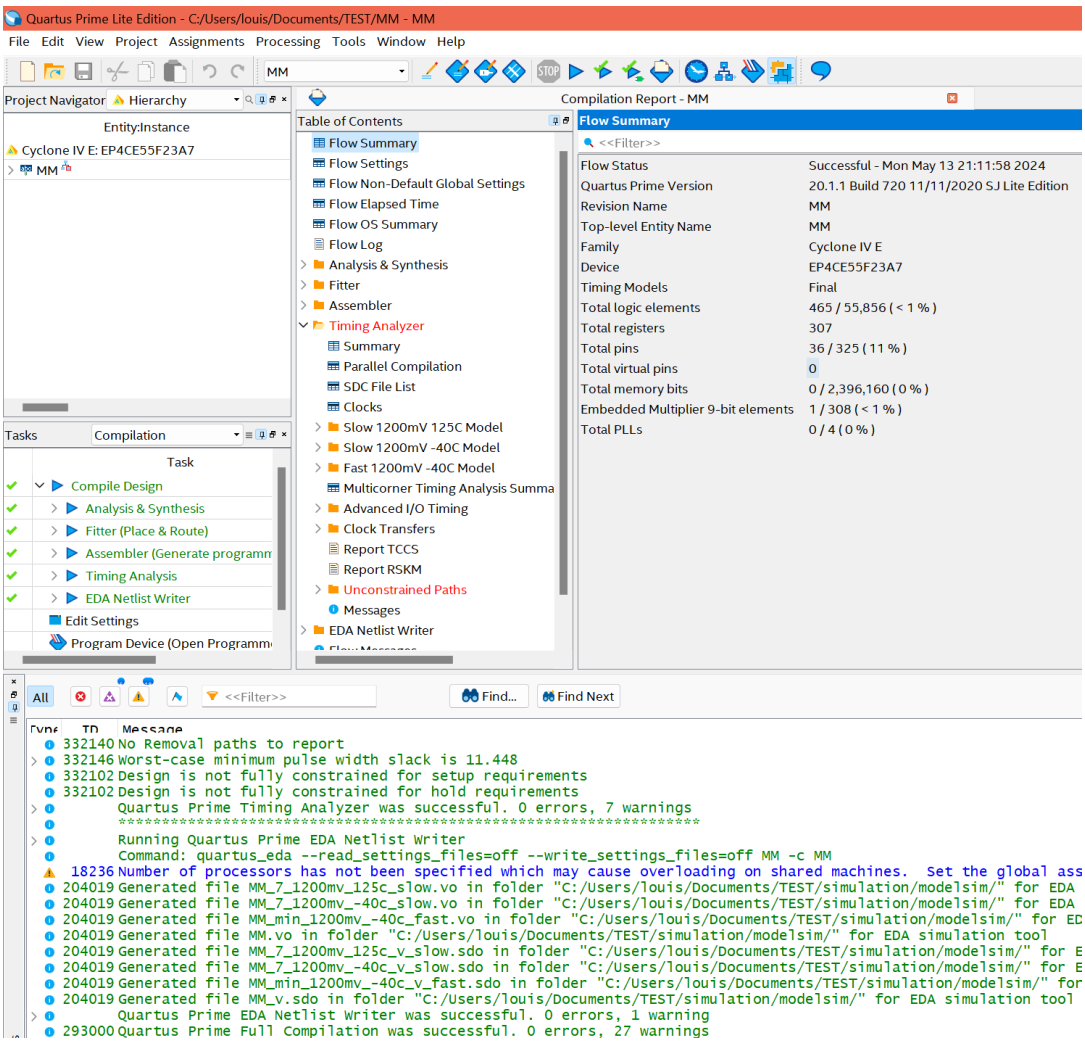
Functional simulation	Score 100	Gate-level simulation	Score 100	Clock width	(ns) 24	Gate-level simulation time	simulation time (ns) 132048





Synthesis Result

Total logic elements	465
Total memory bit	0
Embedded multiplier 9-bit element	1



Description of your design

將 fsm 分成 6 個 state，分別代表 load matrix1, load matrix2, 乘法步驟, 乘法換下一行, 非法, 完成。

乘法步驟是採用一個 clock 乘一格，而不是直接一列一行乘出結果。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (Total cycle used*clock width)*