

2024 Digital IC Design
Homework 3: matrix multiplier

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Simulation Result							
Functional simulation	Score 100	Gate-level simulation	Score 100	Clock width	(ns) 24	Gate-level simulation time	simulation time (ns) 132048
<pre># 6:Pattern 1036 is PASS ! # 6:Pattern 1037 is PASS ! # 6:Pattern 1038 is PASS ! # 4:Pattern 1039 is PASS ! # 4:Pattern 1040 is PASS ! # 4:Pattern 1041 is PASS ! # 1:Pattern 1042 is PASS ! # 1:Pattern 1043 is PASS ! # 6:Pattern 1044 is PASS ! # 4:Pattern 1045 is PASS ! # 6:Pattern 1046 is PASS ! # 4:Pattern 1047 is PASS ! # 1:Pattern 1048 is PASS ! # 6:Pattern 1049 is PASS ! # 6:Pattern 1050 is PASS ! # 4:Pattern 1051 is PASS ! # 6:Pattern 1052 is PASS ! # 6:Pattern 1053 is PASS ! # 4:Pattern 1054 is PASS ! # 1:Pattern 1055 is PASS ! # 1:Pattern 1056 is PASS ! # Pattern 3 pass # ----- Simulation FINISH !----- # score = 100/100 # # \("o")/ CONGRATULATIONS!! The simulation result is PASS!!! # # ----- # ** Note: \$stop : C:/Users/louis/Documents/IC_tmp/testfixture.v(351) # Time: 132048 ns Iteration: 0 Instance: /testfixture1 # Break in Module testfixture1 at C:/Users/louis/Documents/IC_tmp/testfixture.v line 351 VSM6></pre>				<pre># 1:Pattern 1031 is PASS ! # 1:Pattern 1032 is PASS ! # 6:Pattern 1033 is PASS ! # 6:Pattern 1034 is PASS ! # 4:Pattern 1035 is PASS ! # 6:Pattern 1036 is PASS ! # 6:Pattern 1037 is PASS ! # 4:Pattern 1038 is PASS ! # 4:Pattern 1039 is PASS ! # 4:Pattern 1040 is PASS ! # 4:Pattern 1041 is PASS ! # 1:Pattern 1042 is PASS ! # 1:Pattern 1043 is PASS ! # 6:Pattern 1044 is PASS ! # 4:Pattern 1045 is PASS ! # 6:Pattern 1046 is PASS ! # 4:Pattern 1047 is PASS ! # 1:Pattern 1048 is PASS ! # 6:Pattern 1049 is PASS ! # 6:Pattern 1050 is PASS ! # 4:Pattern 1051 is PASS ! # 6:Pattern 1052 is PASS ! # 6:Pattern 1053 is PASS ! # 4:Pattern 1054 is PASS ! # 1:Pattern 1055 is PASS ! # 1:Pattern 1056 is PASS ! # Pattern 3 pass # ----- Simulation FINISH !----- # score = 100/100 # # \("o")/ CONGRATULATIONS!! The simulation result is PASS!!! # # ----- # ** Note: \$stop : C:/Users/louis/Documents/IC_tmp/testfixture.v(351) # Time: 132048 ns Iteration: 0 Instance: /testfixture1 # Break in Module testfixture1 at C:/Users/louis/Documents/IC_tmp/testfixture.v line 351 VSM3></pre>			
Synthesis Result							
Total logic elements				465			
Total memory bit				0			
Embedded multiplier 9-bit element				1			

Quartus Prime Lite Edition - C:/Users/louis/Documents/TEST/MM - MM

File Edit View Project Assignments Processing Tools Window Help

Project Navigator: Entity: Instance
Cyclone IV E: EP4CE55F23A7
MM

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Flow Summary

Flow Status: Successful - Mon May 13 21:11:58 2024

Quartus Prime Version: 20.1.1 Build 720 11/11/2020 SJ Lite Edition

Revision Name: MM

Top-level Entity Name: MM

Family: Cyclone IV E

Device: EP4CE55F23A7

Timing Models: Final

Total logic elements: 465 / 55,856 (< 1 %)

Total registers: 307

Total pins: 36 / 325 (11 %)

Total virtual pins: 0

Total memory bits: 0 / 2,396,160 (0 %)

Embedded Multiplier 9-bit elements: 1 / 308 (< 1 %)

Total PLLs: 0 / 4 (0 %)

Tasks: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Timing Analysis
- EDA Netlist Writer
- Edit Settings
- Program Device (Open Programm...)

Messages

```

332140 No Removal paths to report
332146 Worst-case minimum pulse width slack is 11.448
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 7 warnings
*****
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off MM -c MM
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global ass
204019 Generated file MM_7_1200mv_125c_slow.vo in folder "C:/Users/louis/Documents/TEST/simulation/modelsim/" for EDA
204019 Generated file MM_7_1200mv_-40c_slow.vo in folder "C:/Users/louis/Documents/TEST/simulation/modelsim/" for EDA
204019 Generated file MM_min_1200mv_-40c_fast.vo in folder "C:/Users/louis/Documents/TEST/simulation/modelsim/" for ED
204019 Generated file MM.vo in folder "C:/Users/louis/Documents/TEST/simulation/modelsim/" for EDA simulation tool
204019 Generated file MM_7_1200mv_125c_v_slow.sdo in folder "C:/Users/louis/Documents/TEST/simulation/modelsim/" for E
204019 Generated file MM_7_1200mv_-40c_v_slow.sdo in folder "C:/Users/louis/Documents/TEST/simulation/modelsim/" for E
204019 Generated file MM_min_1200mv_-40c_v_fast.sdo in folder "C:/Users/louis/Documents/TEST/simulation/modelsim/" for
204019 Generated file MM_v.sdo in folder "C:/Users/louis/Documents/TEST/simulation/modelsim/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 27 warnings
  
```

Description of your design

將 fsm 分成 6 個 state，分別代表 load matrix1, load matrix2, 乘法步驟, 乘法換下一行, 非法, 完成。

乘法步驟是採用一個 clock 乘一格，而不是直接一列一行乘出結果。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (Total cycle used*clock width)*