2024 Digital IC Design

Homework 3: matrix multiplier

1. Introduction

Matrix multiplication is a fundamental operation in various fields such as mathematics, computer science, engineering, and physics. It involves the computation of the product of two matrices, resulting in a new matrix that captures the combined effect of the original matrices. This operation finds wide applications in areas such as linear algebra, signal processing, image processing, and machine learning. In this project, we aim to design and implement a matrix multiplier (MM). The specification and function of the circuit is detailed in the following sections.

2. Design Specifications

2.1 Block Overview

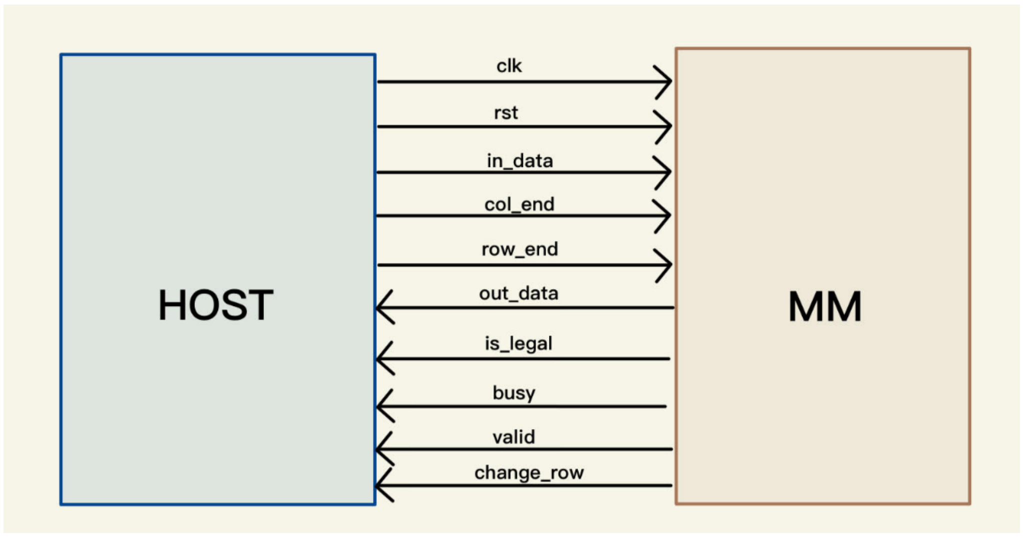


Fig.1. System Block Diagram

2.2 I/O Interface

Table I. I/O interface of the design

Signal Name	I/O	width	Description
clk	I	1	This circuit is a synchronous design triggered at the positive edge of *clk*.
rst	I	1	Active-high asynchronous reset signal.
in_data	I	8	Input 8 bit signed matrix data one by one.

col_end	I	1	This signal is 1 when the input matrix completes the data input of a row, otherwise it is 0.
row_end	I	1	This signal is 1 when an input matrix complete data input, otherwise it is 0.
valid	O	1	When this signal is 1, tb will check out_data, is_legal and change_row signals.
out_data	O	20	Output the 20-bit matrix operation result, one element at a time.
is_legal	O	1	Output whether the two matrices can be multiplied, 1 means they can be multiplied.
change_row	O	1	This signal is 1, When the output matrix completes the output of one row
busy	O	1	This signal is 1 means the system is busy and tb will stop in_data transmission.

2.3 System Description

1. After the system is reset, when tb detects that busy is 0, the matrix data is input one by one from in_data.
2. The shape of the input matrices is controlled by row_end and col_end signal. The following is an example of inputting a 2 x 2 matrix and a 3 x 2 matrix:

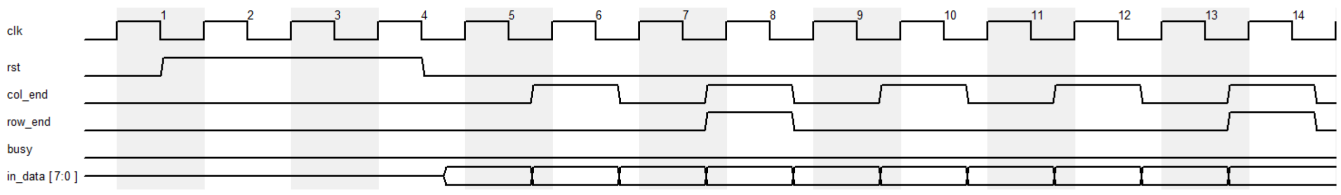


Fig.2. Input Timing Diagram

3. The shape of the output matrices is controlled by change_row signal. The following is an example of outputting a 2 x 2 matrix:

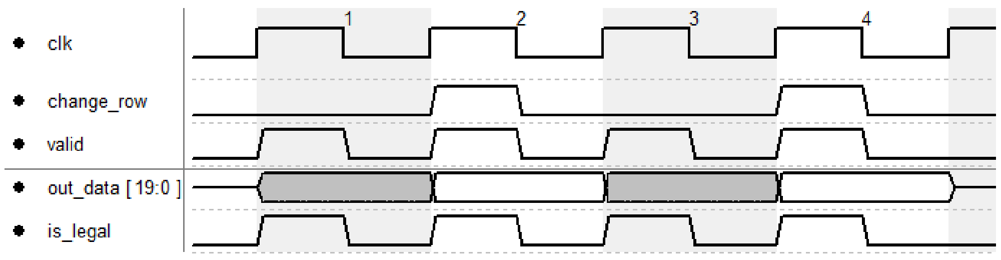


Fig.3. Output Timing Diagram

Notice:

1. When the second matrix is completely input and valid is 1, tb will check whether out_data, is_legal, change_row are correct.(Please keep valid 0 until the second matrix is completely input.)
2. If 4 pieces of data are to be output in this round, but only 3 are output, tb will continue to wait for the output of the fourth data and will not give the next matrix data.

3. File Description

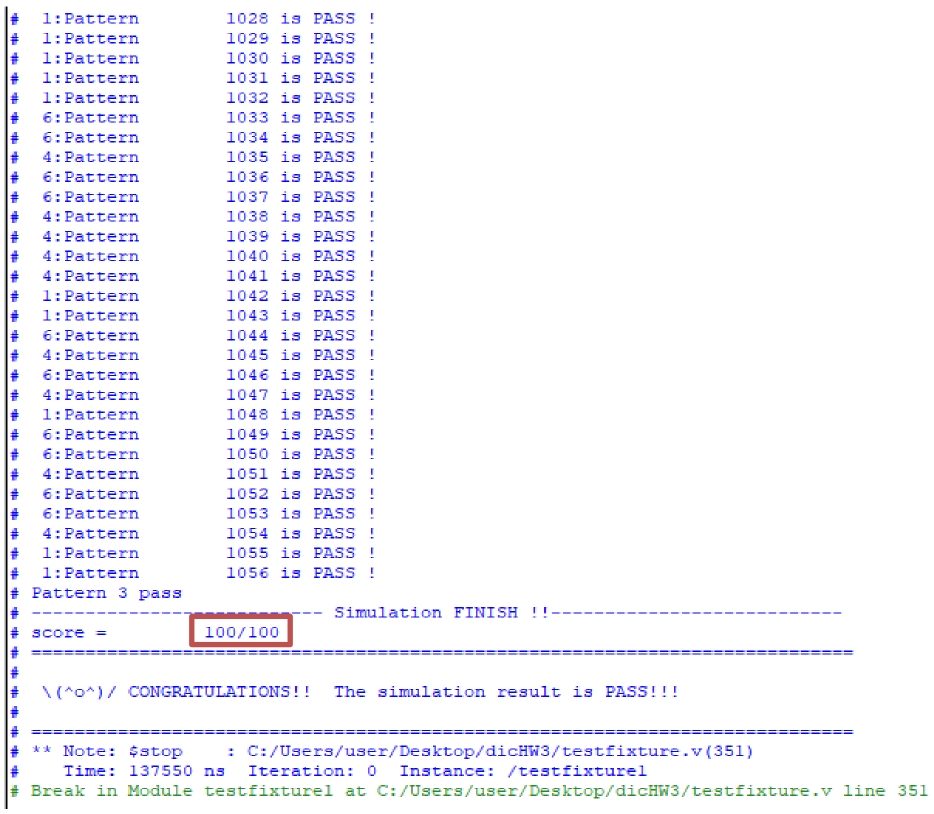
File Name	Description
MM.v	The top module of your design.
testfixture.v	The testbench file. In this homework, you are allowed to modify the defined *cycle* and *terminate_cycle* in testbench.
in1.dat in2.dat in3.dat	Input data
out1.dat out2.dat out3.dat	Golden data

mx_shape1.dat mx_shape2.dat mx_shape3.dat	Matrix shape data

4. Scoring

4.1 Functional simulation [60%]

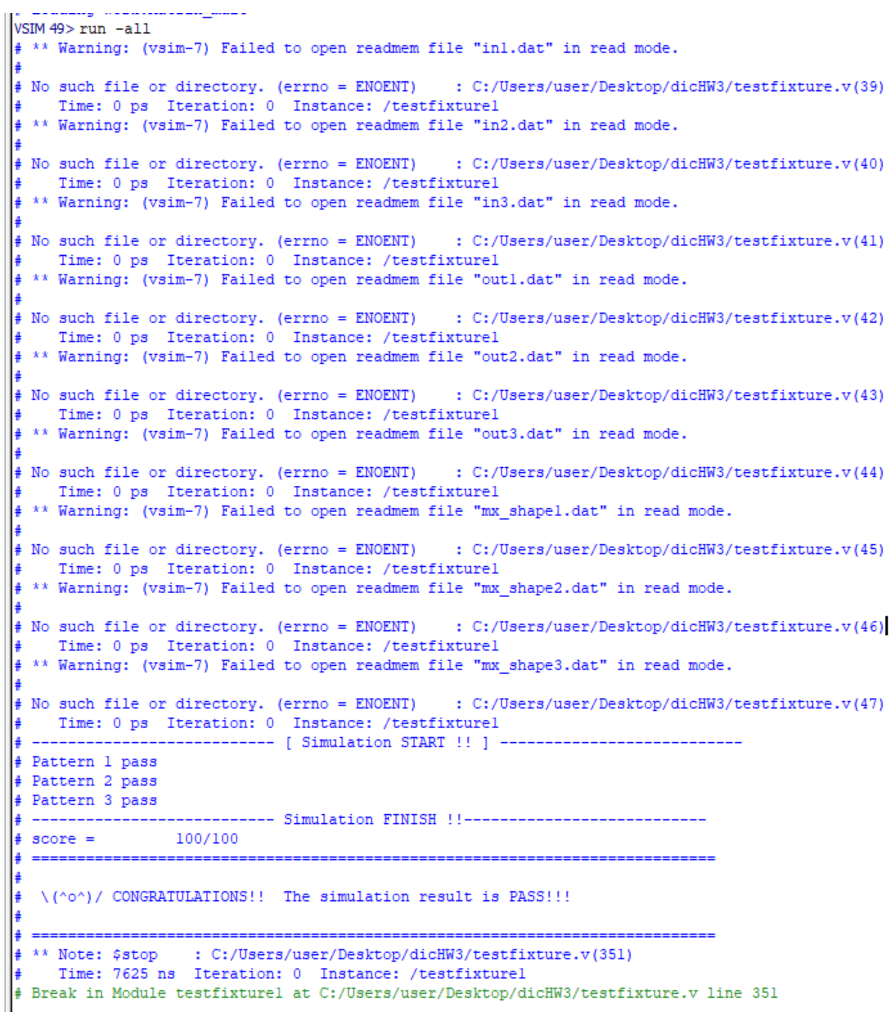
All of the results should be generated correctly, and you will get the following message in ModelSim simulation.(score = 0.6 * total_score)



```
#   1:Pattern        1028 is PASS !
#   1:Pattern        1029 is PASS !
#   1:Pattern        1030 is PASS !
#   1:Pattern        1031 is PASS !
#   1:Pattern        1032 is PASS !
#   6:Pattern        1033 is PASS !
#   6:Pattern        1034 is PASS !
#   4:Pattern        1035 is PASS !
#   6:Pattern        1036 is PASS !
#   6:Pattern        1037 is PASS !
#   4:Pattern        1038 is PASS !
#   4:Pattern        1039 is PASS !
#   4:Pattern        1040 is PASS !
#   4:Pattern        1041 is PASS !
#   1:Pattern        1042 is PASS !
#   1:Pattern        1043 is PASS !
#   6:Pattern        1044 is PASS !
#   4:Pattern        1045 is PASS !
#   6:Pattern        1046 is PASS !
#   4:Pattern        1047 is PASS !
#   1:Pattern        1048 is PASS !
#   6:Pattern        1049 is PASS !
#   6:Pattern        1050 is PASS !
#   4:Pattern        1051 is PASS !
#   6:Pattern        1052 is PASS !
#   6:Pattern        1053 is PASS !
#   4:Pattern        1054 is PASS !
#   1:Pattern        1055 is PASS !
#   1:Pattern        1056 is PASS !
#  Pattern 3 pass
#  --------------------------- Simulation FINISH !!---------------------------
#  score =          100/100
#  ============================================================================
#
#   \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!
#
#  ============================================================================
#  ** Note: $stop    : C:/Users/user/Desktop/dicHW3/testfixture.v(351)
#     Time: 137550 ns  Iteration: 0  Instance: /testfixture1
#  Break in Module testfixture1 at C:/Users/user/Desktop/dicHW3/testfixture.v line 351
```

Fig 4. Functional simulation result

Please make sure to read the .dat file. The following is the wrong simulation result.



```
VSIM 49> run -all
# ** Warning: (vsim-7) Failed to open readmem file "in1.dat" in read mode.
#
# No such file or directory. (errno = ENOENT)    : C:/Users/user/Desktop/dicHW3/testfixture.v(39)
#    Time: 0 ps  Iteration: 0  Instance: /testfixture1
# ** Warning: (vsim-7) Failed to open readmem file "in2.dat" in read mode.
#
# No such file or directory. (errno = ENOENT)    : C:/Users/user/Desktop/dicHW3/testfixture.v(40)
#    Time: 0 ps  Iteration: 0  Instance: /testfixture1
# ** Warning: (vsim-7) Failed to open readmem file "in3.dat" in read mode.
#
# No such file or directory. (errno = ENOENT)    : C:/Users/user/Desktop/dicHW3/testfixture.v(41)
#    Time: 0 ps  Iteration: 0  Instance: /testfixture1
# ** Warning: (vsim-7) Failed to open readmem file "out1.dat" in read mode.
#
# No such file or directory. (errno = ENOENT)    : C:/Users/user/Desktop/dicHW3/testfixture.v(42)
#    Time: 0 ps  Iteration: 0  Instance: /testfixture1
# ** Warning: (vsim-7) Failed to open readmem file "out2.dat" in read mode.
#
# No such file or directory. (errno = ENOENT)    : C:/Users/user/Desktop/dicHW3/testfixture.v(43)
#    Time: 0 ps  Iteration: 0  Instance: /testfixture1
# ** Warning: (vsim-7) Failed to open readmem file "out3.dat" in read mode.
#
# No such file or directory. (errno = ENOENT)    : C:/Users/user/Desktop/dicHW3/testfixture.v(44)
#    Time: 0 ps  Iteration: 0  Instance: /testfixture1
# ** Warning: (vsim-7) Failed to open readmem file "mx_shape1.dat" in read mode.
#
# No such file or directory. (errno = ENOENT)    : C:/Users/user/Desktop/dicHW3/testfixture.v(45)
#    Time: 0 ps  Iteration: 0  Instance: /testfixture1
# ** Warning: (vsim-7) Failed to open readmem file "mx_shape2.dat" in read mode.
#
# No such file or directory. (errno = ENOENT)    : C:/Users/user/Desktop/dicHW3/testfixture.v(46)
#    Time: 0 ps  Iteration: 0  Instance: /testfixture1
# ** Warning: (vsim-7) Failed to open readmem file "mx_shape3.dat" in read mode.
#
# No such file or directory. (errno = ENOENT)    : C:/Users/user/Desktop/dicHW3/testfixture.v(47)
#    Time: 0 ps  Iteration: 0  Instance: /testfixture1
# --------------------------- [ Simulation START !! ] ---------------------------
# Pattern 1 pass
# Pattern 2 pass
# Pattern 3 pass
# --------------------------- Simulation FINISH !!---------------------------
# score =          100/100
# ============================================================================
#
#  \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!
#
# ============================================================================
# ** Note: $stop    : C:/Users/user/Desktop/dicHW3/testfixture.v(351)
#    Time: 7625 ns  Iteration: 0  Instance: /testfixture1
# Break in Module testfixture1 at C:/Users/user/Desktop/dicHW3/testfixture.v line 351
```

Fig 5. Wrong simulation result

4.2 Gate-Level Simulation [20%]

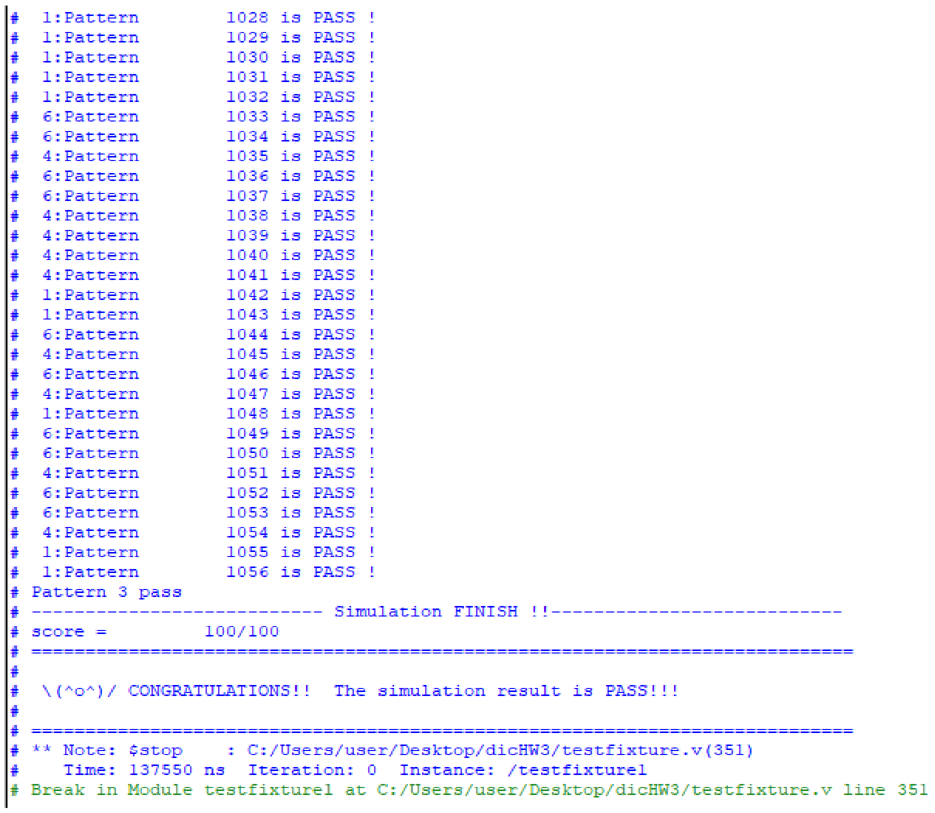
4.2.1 Synthesis

Your code should be synthesizable. After it is synthesized in Quartus, files named *MM.vo* and *MM_v.sdo* will be obtained.

DEVICE： Cyclone IV E - EP4CE55F23A7

4.2.2 Simulation

All of the results should be generated correctly using *MM.vo* and *MM_v.sdo*, and you will get the following message in ModelSim simulation.(score = 0.2 * total_score)

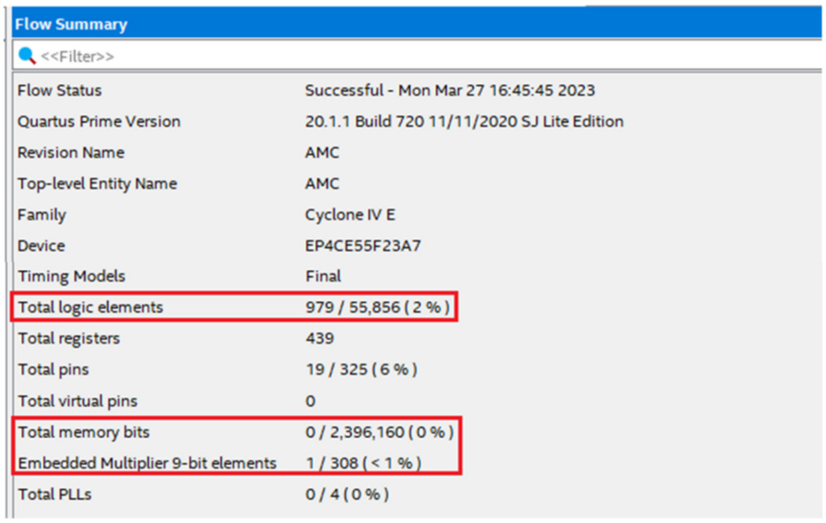


```
#  1:Pattern        1028 is PASS !
#  1:Pattern        1029 is PASS !
#  1:Pattern        1030 is PASS !
#  1:Pattern        1031 is PASS !
#  1:Pattern        1032 is PASS !
#  6:Pattern        1033 is PASS !
#  6:Pattern        1034 is PASS !
#  4:Pattern        1035 is PASS !
#  6:Pattern        1036 is PASS !
#  6:Pattern        1037 is PASS !
#  4:Pattern        1038 is PASS !
#  4:Pattern        1039 is PASS !
#  4:Pattern        1040 is PASS !
#  4:Pattern        1041 is PASS !
#  1:Pattern        1042 is PASS !
#  1:Pattern        1043 is PASS !
#  6:Pattern        1044 is PASS !
#  4:Pattern        1045 is PASS !
#  6:Pattern        1046 is PASS !
#  4:Pattern        1047 is PASS !
#  1:Pattern        1048 is PASS !
#  6:Pattern        1049 is PASS !
#  6:Pattern        1050 is PASS !
#  4:Pattern        1051 is PASS !
#  6:Pattern        1052 is PASS !
#  6:Pattern        1053 is PASS !
#  4:Pattern        1054 is PASS !
#  1:Pattern        1055 is PASS !
#  1:Pattern        1056 is PASS !
# Pattern 3 pass
# --------------------------- Simulation FINISH !!---------------------------
# score =         100/100
# ============================================================================
#
#  \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!
#
# ============================================================================
# ** Note: $stop    : C:/Users/user/Desktop/dicHW3/testfixture.v(351)
#    Time: 137550 ns  Iteration: 0  Instance: /testfixture1
# Break in Module testfixture1 at C:/Users/user/Desktop/dicHW3/testfixture.v line 351
```

Fig 6. Gate level simulation result

4.3 Performance [20%]

The performance is scored by the total logic elements, total memory bit, and embedded multiplier 9-bit element your design used in gate-level simulation and the simulation time your design takes.



Flow Summary

<<Filter>>

Flow Status	Successful - Mon Mar 27 16:45:45 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	AMC
Top-level Entity Name	AMC
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	979 / 55,856 (2 %)
Total registers	439
Total pins	19 / 325 (6 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	1 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

Fig 7. Synthesis result

The performance score will be decided by your ranking in all received homework. Only designs that passed gate-level simulation and meet resource limitations will be considered in the ranking. Otherwise, you can’t get performance score.

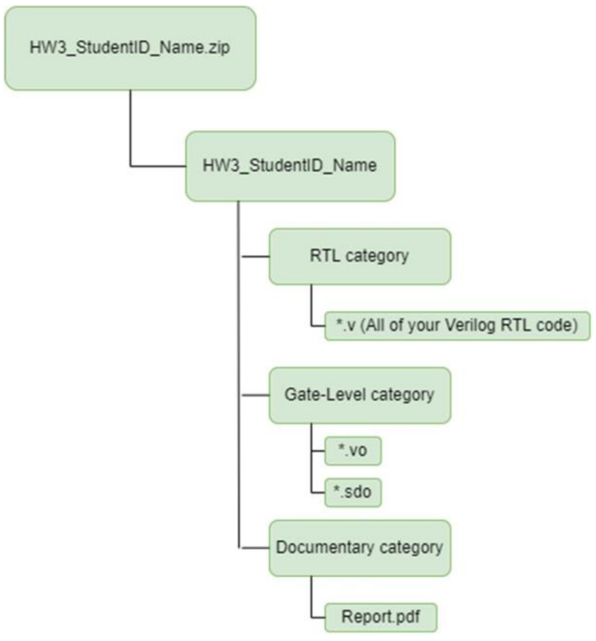
The scoring standard: (The smaller, the better)
Scoring = Area cost * Timing cost
Area cost = Total logic elements + total memory bits + 9*embedded multiplier 9-bit elements
Timing cost = Total cycle used*clock width

5. Submission

5.1 Submitted files

You should classify your files into three directories and compress them to .zip format. The naming rule is HW3_studentID_name.zip. If your file is not named according to the naming rule, you will lose five points.

	RTL category
*.v	All of your Verilog RTL code
	Gate-Level category
*.vo	Gate-Level netlist generated by Quartus
*.sdo	SDF timing information generated by Quartus
	Documentary category
*.pdf	The report file of your design (in pdf).

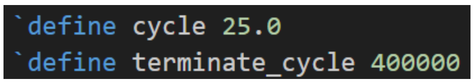


5.2 Report file

Please follow the spec of report. You are asked to describe how the circuit is designed as detailed as possible, and the flow summary result is necessary in the report. Please fill the field of total logic elements, total memory bits, embedded multiplier 9-bit elements according to the flow summary (as shown in Fig. 7) of your synthesized design. And fill the field of clock cycle used and clock width according to the gate-level simulation results that Modelsim shows. If the filled-in values don't match your synthesized design or gate-level simulation results, you will lose 10 points.

5.3 Note

In this homework, you are allowed to modify the defined *cycle* and *terminate_cycle* in testbench file. 'cycle' decides the clock width that is used to validate your design, and 'terminate_cycle' decides the maximum cycles your circuit takes to complete the simulation. Please do not modify any other content of the testbench.



```
`define cycle 25.0
`define terminate_cycle 400000
```

Please submit your .zip file to folder HW3 in moodle.
Deadline: 2024/05/13 23:55

Please don't design specifically for the test pattern. Otherwise, you will get 0 point. Any plagiarism behavior will also get 0 points.

If you have any problem, please contact TA by email
p76124011@gs.ncku.edu.tw