

## 2024 Digital IC Design Homework 5

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Score = area*timing (ps)	52,437,316000 = 45361*1156000(ps)
Cycle time (ns)	10

## Simulation Result

Functional simulation	Completed	Gate-level simulation	Completed
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```

# WARNING: No extended dataflow license exists
V$IM 17> run -all
# -----
# -- Simulation Start --
# -----
# Correct:      100
#
#          /|_/_|
#          / O,O |
# ##### Pass! #####
#          / ^ ^ ^ \
#          / ^ ^ ^ \ |w|
#          \m_m_|
#
# ** Note: $finish      : C:/Users/louis/Documents/T2/tb.v(90)
#    Time: 1156 ns  Iteration: 0  Instance: /tb
# 1
# Break in Module tb at C:/Users/louis/Documents/T2/tb.v line 90

```

## Description of your design

用 `fullkeys_tmp` 和 `stateArr_tmp` 來暫存 `round` 資訊，以及 `keyExpansion`

Flow Summary	
Flow Status	Successful - Mon Jun 24 00:24:31 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	AES
Top-level Entity Name	AES
Family	Cyclone IV E
Device	EP4CE75F29C8
Timing Models	Final
Total logic elements	45,361 / 75,408 ( 60 % )
Total registers	2693
Total pins	387 / 427 ( 91 % )
Total virtual pins	0
Total memory bits	0 / 2,810,880 ( 0 % )
Embedded Multiplier 9-bit elements	0 / 400 ( 0 % )
Total PLLs	0 / 4 ( 0 % )

The scoring standard: (The smaller, the better)

*Scoring =*

*Area cost \* Timing cost*

*Area cost =*

*Total logic elements + total memory bits + 9\*embedded multiplier 9-bit elements*

*Timing cost =*

*Simulation time*

Flow Summary	
<<Filter>>	
Flow Status	Successful - Mon May 20 14:38:37 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	AES
Top-level Entity Name	AES
Family	Cyclone IV E
Device	EP4CE75F29C8
Timing Models	Final
Total logic elements	45,971
Total registers	2954
Total pins	387
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0

```
# Correct:      100
#
#####
###          Pass!          ###
#####
#
#
# ** Note: $finish      : C:/Users/diclab/Desktop/DIC2024/HW5_/tb.v(99)
#   Time: 991250 ps    Iteration: 0   Instance: /tb
```