2024 Digital IC Design
Homework 4: Max-Priority Queue

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Simulation Result

Functional simulation	Score 100	Gate-level simulation	Score 100	Clock width	25 (ns)	Gate-level simulation time	simulation time (ns) **1430(ns)** **2080(ns)** **2455(ns)** **3080(ns)**

```
VSIM 3> run -all
#  ****************************
#  **                        **
#  **  Congratulations !!    **
#  **                        **        |__||
#  **  Simulation PASS !!    **       / 0.0  |
#  **                        **     /_____   |
#  **  Your score =100       **    /^ ^ ^ \  |
#  **                        **   |^ ^ ^ ^ |w|
#  ****************************    \m___m__|_|
# ** Note: $finish    : testfixture.v(157)
#    Time: 1422500 ps  Iteration: 0  Instance: /test
# 1
# Break in Module test at testfixture.v line 157
```

```
#    Time: 0 ps  Iteration: 0  Instance: /test File:
VSIM 21> run -all
#  ****************************
#  **                        **
#  **  Congratulations !!    **
#  **                        **        |__||
#  **  Simulation PASS !!    **       / 0.0  |
#  **                        **     /_____   |
#  **  Your score =100       **    /^ ^ ^ \  |
#  **                        **   |^ ^ ^ ^ |w|
#  ****************************    \m___m__|_|
# ** Note: $finish    : testfixture.v(157)
#    Time: 1430663 ps  Iteration: 0  Instance: /test
# 1
# Break in Module test at testfixture.v line 157
```

```
VSIM 11> run -all
#  ****************************
#  **                        **
#  **  Congratulations !!    **
#  **                        **        |__||
#  **  Simulation PASS !!    **       / 0.0  |
#  **                        **     /_____   |
#  **  Your score =100       **    /^ ^ ^ \  |
#  **                        **   |^ ^ ^ ^ |w|
#  ****************************    \m___m__|_|
# ** Note: $finish    : testfixture.v(157)
#    Time: 2072500 ps  Iteration: 0  Instance: /test
# 1
# Break in Module test at testfixture.v line 157
```

```
VSIM 25> run -all
#  ****************************
#  **                        **
#  **  Congratulations !!    **
#  **                        **        |__||
#  **  Simulation PASS !!    **       / 0.0  |
#  **                        **     /_____   |
#  **  Your score =100       **    /^ ^ ^ \  |
#  **                        **   |^ ^ ^ ^ |w|
#  ****************************    \m___m__|_|
# ** Note: $finish    : testfixture.v(157)
#    Time: 2080663 ps  Iteration: 0  Instance: /test
# 1
# Break in Module test at testfixture.v line 157
```

```
VSIM 15> run -all
#  ****************************
#  **                        **
#  **  Congratulations !!    **
#  **                        **        |__||
#  **  Simulation PASS !!    **       / 0.0  |
#  **                        **     /_____   |
#  **  Your score =100       **    /^ ^ ^ \  |
#  **                        **   |^ ^ ^ ^ |w|
#  ****************************    \m___m__|_|
# ** Note: $finish    : testfixture.v(157)
#    Time: 2447500 ps  Iteration: 0  Instance: /test
# 1
# Break in Module test at testfixture.v line 157
```

```
VSIM 29> run -all
#  ****************************
#  **                        **
#  **  Congratulations !!    **
#  **                        **        |__||
#  **  Simulation PASS !!    **       / 0.0  |
#  **                        **     /_____   |
#  **  Your score =100       **    /^ ^ ^ \  |
#  **                        **   |^ ^ ^ ^ |w|
#  ****************************    \m___m__|_|
# ** Note: $finish    : testfixture.v(157)
#    Time: 2455663 ps  Iteration: 0  Instance: /test
# 1
# Break in Module test at testfixture.v line 157
```

<table>
<tr>
<td>

```
VSIM 19> run -all
#  ****************************
#  **                          **
#  **  Congratulations !!      **
#  **                          **        |__||
#  **  Simulation PASS !!      **       / 0.0  |
#  **                          **     /_____   |
#  **  Your score =100         **    /^ ^ ^ \  |
#  **                          **   |^ ^ ^ ^ |w|
#  ****************************    \m___m__|_|
# ** Note: $finish    : testfixture.v(157)
#    Time: 3072500 ps  Iteration: 0  Instance: /test
# 1
# Break in Module test at testfixture.v line 157
```

</td>
<td>

```
VSIM 33> run -all
#  ****************************
#  **                          **
#  **  Congratulations !!      **
#  **                          **        |__||
#  **  Simulation PASS !!      **       / 0.0  |
#  **                          **     /_____   |
#  **  Your score =100         **    /^ ^ ^ \  |
#  **                          **   |^ ^ ^ ^ |w|
#  ****************************    \m___m__|_|
# ** Note: $finish    : testfixture.v(157)
#    Time: 3080663 ps  Iteration: 0  Instance: /test
# 1
# Break in Module test at testfixture.v line 157
```

</td>
</tr>
<tr><td colspan="2">Synthesis Result</td></tr>
<tr><td>Total logic elements</td><td>15632</td></tr>
<tr><td>Total memory bit</td><td>0</td></tr>
<tr><td>Embedded multiplier 9-bit element</td><td>0</td></tr>
<tr><td colspan="2">

Compilation Report - MPQ

Flow Summary

<<Filter>>

Flow Status	Successful - Sun May 26 18:55:39 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	MPQ
Top-level Entity Name	MPQ
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	15,632 / 55,856 (28 %)
Total registers	2103
Total pins	50 / 325 (15 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	0 / 308 (0 %)
Total PLLs	0 / 4 (0 %)

</td></tr>
<tr><td colspan="2">Description of your design</td></tr>
<tr><td colspan="2">分為六個 state:
LOAD: 讀資料
READ_CMD: 讀 CMD
EXE_CMD: 因為有 heapify 和向上 SWAP，所以會需要在 build 和 heapify 等之間做切換
MAX_HEAPIFY
SWAP: for increase
DONE: busy<=0</td></tr>
</table>

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (Total cycle used*clock width)*