EE5710：系統晶片設計 (SOC Design)

Instructor: 施信毓教授

Office: 電資大樓 工EC7024室

E-mail: xyshih@mail.ee.nsysu.edu.tw

Objectives: You will learn to model digital circuit designs with Verilog and to use commercial CAD tools for system simulation, synthesis, scan chain insertion, ATPG, and APR of dedicated CPU designs.

Prerequisites: "Verilog" and "Computer Architecture" courses (if possible)

TAs: 李秉軒 (E-mail: alan@snsd.ee.nsysu.edu.tw)

謝佳翰 (E-mail: arthur@snsd.ee.nsysu.edu.tw)

吳明峻 (E-mail: benny@snsd.ee.nsysu.edu.tw)

Reference Textbooks: just for reference, not necessary

1. Michael D. Ciletti, *Modeling, Synthesis, and Rapid Prototyping with Verilog HDL*, Prentice Hall, 1999.
2. David A. Patterson, and John L. Hennessy, *Computer Organization and Design–The Hardware/Software Interface, 4th Edition,* Morgan Kaufman Publishers, Inc., 2009.

Course Outline:

Lecture 1: Introduction to System-on-chip Design

Lecture 2: Basic Verilog Coding for Combinational Building Blocks

Lecture 3: Basic Verilog Coding for Sequential Logics

Lecture 4: CPU Design Basics

Lecture 5: Pipelined CPU Design

Lecture 6: Introduction to Design for Testability (DFT) and Reliability

Lecture 7: Design Verification

Lecture 8: RTL Coding Guidelines

Grading Policy:

- **No writing homework & Exam!!**
- **Term project I: Creative Road** (**10%**)
- **Term project II: Game Excitation** (**20%**)
- **Term project III: Example Fighting** (**30%**)
- **Term project IV: Design Flow Father** (**30%**)
- **Term project V: Checking Farmer** (**10%**)

< Details > :

(1) **Term project I: Creative Road (CR)**

- Each group has **2~3** students.
- Main purpose: **Make your-own creative idea from current commercial CPU-based IC products.**
- Basic requirements:
  - Make a broad survey on current commercial CPU-based IC products and show the related background.
  - Describe your inspiration source.
  - Show your-own creative idea with possible benefits in more details.
- Totally at most **8 pages** for one group oral presentation with **15 minutes**. (No hard copy)
- Naming rule of presentation slides: **CR_GXX.ppt** (where XX is your group number)

(2) **Term project II: Game Excitation (GE)**

- Each group has **2~3** students. (Group members should be very different with term project I).
- Main purpose: **Make familiar with Verilog coding.**
- Basic requirements:
  - Develop an interesting game engine with your innovative ideas, including both combinational and sequential circuits.
  - Finish the RTL circuits.
  - Under **6-page** oral presentation slides, the shown content should provide the following items,
    - Game description in details
    - C/Matlab test patterns verified
    - Detailed hardware circuit with showing Verilog codes (*no more than 100 code lines*)
    - Verification with testbench
    - References: website, textbook, or other any possible study

resources

- Totally at most **6 pages** for one group oral presentation with **12 minutes**. (No hard copy)
- Naming rule of presentation slides: **GE_GXX.ppt** (where XX is your group number)

(3) **Term project III: Example Fighting (EF)**

- Each group has **2~3** students (Group members should be very different with term project I~II).
- Main purpose: **Solve the given IC problem/topic and develop the innovative thought with your team member co-operation.**
- Basic requirements:
  - Pass all of the test patterns in RTL-level for the given IC design topic.
  - Finish synthesis steps (showing area, speed, and power results) & pass all of the test patterns in gate-level.
- Totally at most **6 pages** for one group oral presentation with **12 minutes**. (No hard copy)
- Naming rule of presentation slides: **EF_GXX.ppt** (where XX is your group number)
- Also, you have to send out all your RTL Verilog codes in only one file (*.v) to **TA** by deadline of **11pm, the day before your oral presentation**. If you violate the hard rule, your term project score will be finally punished by discounted one half.
- Naming rule of your RTL Verilog file: **ef_gxx.v** (where xx is your group number)

(4) **Term project IV: Design Flow Father (DFF)**

- Each group has **2~3** students (Group members are **the same** with term project III).
- Main purpose: **Make the cell-based design-flow practice of utilizing commercial CAD tools, including scan chain insertion (DFT), ATPG, and APR.**
- Basic requirements:
  - You can refine your previous design in **term project III** with better design performance.
  - Finish scan chain insertion (DFT), ATPG, and APR.
  - Under **6-page** oral presentation slides, the shown content should provide the following items,

- ✧ Scan chain insertion (DFT): scanned Flip-Flop number, scan chain number, etc
- ✧ Synthesis and DFT result comparison in speed, area, and power point-of-view
- ✧ ATPG: fault coverage and test coverage
- ✧ APR results with layout view, including the number of final violations in your circuit layout

- Totally at most **6 pages** for one group oral presentation with **12 minutes**. (No hard copy)
- Naming rule of presentation slides: **DFF_GXX.ppt** (where XX is your group number)

(5) **Term project V: Checking Farmer (CF)**

- Each group has **2~3** students (Group members should be very different with term projects I~IV).
- Main purpose: **Have a precious opportunity to check other's Verilog codes.**
- Basic requirements:
  - ➢ You have to be assigned to check other's Verilog codes, given from different team at term project III).
  - ➢ Find out the good and bad RTL coding styles to show at the presentation stage.
- Totally at most **6 pages** for one group oral presentation with **12 minutes**. (No hard copy)
- Naming rule of presentation slides: **CF_GXX.ppt** (where XX is your group number)

< Attention for all of the term projects >

- **Grading criterion**:
  - ➢ **Completeness** (50%)
  - ➢ **Innovation** (50%)
- Presentation day:
  - ➢ Term project I (Creative Road): **@ Week 5**
  - ➢ Term project II (Game Excitation): **2 weeks** after "**lecture 3**" is finished by the instructor.
  - ➢ Term project III (Example Fighting): **@ Week 13**
  - ➢ Term project IV (Design Flow Father): **@ Week 18**
  - ➢ Term project V (Checking Farmer): **@ Week 17**
- You have to send out your presentation slides (*.ppt / *.pptx files) to **TA**

by deadline of **11pm, the day before your oral presentation**. If you violate the hard rule, your term project score will be finally punished by discounted one half.