Jiaxing Wu

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CS350

Lab 2

Step 5: Input = 7

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Register number** | **Register name** | **Before syscall(one step before)** | **After syscall(one step after)** | **Changed** |
| PC | PC | 400038 | 40003c | 400038 to 40003c |
| 0 | $r0 | 0 | 0 | nothing |
| 1 | $at | 0 | 0 | nothing |
| 2 | $vo | 5 | 7 | 5 to 7 |
| 3 | $v1 | 0 | 0 | nothing |
| 4 | $a0 | 10000000 | 10000000 | nothing |
| 5 | $a1 | 7ffffe14 | 7ffffe14 | nothing |
| 6 | $a2 | 7ffffe1c | 7ffffe1c | nothing |
| 7 | $a3 | 0 | 0 | nothing |
| 8 | $t0 | 0 | 0 | nothing |
| 9 | $t1 | 0 | 0 | nothing |
| 10 | $t2 | 0 | 0 | nothing |
| 11 | $t3 | 0 | 0 | nothing |
| 12 | $t4 | 0 | 0 | nothing |
| 13 | $t5 | 0 | 0 | nothing |
| 14 | $t6 | 0 | 0 | nothing |
| 15 | $t7 | 0 | 0 | nothing |
| 16 | $s0 | 400018 | 400018 | nothing |
| 17 | $s1 | 0 | 0 | nothing |
| 18 | $s2 | 0 | 0 | nothing |
| 19 | $s3 | 0 | 0 | nothing |
| 20 | $s4 | 0 | 0 | nothing |
| 21 | $s5 | 0 | 0 | nothing |
| 22 | $s6 | 0 | 0 | nothing |
| 23 | $s7 | 0 | 0 | nothing |
| 24 | $t8 | 0 | 0 | nothing |
| 25 | $t9 | 0 | 0 | nothing |
| 26 | $k0 | 0 | 0 | nothing |
| 27 | $k1 | 0 | 0 | nothing |
| 28 | $gp | 10008000 | 10008000 | nothing |
| 29 | $sp | 7ffffe10 | 7ffffe10 | nothing |
| 30 | $fp | 0 | 0 | nothing |
| 31 | $ra | 400018 | 400018 | nothing |

Step 7:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Register number** | **Register name** | **Before sll(one step before)** | **After sll(one step after)** | **Changed** |
| PC | PC | 400040 | 400044 | 400040 to 400044 |
| 0 | $r0 | 0 | 0 | nothing |
| 1 | $at | 0 | 0 | nothing |
| 2 | $vo | 7 | 7 | nothing |
| 3 | $v1 | 0 | 0 | nothing |
| 4 | $a0 | 10000000 | 10000000 | nothing |
| 5 | $a1 | 7ffffe14 | 7ffffe14 | nothing |
| 6 | $a2 | 7ffffe1c | 7ffffe1c | nothing |
| 7 | $a3 | 0 | 0 | nothing |
| 8 | $t0 | 7 | 7 | nothing |
| 9 | $t1 | 0 | 1c | 0 to 1c |
| 10 | $t2 | 0 | 0 | nothing |
| 11 | $t3 | 0 | 0 | nothing |
| 12 | $t4 | 0 | 0 | nothing |
| 13 | $t5 | 0 | 0 | nothing |
| 14 | $t6 | 0 | 0 | nothing |
| 15 | $t7 | 0 | 0 | nothing |
| 16 | $s0 | 400018 | 400018 | nothing |
| 17 | $s1 | 0 | 0 | nothing |
| 18 | $s2 | 0 | 0 | nothing |
| 19 | $s3 | 0 | 0 | nothing |
| 20 | $s4 | 0 | 0 | nothing |
| 21 | $s5 | 0 | 0 | nothing |
| 22 | $s6 | 0 | 0 | nothing |
| 23 | $s7 | 0 | 0 | nothing |
| 24 | $t8 | 0 | 0 | nothing |
| 25 | $t9 | 0 | 0 | nothing |
| 26 | $k0 | 0 | 0 | nothing |
| 27 | $k1 | 0 | 0 | nothing |
| 28 | $gp | 10008000 | 10008000 | nothing |
| 29 | $sp | 7ffffe10 | 7ffffe10 | nothing |
| 30 | $fp | 0 | 0 | nothing |
| 31 | $ra | 400018 | 400018 | nothing |

Step 8:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Register number** | **Register name** | **Before jal**  **0x0040002(one step before)** | **After jal**  **0x0040002(one step after)** | **Changed** |
| PC | PC | 400014 | 400024 | 400014 to 400024 |
| 0 | $r0 | 0 | 0 | nothing |
| 1 | $at | 0 | 0 | nothing |
| 2 | $vo | 4 | 4 | nothing |
| 3 | $v1 | 0 | 0 | nothing |
| 4 | $a0 | 1 | 1 | nothing |
| 5 | $a1 | 7ffffe14 | 7ffffe14 | nothing |
| 6 | $a2 | 7ffffe1c | 7ffffe1c | nothing |
| 7 | $a3 | 0 | 0 | nothing |
| 8 | $t0 | 0 | 0 | nothing |
| 9 | $t1 | 0 | 0 | nothing |
| 10 | $t2 | 0 | 0 | nothing |
| 11 | $t3 | 0 | 0 | nothing |
| 12 | $t4 | 0 | 0 | nothing |
| 13 | $t5 | 0 | 0 | nothing |
| 14 | $t6 | 0 | 0 | nothing |
| 15 | $t7 | 0 | 0 | nothing |
| 16 | $s0 | 0 | 0 | nothing |
| 17 | $s1 | 0 | 0 | nothing |
| 18 | $s2 | 0 | 0 | nothing |
| 19 | $s3 | 0 | 0 | nothing |
| 20 | $s4 | 0 | 0 | nothing |
| 21 | $s5 | 0 | 0 | nothing |
| 22 | $s6 | 0 | 0 | nothing |
| 23 | $s7 | 0 | 0 | nothing |
| 24 | $t8 | 0 | 0 | nothing |
| 25 | $t9 | 0 | 0 | nothing |
| 26 | $k0 | 0 | 0 | nothing |
| 27 | $k1 | 0 | 0 | nothing |
| 28 | $gp | 10008000 | 10008000 | nothing |
| 29 | $sp | 7ffffe10 | 7ffffe10 | nothing |
| 30 | $fp | 0 | 0 | nothing |
| 31 | $ra | 0 | 400018 | 0 to 400018 |

Step 9:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Register number** | **Register name** | **Before jr $ra(one step before)** | **After jr $ra(one step after)** | **Changed** |
| PC | PC | 400054 | 400018 | 400054 to 400018 |
| 0 | $r0 | 0 | 0 | nothing |
| 1 | $at | 0 | 0 | nothing |
| 2 | $vo | 1 | 1 | nothing |
| 3 | $v1 | 0 | 0 | nothing |
| 4 | $a0 | 1c | 1c | nothing |
| 5 | $a1 | 7ffffe14 | 7ffffe14 | nothing |
| 6 | $a2 | 7ffffe1c | 7ffffe1c | nothing |
| 7 | $a3 | 0 | 0 | nothing |
| 8 | $t0 | 7 | 7 | nothing |
| 9 | $t1 | 1c | 1c | nothing |
| 10 | $t2 | 0 | 0 | nothing |
| 11 | $t3 | 0 | 0 | nothing |
| 12 | $t4 | 0 | 0 | nothing |
| 13 | $t5 | 0 | 0 | nothing |
| 14 | $t6 | 0 | 0 | nothing |
| 15 | $t7 | 0 | 0 | nothing |
| 16 | $s0 | 400018 | 400018 | nothing |
| 17 | $s1 | 0 | 0 | nothing |
| 18 | $s2 | 0 | 0 | nothing |
| 19 | $s3 | 0 | 0 | nothing |
| 20 | $s4 | 0 | 0 | nothing |
| 21 | $s5 | 0 | 0 | nothing |
| 22 | $s6 | 0 | 0 | nothing |
| 23 | $s7 | 0 | 0 | nothing |
| 24 | $t8 | 0 | 0 | nothing |
| 25 | $t9 | 0 | 0 | nothing |
| 26 | $k0 | 0 | 0 | nothing |
| 27 | $k1 | 0 | 0 | nothing |
| 28 | $gp | 10008000 | 10008000 | nothing |
| 29 | $sp | 7ffffe10 | 7ffffe10 | nothing |
| 30 | $fp | 0 | 0 | nothing |
| 31 | $ra | 400018 | 400018 | nothing |

Step 10: Jal is jump and link. It jumps to a target address and saves/links the address of the instruction one step after to the 31 or ra register. Jr just jumps to a target address but doesn’t save/link the instruction address after it.