

ENGI-9865 Project

File / Directory	Note
software/	The software side of our project. Explained in detail below.
src_doc/	The source (.tex and .cls files and all pictures embed in the report) of the document of 9865.final.pdf.
testbench/	The testbench project.
9865.final.pdf	The final project report.
block_breaker.qar	The Quartus II project archive that <u>containing only hardware side of our project.</u>

Steps to run our project is listed below.

1. How to run testbench

First unpack block_breaker.qar to restore the Quartus II project.

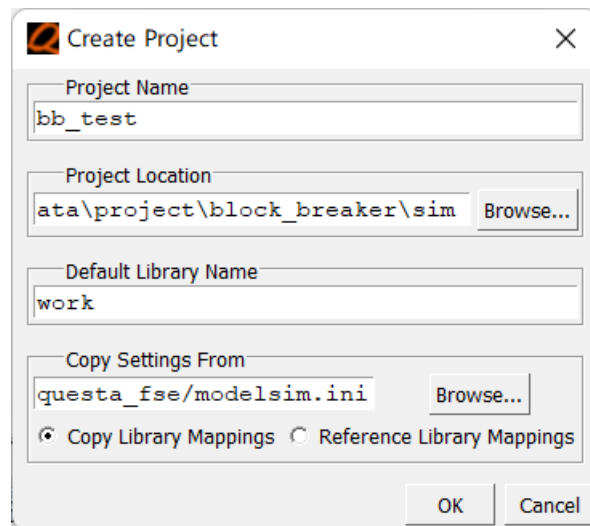
Assuming the restored project root folder is called “block_breaker”, then

```
$ cp -r testbench/ block_breaker/
```

Then, to run testbench,

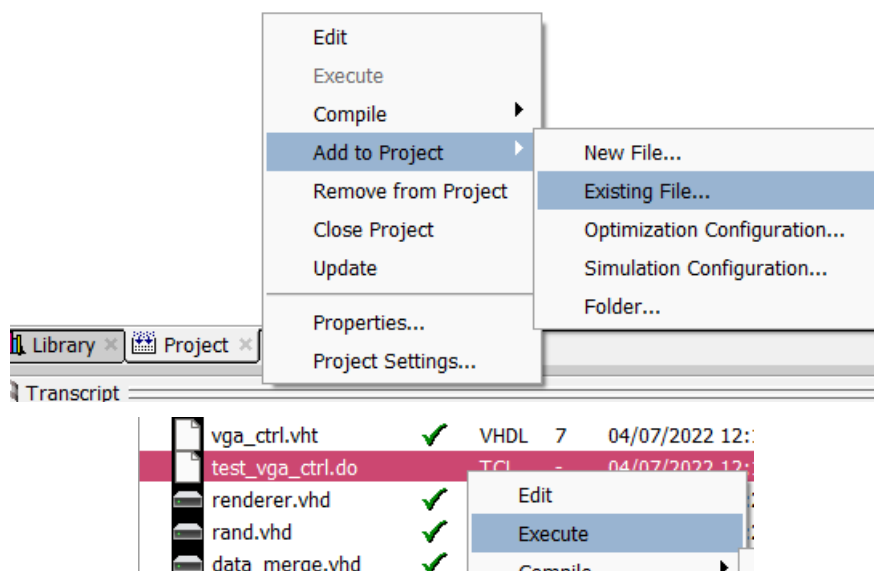
```
$ vsim
```

Using vsim command or some others ways to launch the QuestaSim or ModelSim software, **creating a new QuestaSim/ModelSim project**, the project name can be arbitrary, the project root should be in the testbench folder, then choose “Add Existing Files”, and select everything inside the testbench folder.



Project - E:/data/project/block_breaker/sim/bb_sim

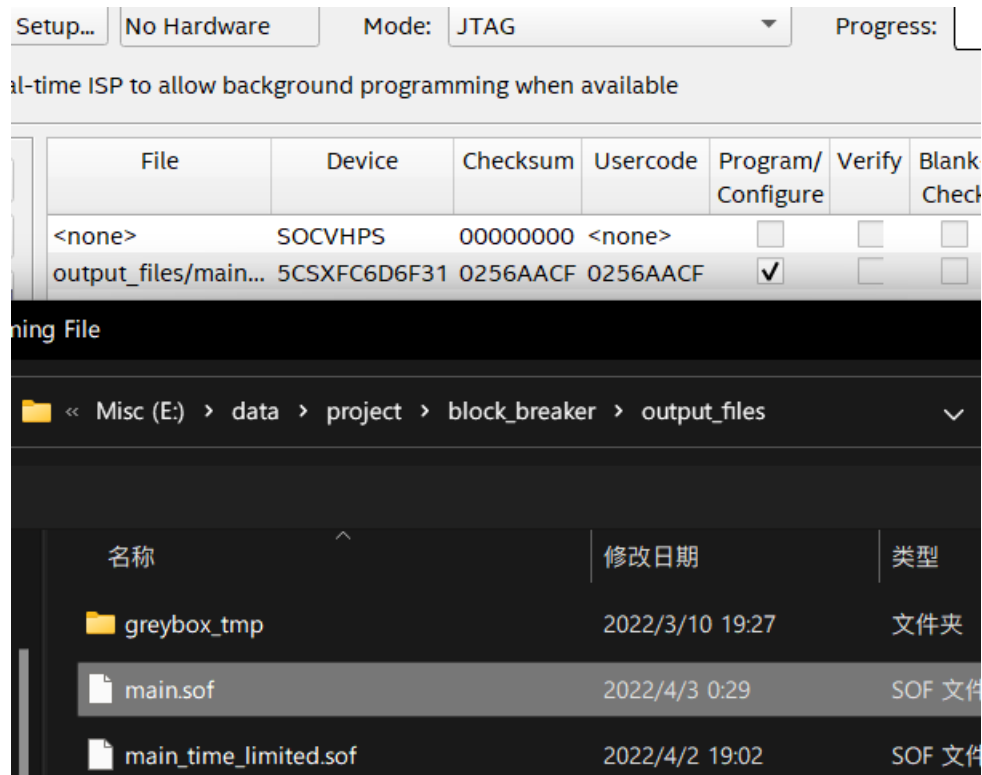
Name	Status	Type	Order	Modified
pll2.vhd	✓	VHDL	2	03/10/2022 05:56:28 ...
vga_ctrl.vhd	✓	VHDL	4	04/02/2022 09:56:04 ...
vga_ctrl.vht	✓	VHDL	7	04/07/2022 12:17:41 ...
test_vga_ctrl.do		TCL	-	04/07/2022 12:12:53 ...
renderer.vhd	✓	VHDL	3	03/13/2022 06:24:42 ...
rand.vhd	✓	VHDL	0	03/26/2022 07:28:51 ...
data_merge.vhd	✓	VHDL	1	04/02/2022 08:38:12 ...
rand.vht	✓	VHDL	5	03/26/2022 10:00:22 ...
test_rand.do		TCL	-	04/06/2022 11:52:16 ...
data_merge.vht	✓	VHDL	6	04/06/2022 11:37:29 ...
test_data_merge.do...		TCL	-	04/06/2022 11:52:09 ...



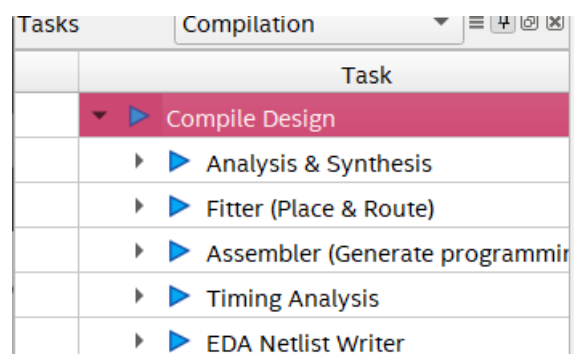
Finally, switch to project tab and select one TCL file (.do files), right click, and select “Execute”, after several seconds should the auto-generated test report appears.

2. How to download the hardware side to the DE-10 board

In the unpacked (restored) Quartus II project, there is already a prepared .sof file located in output_files/main.sof. Using programmer to download this file directly to the board.



To re-compile the project for a new .sof file: Just double click “Compile Design”.



3. How to restore and compile the software side (NIOS-II)

First configure the Eclipse IDE and NIOS-II development environment for Quartus II, by following this official instruction:

<https://www.intel.com/content/www/us/en/support/programmable/articles/000086893.html>

Then configure all environment variables, adding the following to the \$PATH. This step is vitally important but there are no helps related to this on the internet.

```
Path\to\intelFPGA_lite\21.1\questa_fse\win64  
Path\to\intelFPGA_lite\21.1\nios2eds\bin\gnu\H-x86_64-mingw32\bin  
Path\to\intelFPGA_lite\21.1\nios2eds\bin  
Path\to\intelFPGA_lite\21.1\quartus\bin64  
Path\to\intelFPGA_lite\21.1\nios2eds\sdk2\bin
```

Before adding these, replace the paths to the absolute path of your own intelFPGA installation location.

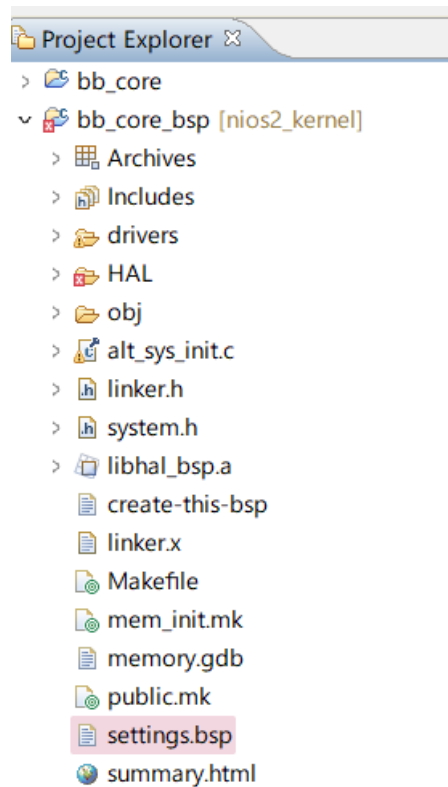
Then,

```
$ cp -r software/ block_breaker/
```

Then launch the eclipse from Quartus II (Menu: Tools -> Nios II Software Build Tools for Eclipse),

and **set the block_breaker/software directory as the workspace.**

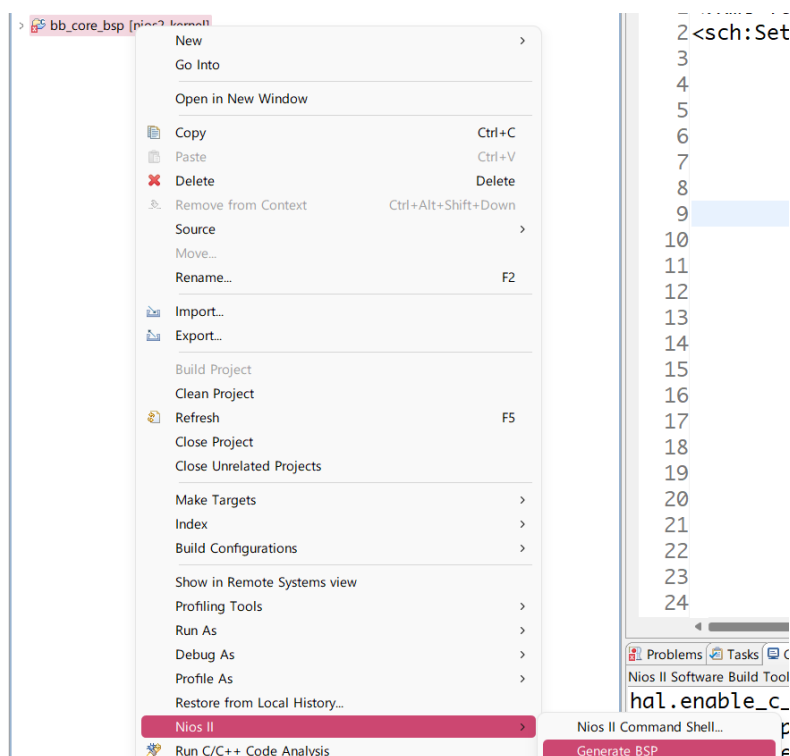
(See next page)

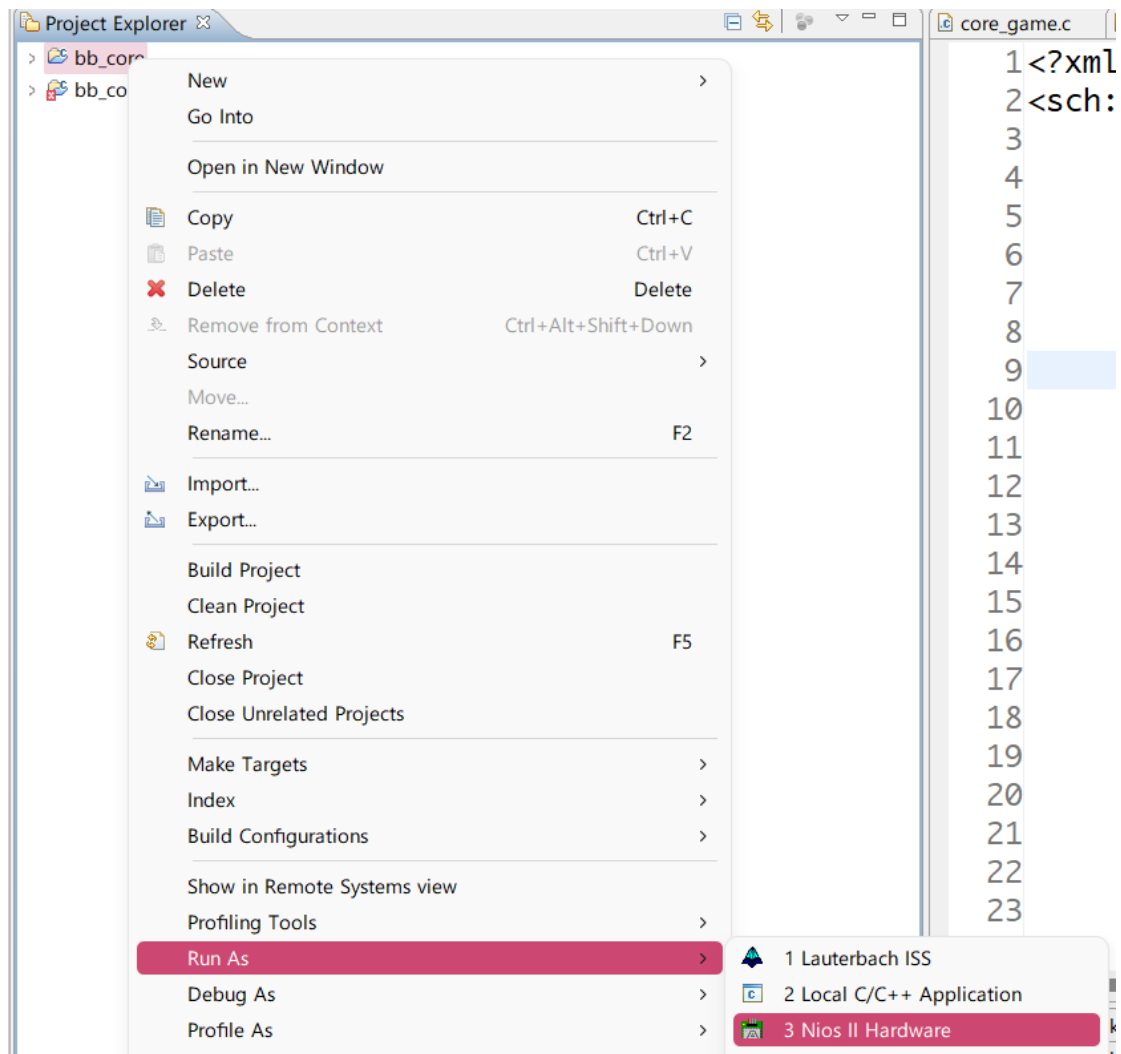


Editing the settings.bsp, replacing all “E:\data\project\block_breaker\”

Partterns to the absolute path to the block_breaker folder.

Then generate BSP:





Finally, connect the board to computer, **first download the hardware side**, then compile and download the software side, operate as the picture shows.

4. How to run software test using Easy Test

```
$ cd software/bb_core/test  
$ sh run_test
```

Zhen Guan (202191382, zguan@mun.ca)

Jiabao Guo (202096888, jiabaog@mun.ca)