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1.6 [20] <§1.6> Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.

Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

a. What is the global CPI for each implementation?

b. Find the clock cycles required in both cases.

a. For implementation P1.

clock rate: 2.5GHz

	A	B	C	D
CPI	1	2	3	3
	10%	20%	50%	20%

⇒ global CPI = 1×10% + 2×20% + 3×50% + 3×20% = 2.6

CPU time = $\frac{2.6 \times 1.0E6}{2.5 \times 1.0E9}$ = 1.04 ms

For implementation P2

⇒ global CPI = 2×10% + 2×20% + 2×50% + 2×20% = 2

CPU time = $\frac{2 \times 1.0E6}{3.0 \times 1.0E9}$ = 0.67 ms

⇒ So the second implementation is faster.

b. clock cycles = Instruction counts × clock cycles per instruction

For implementation P1.

⇒ clock cycles = 1.0E6 × 2.6 = 2.6E6.

For implementation P2.

⇒ clock cycles = 1.0E6 × 2.0 = 2.0E6

1.8 The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power.

The Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.

1.8.1 [5] <§1.7> For each processor find the average capacitive loads.

1.8.2 [5] <§1.7> Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.

1.8.3 [15] <§1.7> If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current? Note: power is defined as the product of voltage and current.

1.8.1. $P = P_{static} + P_{dynamic}$

$C = \frac{2P_D}{V^2 \cdot \text{frequency switched}}$

For Pentium 4 Prescott processor

Capacitive loads = $\frac{2 \times 90}{1.25^2 \times 3.6E9}$ = 32 pF

For Core i5 Ivy Bridge

Capacitive loads = $\frac{2 \times 40}{0.9^2 \times 3.4E9}$ ≈ 29 pF

1.8.2

	percentage of the total dissipated power	the ratio of static power to dynamic power
Pentium 4	$\frac{10}{90+10} = 10\%$	$\frac{10}{90} = \frac{1}{9}$
Core i5	$\frac{30}{30+40} = 43\%$	$\frac{30}{40} = \frac{3}{4}$

1.15 [5] <§1.8> When a program is adapted to run on multiple processors in a multiprocessor system, the execution time on each processor is comprised of computing time and the overhead time required for locked critical sections and/or to send data from one processor to another.

Assume a program requires t = 100 s of execution time on one processor. When run *p* processors, each processor requires t/p s, as well as an additional 4 s of overhead, irrespective of the number of processors. Compute the per-processor execution time for 2, 4, 8, 16, 32, 64, and 128 processors. For each case, list the corresponding speedup relative to a single processor and the ratio between actual speedup versus ideal speedup (speedup if there was no overhead).

As saying,

p is the number of processors,

total time $T(p) = \frac{t}{p} + 4$

number of processors	2	4	8	16	32	64	128
execution time	54	29	16.5	10.25	7.125	5.5625	4.78125
speedup	1.85	3.45	6.06	9.76	14.04	17.98	20.92
actual speedup / ideal speedup	92.6%	86.2%	75.8%	61.0%	43.9%	28.1%	16.3%

1.8.3.

- For Pentium 4 Prescott Process

$P_S = 10W$, $P_D = 90W$, $U = 1.25V$

The new power requirement is 90 W

The current $I = \frac{P_S}{U} = 8A$

$P_{new} = I \cdot U_{new} + \frac{1}{2} U_{new}^2 \cdot C \cdot \text{frequency switched}$

⇒ $U_{new} = 1.18V$

- For Core i5 Ivy Bridge

$P_S = 30W$, $P_D = 40W$, $U = 0.9V$

The new power requirement is 63 W

The current $I = \frac{P_S}{U} = 33.3A$

$P_{new} = I \cdot U_{new} + \frac{1}{2} U_{new}^2 C \cdot \text{frequency switched}$

⇒ $U_{new} = 0.84V$