同济大学计算机系

数字逻辑课程实验报告

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一、实验内容

使用 Verilog HDL 语言实现行为级 ALU 的设计和仿真

二、模块建模

```
`timescale 1ns / 1ps
module alu(
    input [31:0] a,
    input [31:0] b,
    input [3:0] aluc,
    output reg [31:0] r,
    output reg zero,
    output reg carry,
    output reg negative,
    output reg overflow
    );
    reg [32 : 0] temp;
    reg signed [31:0] temp_b;
    always @(*)
        casex (aluc)
            4'b0000:        //a+b unsigned
            begin
                r = a + b;
                temp = {1'b0, a} + {1'b0, b};
                zero = (r == 0) ? 1 : 0;
                carry = temp[32];
                negative = r[31];
                overflow = 0;
            end

            4'b0010:        //a+b signed
            begin
                r = a + b;
                zero = (r == 0) ? 1 : 0;
                carry = 0;
                negative = r[31];
                overflow = ((a[31] == b[31]) && (r[31] != a[31])) ? 1 : 0;
            end

            4'b0001:        //a-b unsigned
            begin
                r = a - b;
                zero = (r == 0) ? 1 : 0;
```

```
        carry = (a < b) ? 1 : 0;
        negative = r[31];
        overflow = 0;
end

4'b0011:        //a-b signed
begin
        r = a - b;
        zero = (r == 0) ? 1 : 0;
        carry = 0;
        negative = r[31];
        overflow = ((a[31] != b[31]) && (r[31] != a[31])) ? 1 : 0;
end

4'b0100:        //a&b
begin
        r = a & b;
        zero = (r == 0) ? 1 : 0;
        carry = 0;
        negative = r[31];
        overflow = 0;
end

4'b0101:        //a|b
begin
        r = a | b;
        zero = (r == 0) ? 1 : 0;
        carry = 0;
        negative = r[31];
        overflow = 0;
end

4'b0110:        //a^b
begin
        r = a ^ b;
        zero = (r == 0) ? 1 : 0;
        carry = 0;
        negative = r[31];
        overflow = 0;
end

4'b0111:        //~(a|b)
begin
        r = ~(a | b);
```

```
        zero = (r == 0) ? 1 : 0;
        carry = 0;
        negative = r[31];
        overflow = 0;
    end

    4'b100x:        //{b[15:0, 16'b0]}
    begin
        r = {b[15:0], 16'b0};
        zero = (r == 0) ? 1 : 0;
        carry = 0;
        negative = r[31];
        overflow = 0;
    end

    4'b1011:        //a<b signed
    begin
        r = a - b;
        zero = (r == 0) ? 1 : 0;
        carry = 0;
        negative = r[31];
        overflow = ((a[31] != b[31]) && (r[31] != a[31])) ? 1 : 0;
        r = (overflow == 1 || (r[31] == 1)) ? 1 : 0;
    end

    4'b1010:        //a<b unsigned
    begin
        r = a - b;
        zero = (r == 0) ? 1 : 0;
        carry = (a < b) ? 1 : 0;
        negative = 0; //  无符号数比较运算不影响  negative  标志位
        overflow = 0;
        r = carry;
    end

    4'b1100:        //b>>>a algo
    begin
        temp_b = b;
        r = temp_b >>> a;
        zero = (r == 0) ? 1 : 0;
        carry = (a >= 32) ? b[31] : b[a];
        negative = r[31];
        overflow = 0;
    end
```

```
            4'b111x:        //b<<a
            begin
                r = b << a;
                zero = (r == 0) ? 1 : 0;
                carry = (a >= 32) ? 0 : b[31-a];
                negative = r[31];
                overflow = 0;
            end

            4'b1101:        //b>>a logi
            begin
                r = b >> a;
                zero = (r == 0) ? 1 : 0;
                carry = (a >= 32) ? 0 : b[a];
                negative = r[31];
                overflow = 0;
            end

            default:
            begin
                r = 1'bz; zero = 1'bz; carry = 1'bz; negative = 1'bz; overflow = 1'bz;
            end
        endcase
endmodule
```

三、测试模块建模

```
`timescale 1ns / 1ps
module alu_tb;
    reg [31:0] a, b;
    reg [3:0] aluc;
    wire [31:0] r;
    wire zero, carry, negative, overflow;

    alu uut(.a(a), .b(b), .aluc(aluc),
            .r(r),
            .zero(zero), .carry(carry), .negative(negative), .overflow(overflow));

    initial
    begin
        aluc <= 4'b0000;
        a <= 32'hffffffff; b <= 32'h00000001;
        #20 aluc <= 4'b0010;
```

```
        a <= 32'h7fffffff; b <= 32'h00000001;

        #20 aluc <= 4'b0001;
        a <= 32'h00000001; b <= 32'hffffffff;
        #20 aluc <= 4'b0011;
        a <= 32'h80000000; b <= 32'h00000001;

        #20 aluc <= 4'b0100;
        a <= 32'hffffffff; b <= 32'haaaaaaaa;
        #20 aluc <= 4'b0101;
        #20 aluc <= 4'b0110;
        #20 aluc <= 4'b0111;
        #20 aluc <= 4'b1001;
        #10 aluc <= 4'b1000;

        #10 aluc <= 4'b1011;
        a <= 32'hffffffff; b <= 32'h7fffffff;
        #20 aluc <= 4'b1010;

        #20 aluc <= 4'b1100;
        a <= 32'h00000010; b<= 32'hf1234567;
        #20 aluc <= 4'b1110;
        #20 aluc <= 4'b1101;
        #20 aluc <= 4'b1111;
    end
endmodule
```

四、实验结果