1. a. block offset: 4-0

block size: 2^5 bytes = 8 words

b. Index: 9-5

blocks: $2^5 = 32$

c. Total bits 32 X (1 valid bit + 54 tag bits + 32X8 data bits)

Data bits 32 X (32 X 8 data bits)

Ratio = Total bits / Data bits

= 1.2148

d. (1) reference:

	tag	index	offset	hit/miss	
0	0~0	00000	00000	miss	
4	0~0	00000	00100	hit	
16	0~0	00000	10000	hit	
132	0~0	00100	00100	miss	
232	0~0	00111	01000	miss	
160	0~0	00101	00000	miss	
1024	0~01	00000	00000	miss	☆ replace
30	0~0	00000	11110	miss	replace
140	0~0	00100	01100	hit	
3100	0~011	00000	11100	miss	replace
180	0~0	00101	10100	hit	
2180	0~010	00100	00100	miss	replace

e. hit ratio = hit / (hit + miss) = 4/(4+8) = 33.3%

f. final state

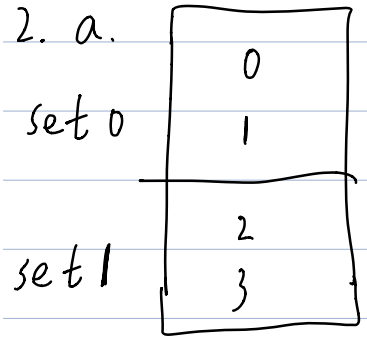
< 00000, 0 ~ 011, mem[3072] - Mem[3103] >

< 00100, 0 ~ 010, mem[2176] - Mem[2207] >

< 00101, 0 ~ 000, mem[160] - Mem[191] >

< 00111, 0 ~ 000, mem[224] - Mem[255] >

2. a.

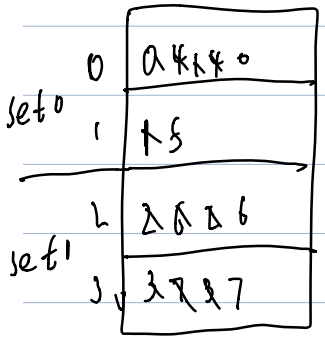


LRU

set 0	0	a4x40
	1	xs
set 1	2	2626
	3	3737

0	1	2	3	4	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0
M	M	M	M	M	H	H	H	M	M	M	M	M	M	M	M	H	M	M	M

b. MRU



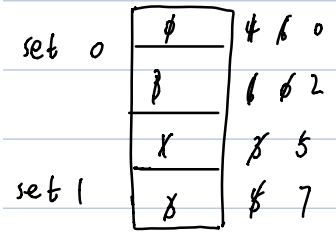
0	1	2	3	4	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0
M	M	M	M	M	H	H	H	M	M	M	M	M	M	M	M	H	M	M	M

c.

d. optimal:

0 1 2 3 4 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0

M M M M H H H H H H H H H H H H H H M M



hit 14

miss 6

e: the optimal replacement policy looks for the pages that have least changes of getting used in future. Thus it is necessary for CPU to know what page frame would be demanded.

3. a. P1: clock rates = 1/L1 hit time = 1/0.66 = 1.515 GHz

P2: clock rates = 1/L1 hit time = 1/0.99 = 1.11 GHz

b. P1:

L1 hit time + L1 miss rate * mem access Time

= 0.66 + (8% X 70) = 6.26ns

P2:

L1 hit time + L1 miss rate * mem access Time

= 0.90 + (6% X 70) = 5.10 ns

c.

P_1: $1 + 36\% \times 8\% \times 70 / 0.66 = 4.054$

P_2: $1 + 36\% \times 6\% \times 70 / 0.90 = 2.68$

$4.054 \times 0.66 = 2.67564$

$\vee$

$2.68 \times 0.9 = 2.412$

thus: Processor P_2 is faster.

d. P_1:

L_1 hit time + L_1 miss rate * (L_2 hit time + L_2 miss rate · MAT)

$= 0.66 + 8\% (5.62 + 95\% \times 70)$

$= 6.4296$ ns

The AMAT has become worse on adding an extra L2 cache.

e. $1 + 36\% \times 8\% \times (5.62 + 95\% \times 70) / 0.66$

$= 1 + 3.14 = 4.14$

f. P_1 with out L_2 2.67564 (time per I)

with L_2 $(1 + 36\% \times 8\% \times (5.62 + R \times 70) / 0.66) * 0.66 < 2.67564$

thus $R > 0.9194$