**Signal Naming Convention:**

*(generating\_unit)*\_*(signal\_name)*\_*(pipeline\_stage)*[\_b if active low]

**CS\_MUX\_RESULT\_EX**

selects whether the ALU or Shifter result goes into WB.results

1'b0 = ALU result

1'b1 = Shifter result

**CS\_MUX\_SRC1\_AG**

select source of A at address generation stage

1'b00 = reg\_A

1'b01 = seg\_src

**CS\_MUX\_SRC1\_ME**

select source of A at memory stage

1'b00 = ME.A

1'b01 = mem\_result

**CS\_MUX\_SRC2\_AG**

selects source of B at address generation stage

2'b00 = reg\_B

2'b01 = seg\_src

2'b10 = AG.imm

**CS\_MUX\_SRC2\_ME**

select source of B at memory stage

1'b00 = ME.A

1'b01 = mem\_result

**CS\_MUX\_ALUK\_DE**

selects whether the AG.ALUK will come from the control store or the reg/opcode bits of the instruction itself.

1'b0 = control store

1'b1 = reg/opcode

**CS\_ALUK\_EX**

selects operation for ALU

3'b000 = add

3'b001 = or

3'b010 = not

3'b011 = xchg

3'b100 = and

3'b101 = daa

3'b110 = cmp

3'b111 = chk\_if\_zero

**CS\_SR1\_NEEDED\_AG**

true if instruction sources operand1 from GPR

1'b0 = false

1'b1 = true

**CS\_SR2\_NEEDED\_AG**

true if instruction sources operand2 from GPR

1'b0 = false

1'b1 = true

**CS\_LD\_DR\_WB**

true if instruction writes back to GPR

1'b0 = false

1'b1 = true

**CS\_SEG1\_NEEDED\_AG**

true if instruction sources operand1 from segment register

1'b0 = false

1'b1 = true

**CS\_SEG2\_NEEDED\_AG**

true if instruction sources operand2 from segment register

1'b0 = false

1'b1 = true

**CS\_LD\_SEG\_WB**

true if instruction writes back to segment register

1'b0 = false

1'b1 = true

**CS\_MM1\_NEEDED\_AG**

true if instruction sources MM operand1 from MM register

1'b0 = false

1'b1 = true

**CS\_MM1\_NEEDED\_AG**

true if instruction sources MM operand1 from MM register

1'b0 = false

1'b1 = true

**CS\_MM2\_NEEDED\_AG**

true if instruction sources MM operand2 from MM register

1'b0 = false

1'b1 = true

**CS\_LD\_MM\_WB**

true if instruction writes back to MM register

1'b0 = false

1'b1 = true

**CS\_LD\_FLAGS\_WB**

true if instruction writes back to Flags

1'b0 = false

1'b1 = true

**CS\_SIB\_S\_NEEDED\_AG**

true if instruction sources SIB's scale from GPR

1'b0 = false

1'b1 = true

**CS\_SIB\_I\_NEEDED\_AG**

true if instruction sources SIB's index from GPR

1'b0 = false

1'b1 = true

**CS\_MEM\_READ\_ME**

true if instruction needs to read from dcache

1'b0 = false

1'b1 = true

**CS\_MEM\_WRITE \_WB**

true if instruction writes back to memory

1'b0 = false

1'b1 = true

**CS\_DATA\_SIZE\_DE**

data\_size if determinable from opcode

2'b00 = 8 bits

2'b10 = 32 bits

2'b11 = 64 bits