**Latch Naming Convention:**

*(SIGNAL\_NAME)*[\_b if active low]

*In verilog, (PIPE\_STAGE)*\_*(SIGNAL\_NAME)[\_b if active low]* *indicates that the latch for a particular stage*

**MOD** (2 bits)

mod field (3bits) from ModR/M of raw instruction

**SR1** (3 bits)

register identifier associated with either:

1) r/m field (ModR/M)

2) AL/AX/EAX

4) SIB\_Base

|  |  |
| --- | --- |
| 000 | AL/AX/EAX |
| 001 | CL/CX/ECX |
| 010 | DL/DX/EDX |
| 011 | BL/BX/EBX |
| 100 | AH/SP/ESP |
| 101 | CH/BP/EBP |
| 110 | DH/SI/ESI |
| 111 | BH/DI/EDI |

**SR2** (3 bits)

register identifier associated with either

1) reg field (ModR/M)

**SIB\_INDEX** (3 bits)

register identifier for index

**IMM** (32 bits)

immediate field from raw instruction

**DISP** (32 bits)

displacement field from raw instruction

**V** (1 bit)

determines if Memory stage is valid or a bubble

**SEGR**

|  |  |
| --- | --- |
| 000 | CS |
| 001 | DS |
| 010 | SS |
| 011 | ES |
| 100 | FS |
| 101 | GS |

**A**

Operand A

**B**

Operand B

**MEM** **Specific**

**ME\_ADDRESS**

Physical Address

**WB Specific**

**WB\_RESULT**

Result from ALU or other logical units

**WB\_Flags**

Falgs from ALU or other logical units