**Latch Naming Convention:**

*(SIGNAL\_NAME)*[\_b if active low]

*In verilog, (PIPE\_STAGE)*\_*(SIGNAL\_NAME)[\_b if active low]* *indicates that the latch for a particular stage*

**MOD** (2 bits)

mod field (3bits) from ModR/M of raw instruction

**R\_M** (3 bits)

r/m field (3bits) from ModR/M of raw instruction

**REG** (3 bits)

reg field (3bits) from ModR/M of raw instruction

**IMM** (32 bits)

immediate field from raw instruction

**DISP** (32 bits)

displacement field from raw instruction

**V** (1 bit)

determines if Memory stage is valid or a bubble

**ME\_**