Analysis and Design of High Performance Wireless Power Delivery Using On-chip Octagonal Inductor in 65-nm CMOS

Weijun Mao, Liusheng Sun, Junwei Xu, Jiajia Wu, Xiaolei Zhu
Institute of VLSI Design
Zhejiang University
310027 Hangzhou, P. R. China
zhuxl@vlsi.zju.edu.cn

***Abstract*—This paper analyzes and designs inductive coupling power delivery (ICPD) system for 3-D stacked chips in SMIC 65-nm CMOS process. Two shapes of inductors, the rectangular and the octagonal inductor, are compared. Fully customized octagonal inductors with 500 μm diameter are optimized to improve power delivery efficiency. An octagonal inductor based ICPD consisting transmitter and receiver circuit is proposed by using H-bridge architecture and NMOS cross-gate rectifier. Simulation results show that the received power is 12 mW with a delivery efficiency of 12% and a power density of 59.5 mW/mm^2. In order to achieve the higher power at the receiver side in some special applications, a four parallel connected inductors based wireless power link is designed, which reaches 34.2 mW.**

Keywords—wireless; inductor; power; efficiency

I. INTRODUCTION

Three–dimensional (3D) System in a package (SiP) is a possible way of reducing cost and realizing high-density, high-performance LSI (Large Scale Integration) system [1]. In a 3D system, chips are stacked and connected with vertical inter-chip links. The total performance of the 3D system is affected by the inter-chip link. For data and clock transmission among stacked chips, wireless data transmission technologies have been widely investigated [2]-[3]. In previous works of wireless data link [2]-[3], power is transmitted to the chips by bonding wires. However, in conventional wire-bonding based 3-D SiP, the bonding will become complicated and unreliable when hundreds of input/output is stacked on top of the other. Wireless power delivery to IC chips is proposed to solve this problem. As is shown in Fig. 1, a SiP with wireless power delivery channel and wireless data transmission channel can be accessed without mechanical contacts. Also, non-contact interfaces mitigate risks of damaging thinned and 3-D stacked chips due to mechanical stress while bonding [4].

There are two different ways to deliver the power wirelessly in a near filed, capacitive-coupling and inductive-coupling [5]. However, capacitive-coupling technology has a limitation. It is a voltage-driven scheme and the received voltage can't be higher than the transmitter voltage without using a pull-up rectifier circuit. By contrast, the inductive-coupling technology is a current-driven scheme and the received voltage can be controlled by setting the ratio of the two inductors, which makes it flexible. Therefore, designing a pair of inductors to make the system operating in high efficiency is crucial.

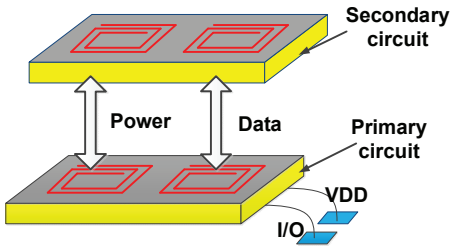

Fig. 1. SiP with wireless power and data transmission

This paper analyses the optimization of the circuit design, specifically the inductor, and improve the delivery efficiency and power density. Simulation results show that the output power of the receiver with single inductor is 12.05mW with a delivery efficiency of 12.7% and a power density of 59.5 mW/mm^2, improved 23% and 197.5%, respectively compared with previous work [6]. The output power of the receiver with four parallel connected inductors is 34.2mW, which can be used in some applications requiring higher power.

II. INDUCTOR DESIGN

An inductor with high quality factor Q is able to improve the power deliver efficiency for low power dissipation on the inductor. In order to achieve high Q value of inductor, the inductance should be high, while the resistance should be low [7]-[8]. For this reason, connecting multi-layer metals in parallel to customize an inductor is an effective way to achieve high inductance and low resistance [9]. In this design, four metals are connected parallel to make an inductor, due to the limitation of the metal width defined by foundry. The thickness of each metal layers can be seen in Tab. I.

There are three shape types of inductor, circle, rectangle and octagon, which are used in conventional RF system as shown in Fig. 2. As for a ICPD system, selecting a right shape type of inductor is very necessary to improve the power delivery efficiency. The circular inductor, as is shown in Fig. 2 (a), has a good performance in inductance and the quality

TABLE I. THE METAL THICKNESS

Metal layers	M1	M2	M3	M4	M5	TM2
Thickness(nm)	180	220	220	220	220	3400

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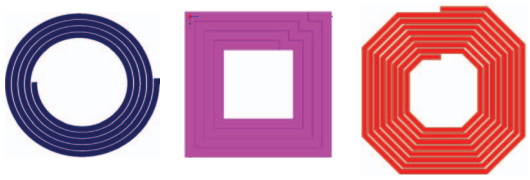


(a) Circular (b) Rectangular (c)Octagonal

Fig. 2. Plannar spiral inductors

factor Q. However, it is hard to be customized and it doesn't make full use of the area, since circle in shape is not easy to be compatible with a layout which is always in rectangular shape.

In order to decide whether a rectangular inductor or an octagonal inductor to be used, a comparison between these two types of inductors is made by using High Frequency Structure Simulator (HFSS). The HFSS simulation model is shown in Fig. 3. The electrical parameters such as self inductance L and parasitic resistance R can be simulated by using this model while the layout parameters such as diameter d, width w, space s and number of turn are fixed. The parameters of these two different shape inductors in Fig. 2 (b) and (c) are shown in Tab. II.

In table I, the layout parameters of these two inductors are exactly the same. By comparing the simulation result of the rectangular inductor and the octagonal inductor, a better shape of inductor is able to be determined to in light of the achieved inductance, quality factor Q and the delivery efficiency. The electrical parameters simulated in HFSS are shown in Fig. 4. The simulation is performed on two shapes of inductors respectively with the frequency ranging from 125 MHz to 250 MHz. The value of self inductance L of both rectangular and the octagonal inductor will decrease along with the frequency increasing as depicted in Fig. 4 (a) and (b). However, the octagonal inductor shows better performance in self inductance since it decreases 0.25 nH of the L while the L of the rectangular inductor decreases 0.37 nH. Fig. 4 (c) and (d) shows that the quality factor Q of these two inductors increase with the frequency rising. But the quality factor Q of the octagonal inductor remains higher than the rectangular inductor. As is described before, an inductor with high quality factor Q and high inductance will improve the wireless power delivery efficiency, so the octagonal inductor is a better option to improve the power delivery efficiency in ICPD.

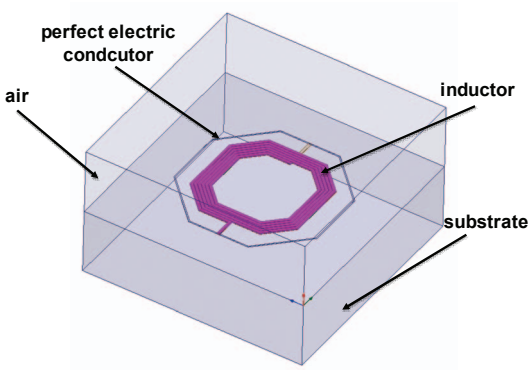
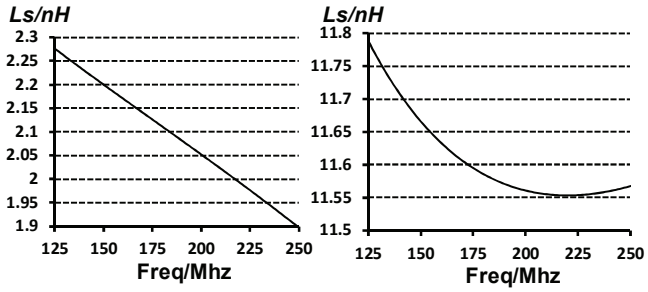


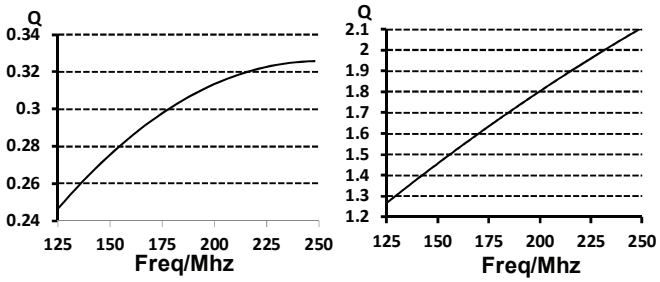
Fig. 3. The HFSS simulation model

TABLE II. THE PARAMETERS OF TWO DIFFERENT SHAPE INDUCTORS

Parameter / Shape	Diameter (d)	Width (w)	Space (s)	Turn	Metal layers
Rectangle	500(μm)	12(μm)	0.5(μm)	3.5	4
Octagon	500(μm)	12(um)	0.5(μm)	3.5	4



(a) L_s of rectangular inductor (b) L_s of octagonal inductor



(c) Q of rectangular inductor (d) Q of octagonal inductor

Fig. 4. The comparision of the two inductors

Once the layout parameters of the inductor is determined, a suitable power delivery distance between two stacked chips should be set in order to get a high coupling coefficient k since a high value of k is crucial to the power delivery efficiency. The relationship between the layout parameters and the coupling coefficient k can be derived as

$$k = \left(\frac{0.35d^2}{X^2 + 0.35d^2} \right)^{\frac{3}{2}} - f(T) \quad (1)$$

where d is the diameter of the inductor and X is the communication distance, $f(T)$ is a metal thickness and inductor shape parameter that indicates the leakage of the magnetic field from edge of the inductor [10]. A clear relation between them can be seen in Fig. 5. When X/d is smaller than 0.1, the value of k is higher than 0.7, which makes possible to get a high coupling coefficient. When X/d is higher than 0.1,

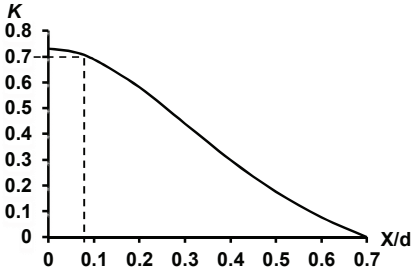
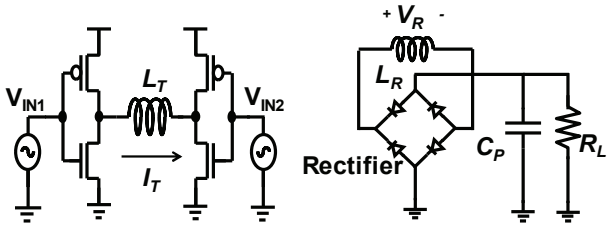


Fig. 5. The relation between k and X/d

the value of k decrease rapidly. Thus, when the diameter of the inductor is fixed, the delivery distance should be set smaller than the value of 0.1*d. The diameter of designed inductor in this work is 500um, the value of k is around 0.7 based on Eq. (1) while the distance X is 50um. The distance X in this design is 50 um which is feasible and relax for most applications.

III. CIRCUIT DESIGN

The ICPD system consists of power transmitter side and power receiver side. As is shown in Fig. 6 (a), an H-bridge inverter circuit is implemented in transmitter side to changes the DC voltage into AC current, so a magnetic field will be produced around the primary inductor L_T. The receiver inductor L_R in Fig. 6 (b) senses the change of the field and engenders AC voltage in itself [9].



(a) transmitter circuit (b) receiver circuit

Fig. 6. Circuit diagram of ICPD

In this work, in order to get a simple equation to describe the delivery efficiency, a simplified model is used in Fig. 7. V_S is the source voltage, R_M is the resistance of the H-bridge, C_T and R_T is the parasitic parameter of primary inductor, and L_T is the inductance of the transmitter inductor. V_R is the voltage engendered on the receiver inductor, C_R is the parasitic parameter of transmitter inductor, RR is the total resistance of rectifier and parameter resistance of receiver inductor, and L_R is the inductance of the receiver inductor. In order to improve the delivery efficiency, the inductors in the transmitter circuit and the receiver circuit should work at the same resonance point [11]. In this condition, the equations can be derived as

$$f = \frac{1}{2\pi\sqrt{L_R C_R}} = \frac{1}{2\pi\sqrt{L_T C_T}} \tag{2}$$

$$Q = 2\pi f \frac{L}{R} \tag{3}$$

$$V_R = Q^2 \cdot K\sqrt{L_T L_R} I_T \tag{4}$$

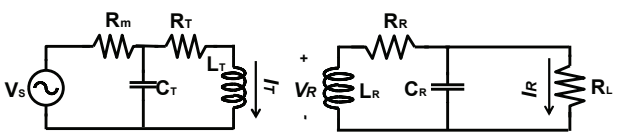


Fig. 7. The equivalent system circuit

The delivery efficiency is the ratio of received power and transmitted power. Refer to Eq. (2), Eq. (3) and Eq. (4), the delivery equation can be derived as

$$P_{efficiency} = \frac{I_R^2 \cdot R}{V_S \cdot I} = \frac{Q^6 \cdot K^2 L_T L_R}{\left(R_L + \frac{L_R}{R_R C_R}\right)} \cdot \frac{R_L}{\left(R_M + \frac{L_T}{R_T C_T}\right)} \tag{5}$$

From Eq. (5), the delivery efficiency is related to Q, K, primary inductance L_T and secondary inductance L_R. In order to improve the power delivery efficiency Pefficiency, high Q value of inductor is required. What's more, based on Eq. (5), if Q is fixed, maximum value of Pefficiency is achieved when the load $R_L = L_R/(R_R \cdot C_R)$. the load R_L will affect the total performance of the system. This means the Q and R_L should be carefully designed in order to achieve high power delivery efficiency. In this design, the value of Q and R_L is 2.5 and 350 Ω respectively.

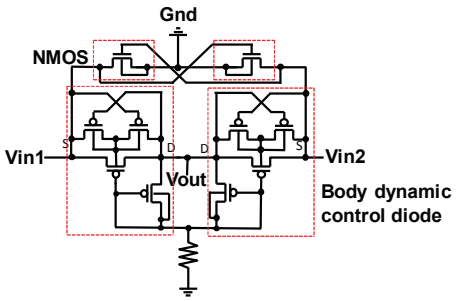


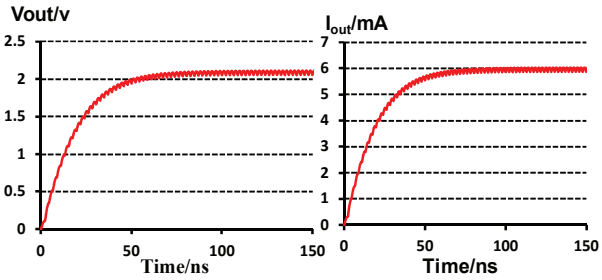
Fig. 8. NMOS cross-gate rectifier

On the purpose of improving the delivery efficiency, the rectifier is specially designed. As is shown in Fig. 8, the rectifier consists of two body dynamic control diodes and two NMOS transistors [9]. The body dynamic control leaves little chance of latch-up and any other leakage to the substrate, even when the voltage swing on the terminal is very large. This cross-gate connection makes the NMOS works with a very high over-drive voltage when it is turned on. So the NMOS cross-gate rectifier incorporates higher power conversion capability.

IV. SIMULATION RESULT

A. Single coil

The delivery system with single coil in the receiver side is simulated, and the output voltage and current are measured. The load is 350 Ω. The operating frequency is 350 Mhz. As shown in Fig. 9, the output voltage is around 2.08V with a ripple of 60mV. The output current is around 5.95mA with a



(a) output voltage (b) output current

Fig. 9. Tested result of the single inducotr receiver

ripple of 0.16mA. So the output power is around 12.3mW. the Simulation also shows the total input power is 94.76mW. By calculating, the delivery efficiency is around 12.9%, and the power density reaches 59.38mW/mm^2. Compared to previous work [6], the improvement of the delivery efficiency and the power density is 25.5% and 197% , respectively.

In the transmitter side, the primary circuit consumed 83.65mW. In the receiver side, the secondary inductor received 17.47mW, the load consumed 12.3mW, and the rectifier consumed 5.17mW. The coupling efficiency is 0.21.

B. Parallel power link

The delivery system with single inductor can only provide 12.3mW, so a parallel inductive power link, as shown in Fig. 10, is proposed to increase the received power [12]. The parallel power link system consists of four pairs of inductors, H-bridge inverters and rectifiers. Each pair of the inductors work in parallel in order to achieve higher output power.

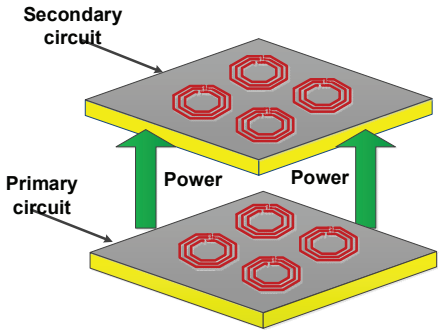
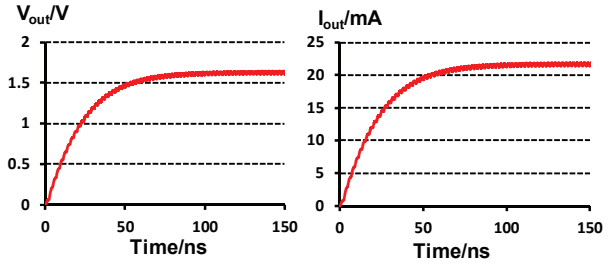


Fig. 10. Parallel Power Link



(a) output voltage (b)output current

Fig. 11. Tested result of the four parallel inductors receiver

As is shown in Fig. 11, the output voltage is around 1.6 V, and the output current is around 21.4 mA. So the received power is around 34.2 mW with 10% of the delivery efficiency and 20.65mW/mm^2 of the power density while the load is 75 Ω. Thus if the area is allowed for a ICPD system, a parallel power link can be implemented with the diameter of each coil is 500 μm. It achieves 10% of the delivery efficiency and 20.7mW/mm^2 of the power density. This prototype can be implemented in some applications requiring higher power.

V. CONCLUSION

A ICPD system for 3-D stacked chips in SMIC 65-nm CMOS process is presented in this paper. The delivery efficiency is improved by using optimized octagonal inductors and NMOS gate-cross rectifier. the output power of the receiver with single inductor is 12.05mW with a delivery efficiency of 12.7% and a power density of 59.5 mW/mm^2. Compared to previous publications [6] shown is table III, this prototype achieves an improvement of x1.2 in power delivery efficiency and x2.97 in power density. In the parallel power link which can be used in some applications requiring higher power, the received power reaches 34.2 mW with 10% of the delivery efficiency and 20.7 mW/mm^2 of the power density. In these two prototypes, the operating frequency is around 230 MHz. A higher working frequency can minimize the size of the inductor and therefore improve the power density a lot [11]. But the transmitter in [11] is off-chip and the inductor is hand-wound with 80um-thick wire, which has a better performance compared to an on-chip inductor. Also, in a wireless communication system, the data is usually transmitted in giga hertz, which may increase the crosstalk between the data and the power. The operating frequency in this work is much smaller than that of a wireless data transmission system, which is helpful to decrease the magnetic interference between the data and the power in a SiP [13].

TABLE III. PERFORMANCE COMPARISION

	This work Single Coil	This work Parallel Power Link	Yuan VLSI'10[6]	Onizuka CICC'06[14]	Sangwook Han CICC'12[11]
Received Power	12.3mW	34.2mW	10mW	2.5mW	8.78mW
Coil Size	0.5x0.5mm^2	0.5x0.5mm^2	0.7x0.7mm^2	0.7x0.7mm^2	0.12x0.12mm^2
Power Density	59.4mW/mm^2	20.7mW/mm^2	20mW/mm^2	5.1mW/mm^2	0.61W/mm^2
Power Efficiency	12.8%	10%	10.2%	–	19%
Carrier Frequency	230Mhz	230Mhz	–	150~350Mhz	3.5Ghz
Technology	65nm CMOS	65nm CMOS	65nm CMOS	0.35μm CMOS	65nm CMOS

ACKNOWLEDGMENT

This work was supported by the National Natural Science Foundation of China (NSFC61306028) and Funds of National College Students'Innovative Program (20141033503712).

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